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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28243-24pvxit

PSoC Functional Overview

The PSoC family consists of many devices with On-Chip Controllers. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog blocks, digital blocks, and interconnections. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. In addition, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The CY8C28xxx group of PSoC devices described in this datasheet have multiple resource configuration options available. Therefore, not every resource mentioned in this datasheet is available for each CY8C28xxx subgroup. The CY8C28x45 subgroup has a full feature set of all resources described. There are six more segmented subgroups that allow designers to use a device with only the resources and functionality necessary for a specific application. See Table 2 on page 9 to determine the resources available for each CY8C28xxx subgroup. The same information is also presented in more detail in the Ordering Information section.

The architecture for this specific PSoC device family, as shown in the Logic Block Diagram on page 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. The configurable global bus system allows all the device resources to be combined into a complete custom system. PSoC CY8C28xxx family devices have up to six I/O ports that connect to the global digital and analog interconnects, providing access to up to 12 digital blocks and up to 16 analog blocks.

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general Purpose I/O (GPIO). The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microcontroller.

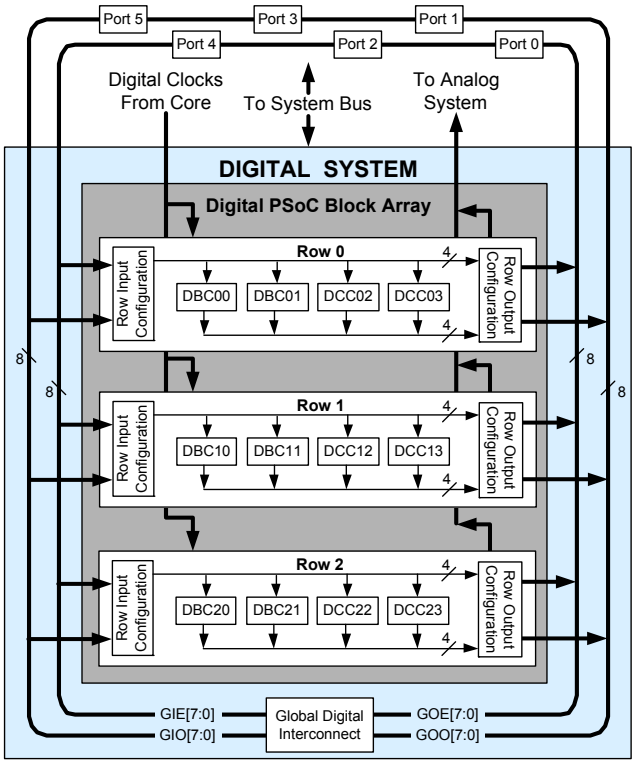
Memory encompasses 16K bytes of Flash for program storage, 1K bytes of SRAM for data storage. The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 2.5% over temperature and voltage. A low power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and watch dog timer (WDT). The 32.768 kHz external crystal oscillator (ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL.

PSoC GPIOs provide connections to the CPU, and digital and analog resources. Each pin's drive mode may be selected from 8 options, which allows great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of up to 12 configurable digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to create 8, 16, 24, and 32-bit peripherals, which are called user modules. The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin.

Figure 2. Digital System Block Diagram[1]



Digital peripheral configurations include:

- PWMs (8- and 16-bit, One-shot and Multi-shot capability)
- PWMs with Dead band/Kill (8- and 16-bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- Full-duplex 8-bit UARTs (up to 3) with selectable parity
- Half-duplex 8-bit UARTs (up to 6) with selectable parity
- Variable length SPI slave and master
  - Up to 6 total slaves and masters (8-bit)
  - Supports 8 to 16 bit operation
- I^2C slave, master, or multi-master (up to 2 available as System Resources)
- IrDA (up to 3)
- Pseudo Random Sequence Generators (8 to 32 bit)
- Cyclical Redundancy Checker/Generator (16 bit)
- Shift Register (2 to 32 bit)

Note
1. CY8C28x52 devices do not have digital block row 2. They have two digital rows with eight total digital blocks.

The devices covered by this datasheet all have the same architecture, specifications, and ratings. However, the amount of some hardware resources varies from device to device within the group. The following table lists resources available for the specific device subgroups covered by this datasheet.

Table 2. CY8C28xxx Device Characteristics

PSoC Part Number	CapSense	Digital Blocks	Regular Analog Blocks	Limited Analog Blocks	HW I^2C	Decimators	Digital I/O	Analog Inputs	Analog Outputs	Analog Mux Buses
CY8C28x03	N	12	0	0	2	0	up to 24	up to 8	0	0
CY8C28x13	Y	12	0	4	1	2	up to 40	up to 40	0	2
CY8C28x23	N	12	6	0	2	2	up to 44	up to 10	2	0
CY8C28x33	Y	12	6	4	1	4	up to 40	up to 40	2	2
CY8C28x43	N	12	12	0	2	4	up to 44	up to 44	4	2
CY8C28x45	Y	12	12	4	2	4	up to 44	up to 44	4	2
CY8C28x52	Y	8	12	4	1	4	up to 24	up to 24	4	2

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Table 14. CY8C28x33 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 18. CY8C28x45 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#	ASC12CR0	88	RW		C8	
PRT2IE	09	RW	DCC22DR1	49	W	ASC12CR1	89	RW		C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW	ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#	ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW	DCC23DR0	4C	#	ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW	DCC23DR1	4D	W	ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW	ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC	I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC	I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW	DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

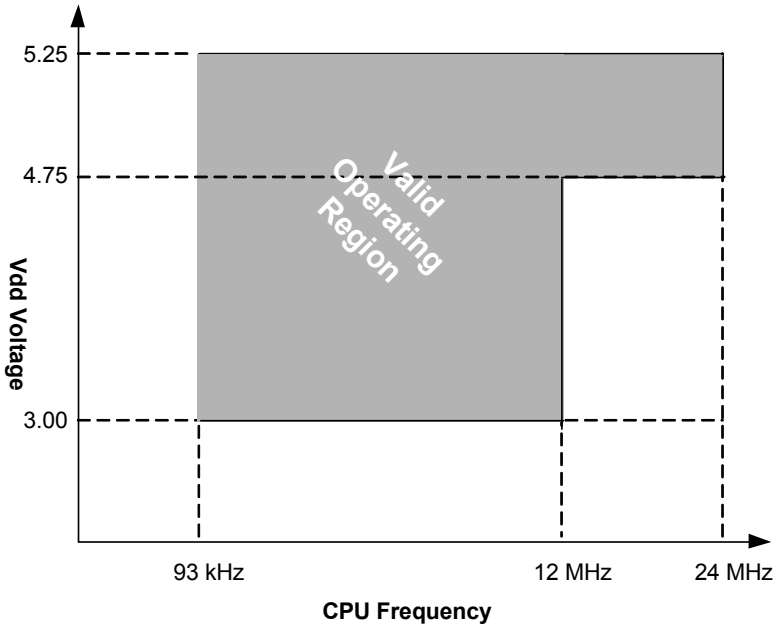
Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C28xxx PSoC devices. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http//www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications for devices running at greater than 12 MHz are valid for –40 °C ≤ T_A ≤ 70 °C and T_J ≤ 82 °C.

Figure 8. Voltage versus CPU Frequency



DC Electrical Characteristics

DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.00	–	5.25	V	
I_{DD}	Supply current	–	8	14	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DD3}	Supply current	–	5	9	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DDP}	Supply current when IMO = 6 MHz using SLIMO mode=1	–	2	3	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT.[12]	–	3	10	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C.
I_{SBH}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT at high temperature.[12]	–	4	25	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, sleep timer, WDT, and external crystal.[12]	–	4	13	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C.
I_{SBXTLH}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and external crystal at high temperature.[12]	–	5	26	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
I_{SBRTC}	Current consumed by RTC during sleep	–	0.5	1	µA	Extra current consumed by the RTC during sleep. This number is typical at 25 °C and 5 V.
V_{REF}	Reference voltage (Bandgap)	1.280	1.300	1.320	V	Trimmed for appropriate V_{DD}.
I_{SXRES}	Supply current with XRES asserted 5 V	–	0.65	3	mA	Max is peak current after XRES; Typical value is the steady state current value. T_A = 25 °C.
	Supply current with XRES asserted 3.3 V	-	0.4	1.5	mA	

Note
12. Standby (sleep) current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD} – 1.0 V, see the limitations of the total current in the note for V_{OH}.
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25.
V_{IH}	Input high level	2.1	–	–	V	V_{DD} = 3.0 to 5.25.
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. 5 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	20	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 0.5 × V_{DD} + 1.3 0.5 × V_{DD} + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.0) ≤ V_{OUT} ≤ (0.5 × V_{DD} + 0.9).

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 34. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.214	$V_{DD}/2$ + 1.279	$V_{DD}/2$ + 1.341	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.018	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.01	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.301	$V_{DD}/2$ – 1.273	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 0.228	$V_{DD}/2$ + 1.284	$V_{DD}/2$ + 1.344	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.015	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.011	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.303	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.287	$V_{DD}/2$ + 1.345	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.276	V

Note
15. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.055	P2[4] + P2[6] – 0.019	P2[4] + P2[6] + 0.019	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.035	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.05	P2[4] + P2[6] – 0.015	P2[4] + P2[6] + 0.021	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.001	P2[4] – P2[6] + 0.031	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.048	P2[4] + P2[6] – 0.013	P2[4] + P2[6] + 0.022	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] – 0.001	P2[4] – P2[6] + 0.031	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.047	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.023	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.036	P2[4] – P2[6] – 0.002	P2[4] – P2[6] + 0.030	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.028	V_{DD} – 0.010	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.002	V_{DD}/2 + 0.012	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.008	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.021	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.001	V_{DD}/2 + 0.012	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.005	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.019	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.001	V_{DD}/2 + 0.012	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.004	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.017	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.001	V_{DD}/2 + 0.013	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.003	V

Table 35. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.226	P2[4] + 1.286	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.323	P2[4] – 1.293	P2[4] –1.262	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.232	P2[4] + 1.29	P2[4] + 1.344	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.296	P2[4] – 1.267	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.233	P2[4] + 1.291	P2[4] + 1.345	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.298	P2[4] – 1.269	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.234	P2[4] + 1.292	P2[4] +1.345	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.299	P2[4] – 1.270	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.504	2.595	2.672	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.013	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.593	2.674	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.008	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.594	2.675	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.007	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.507	2.595	2.675	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.005	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices, for more information on the VLT_CR register.

Table 40. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} Value for PPOR Trip (positive ramp)					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0R}	PORLEV[1:0] = 00b	–	2.91	2.985	V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	4.49	V	
V_{PPOR2R}	PORLEV[1:0] = 10b	–	4.55	4.65	V	
	V_{DD} Value for PPOR Trip (negative ramp)					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.82	2.90	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	4.49	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.64	V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.83	2.91	3.00[16]	V	
V_{LVD1}	VM[2:0] = 001b	2.93	3.01	3.10	V	
V_{LVD2}	VM[2:0] = 010b	3.04	3.12	3.21	V	
V_{LVD3}	VM[2:0] = 011b	3.90	3.99	4.09	V	
V_{LVD4}	VM[2:0] = 100b	4.38	4.47	4.58	V	
V_{LVD5}	VM[2:0] = 101b	4.54	4.63	4.74[17]	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.71	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.80	4.92	V	
	V_{DD} Value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.93	3.01	3.10	V	
V_{PUMP1}	VM[2:0] = 001b	3.00	3.08	3.17	V	
V_{PUMP2}	VM[2:0] = 010b	3.16	3.24	3.33	V	
V_{PUMP3}	VM[2:0] = 011b	4.09	4.17	4.28	V	
V_{PUMP4}	VM[2:0] = 100b	4.53	4.62	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.61	4.71	4.82	V	
V_{PUMP6}	VM[2:0] = 110b	4.70	4.80	4.91	V	
V_{PUMP7}	VM[2:0] = 111b	4.88	4.98	5.10	V	

Notes
16. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
17. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 43. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6[21]	MHz	Trimmed. Utilizing factory trim values. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[21]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. SLIMO Mode = 1.
F_{CPU1}	CPU Frequency (5 V Nominal)	0.091	24	24.6[21]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F_{CPU2}	CPU Frequency (3.3 V Nominal)	0.091	12	12.3[22]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F_{BLK5}	Digital PSoC Block Frequency	0	–	49.2[21, 23]	MHz	4.75 V< V_{DD} <5.25 V
F_{BLK33}	Digital PSoC Block Frequency	0	24	24.6[23]	MHz	3.0 V<V_{DD}<3.6 V
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	Trimmed. Utilizing factory trim values.
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	Internal Low Speed Oscillator Untrimmed Frequency	5	–	100	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference manual for details on timing this.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Multiple (x732) of crystal frequency.
$t_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$t_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{DD} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.

Notes
21. 4.75 V < V_{DD} < 5.25 V.
22. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
23. See the individual user module datasheets for information on maximum frequencies for user modules.

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 55. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
t_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
t_{WRITE}	Flash Block Write Time	–	40	–	ms	
t_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	55	ns	$V_{DD} > 3.6$
t_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	75	ns	$3.0 \le V_{DD} \le 3.6$
$t_{ERASEALL}$	Flash Erase Time (Bulk)	–	40	–	ms	Erase all blocks and protection fields at once.
$t_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100[30]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200[30]	ms	–40 °C ≤ Tj ≤ 0 °C

Note
30. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note, AN2015 at http://ww.cypress.com under Application Notes for more information.

Figure 18. 28-pin SSOP (210 Mils) O28.21 Package Outline, 51-85079

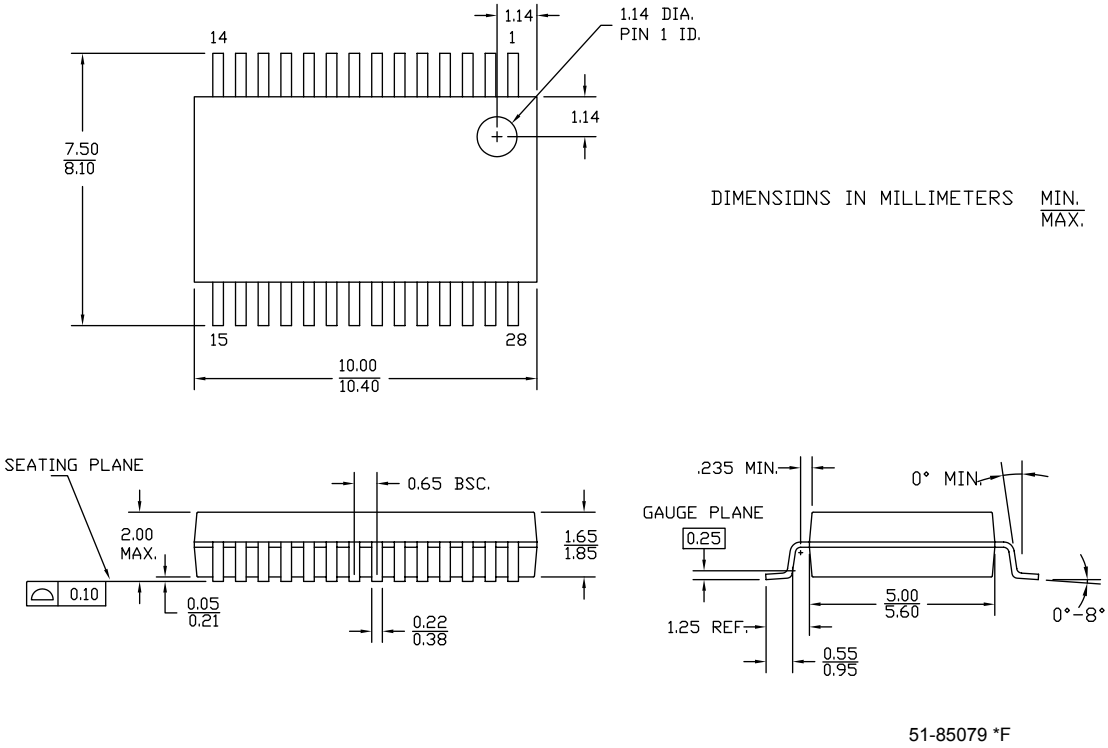
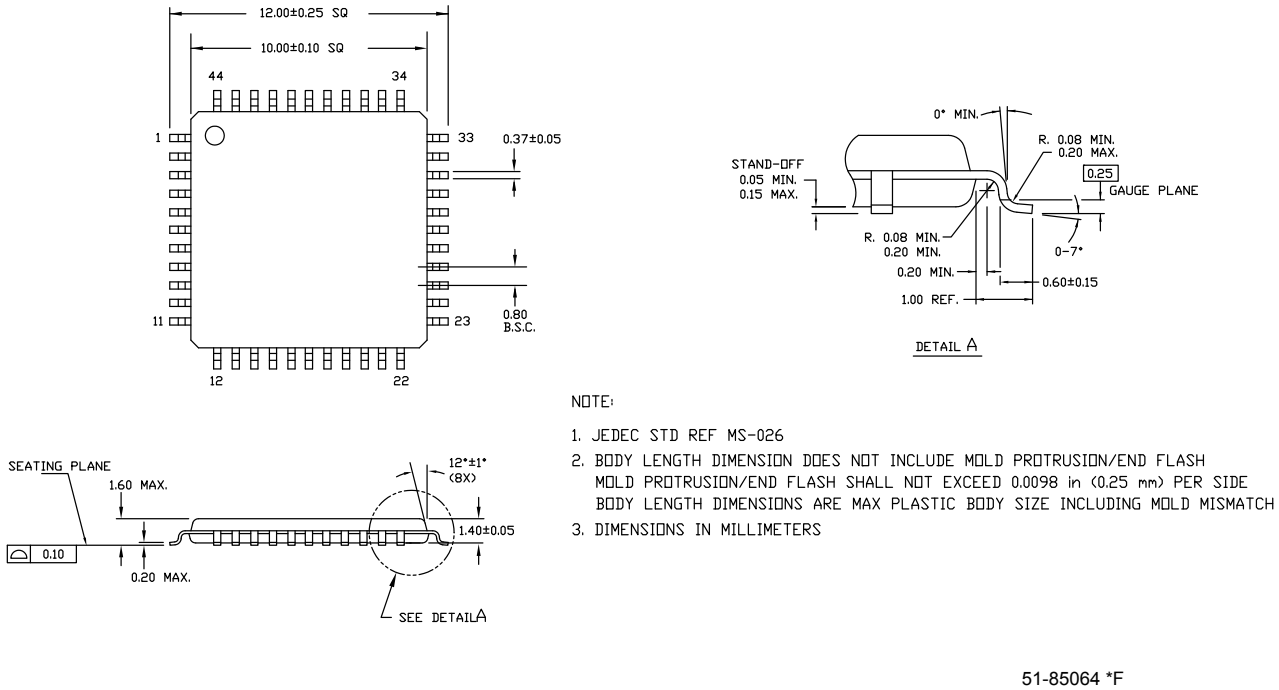


Figure 19. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064



Ordering Information

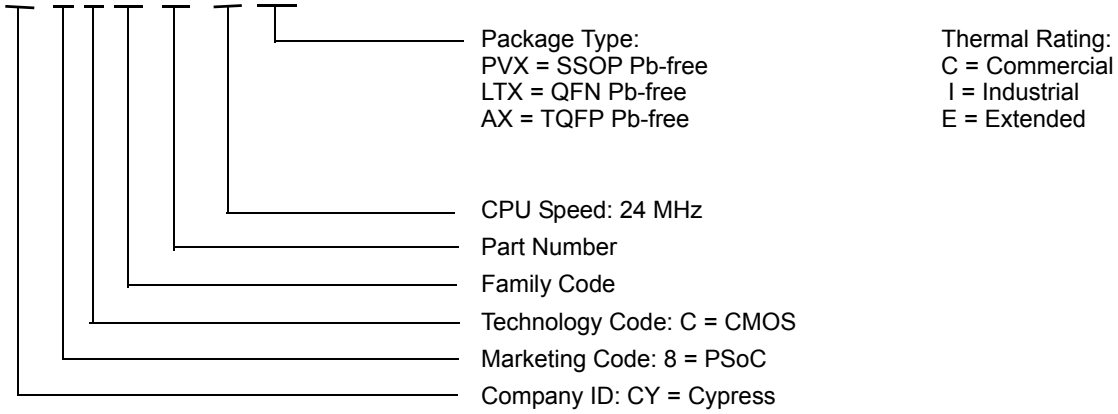
The following table lists the CY8C28xxx PSoC devices key package features and ordering codes.

Package	Ordering Code	Temperature Range	CapSense	Digital Blocks	Regular Analog Blocks	Limited Analog Blocks	HW I^2C	Decimators	10-bit SAR ADC	Digital I/O Pins	Analog Inputs	Analog Outputs	Flash (KBytes)	RAM (KBytes)	XRES Pin
28-Pin (210-Mil) SSOP	CY8C28403-24PVXI	–40 °C to 85 °C	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28403-24PVXIT	–40 °C to 85 °C	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28413-24PVXI	–40 °C to 85 °C	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28413-24PVXIT	–40 °C to 85 °C	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
44-Pin TQFP	CY8C28513-24AXI	–40 °C to 85 °C	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28513-24AXIT	–40 °C to 85 °C	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
48-Pin Sawn QFN	CY8C28623-24LTXI	–40 °C to 85 °C	N	12	6	0	2	2	N	44	10	2	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28623-24LTXIT	–40 °C to 85 °C	N	12	6	0	2	2	N	44	10	2	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28433-24PVXI	–40 °C to 85 °C	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28433-24PVXIT	–40 °C to 85 °C	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
20-Pin (210-Mil) SSOP	CY8C28243-24PVXI	–40 °C to 85 °C	N	12	12	0	2	4	Y	16	16	4	16	1	Y
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28243-24PVXIT	–40 °C to 85 °C	N	12	12	0	2	4	Y	16	16	4	16	1	Y
48-Pin Sawn QFN	CY8C28643-24LTXI	–40 °C to 85 °C	N	12	12	0	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28643-24LTXIT	–40 °C to 85 °C	N	12	12	0	2	4	Y	44	44	4	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28445-24PVXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28445-24PVXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
44-Pin TQFP	CY8C28545-24AXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28545-24AXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
48-Pin Sawn QFN	CY8C28645-24LTXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28645-24LTXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28452-24PVXI	–40 °C to 85 °C	Y	8	12	4	1	4	N	24	24	4	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28452-24PVXIT	–40 °C to 85 °C	Y	8	12	4	1	4	N	24	24	4	16	1	Y
56-Pin SSOP OCD	CY8C28000-24PVXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

CY 8 C 28 xxx - SP xxxx



Glossary *(continued)*

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

1. 10-bit SAR ADC does not meet DNL/INL specification.

■ **Problem Definition**

The 10-bit hardware SAR ADC does not meet datasheet accuracy specifications for DNL and INL under some conditions.

■ **Parameters Affected**

INLSAR10: Integral nonlinearity

DNLSAR10: Differential nonlinearity

■ **Trigger Condition(S)**

The SAR ADC DNL has been measured greater than 2 LSB over temperature in all cases, as compared to the datasheet specification of 1.5 LSB.

When using the VPWR (Vdd) reference configuration, the SAR ADC DNL has been measured over temperature at 2 LSB for a supply voltage of 3.3 V. With a supply voltage of 5.5 V, the DNL has been measured greater than 3.5 LSB.

■ **Scope of Impact**

Inaccurate converted data.

■ **Workaround**

- Use an alternate ADC implementation (DelSig, ADCINC) available in CY8C28xxx devices.
- Avoid CPU operations that change the address and data buses while A-D conversion is running with internal Vpwr (Vdd) as Vref.
- Use un-buffered RefHi as ADC Vref. This may have a negative effect on the analog blocks in the analog array due to the noise introduced on RefHi reference.

■ **Fix Status**

Silicon fix is not planned. The workaround mentioned above should be used.

2. Wrong data read from IDAC_CRx and DACx_D registers.

■ **Problem Definition**

The CPU may read an incorrect value of bits 0, 3, 5, or 7 from the following registers:

- IDAC_CR0
- IDAC_CR1
- DAC0_D
- DAC1_D

■ **Parameters Affected**

F_{CPU1} and F_{CPU2} from the device data sheet.

■ **Trigger Condition(S)**

When CPU Clock is set at its highest frequency setting (24 MHz nominal).

■ **Scope of Impact**

Incorrect data read from affected registers.

■ **Workaround**

Temporarily slow down CPU Clock frequency to 12 MHz nominal (or lower) when affected registers are read.