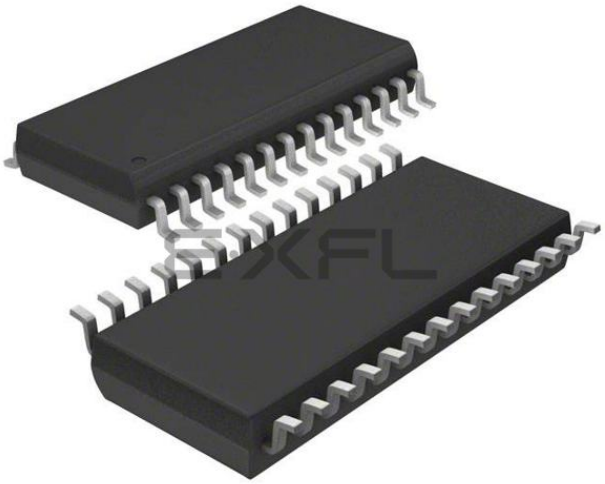

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28403-24pvxit

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

Note: For CY8C28xxx devices related Application note please click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C28xxx devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout

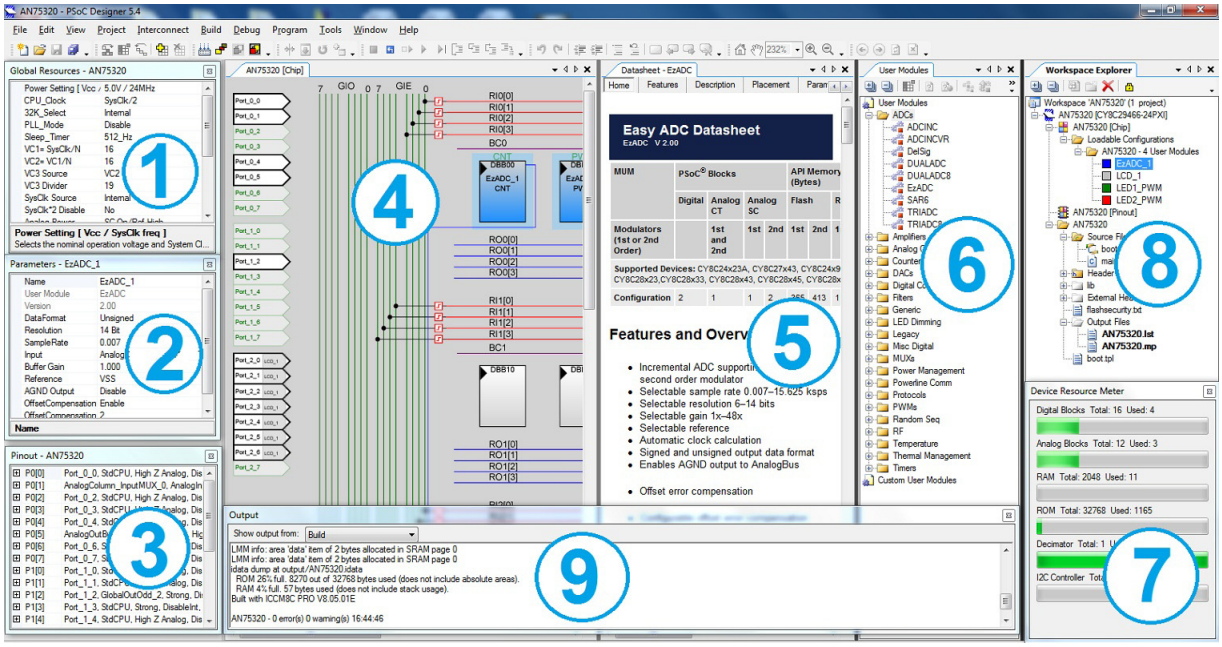


Figure 6. Analog System Block Diagram for CY8C28x23 Devices

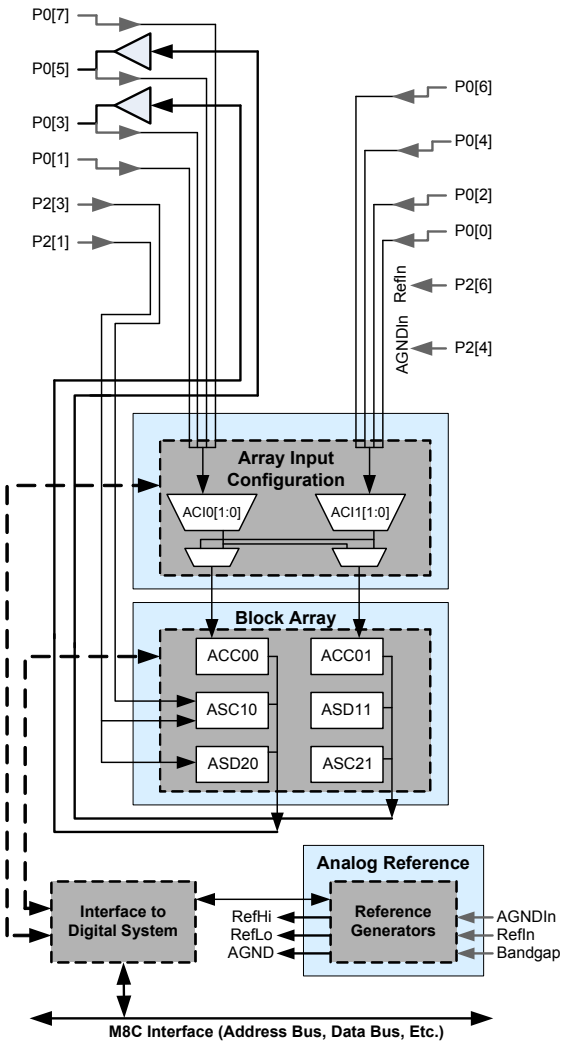
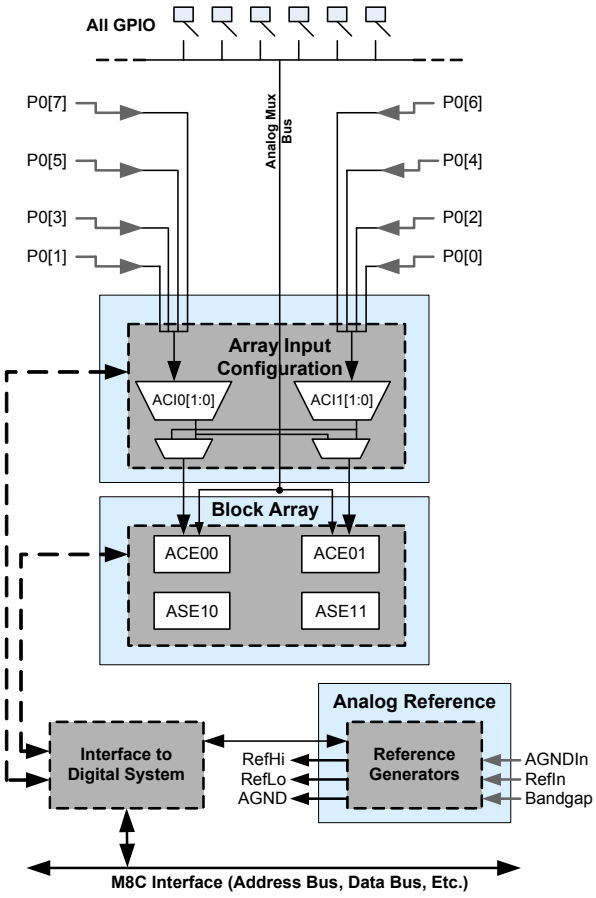


Figure 7. Analog System Block Diagram for CY8C28x13 Devices



Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Table 7. 56-pin Part Pinout (SSOP) *(continued)*

Pin No.	Type		Pin Name	Description
	Digital	Analog		
41	Input		XRES	Active high external reset with internal pull-down.
42	OCD	M	HCLK	OCD high speed clock output.
43	OCD	M	CCLK	OCD CPU clock output.
44	I/O	M	P4[0]	
45	I/O	M	P4[2]	
46	I/O	M	P4[4]	
47	I/O	M	P4[6]	
48	I/O	I, M	P2[0]	Direct switched capacitor block input.
49	I/O	I, M	P2[2]	Direct switched capacitor block input.
50	I/O	M	P2[4]	External Analog Ground (AGND).
51	I/O	M	P2[6]	External Voltage Reference (VRef).
52	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.
53	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.
54	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.
55	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.
56	Power		V_{DD}	Supply voltage.

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, M = Analog Mux Bus Input, and OCD = On-Chip Debug.

Table 8. CY8C28x03 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#		80		RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W		81		RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW		82		RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#		83		RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#		84		RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W		85		RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW		86		RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#		87		RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
PRT4GS	12	RW		52			92			D2	
PRT4DM2	13	RW		53			93		IDX_PP	D3	RW
PRT5DR	14	RW		54			94		MVR_PP	D4	RW
PRT5IE	15	RW		55			95		MVW_PP	D5	RW
PRT5GS	16	RW		56			96		I2C0_CFG	D6	RW
PRT5DM2	17	RW		57			97		I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#		60			A0		INT_MSK0	E0	RW
DBC00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBC00DR2	22	RW		62			A2		INT_VC	E2	RC
DBC00CR0	23	#		63			A3		RES_WDT	E3	W
DBC01DR0	24	#		64			A4		I2C1_SCR	E4	#
DBC01DR1	25	W		65			A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW		66			A6			E6	
DBC01CR0	27	#	I2C1_DR	67	RW		A7			E7	
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RDI0RI	B0	RW		F0	
DBC10DR1	31	W		71		RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR0	33	#		73		RDI0LT0	B3	RW		F3	
DBC11DR0	34	#		74		RDI0LT1	B4	RW		F4	
DBC11DR1	35	W		75		RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR0	37	#		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 9. CY8C28x03 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51			91		GDI_E_IN	D1	RW
PRT4IC0	12	RW		52			92		GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94			D4	
PRT5DM1	15	RW		55			95			D5	
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW		60		GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW		61		GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW		62		GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW		63		GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW		64		RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW		E5	
DBC01OU	26	RW		66		RTC_S	A6	RW		E6	
DBC01CR1	27	RW		67		RTC_CR	A7	RW		E7	
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW		69		SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW		6A		SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW		EC	
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 12. CY8C28x23 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4		I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#		A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW		A7		DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 14. CY8C28x33 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 20. CY8C28x52 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 27. 3.3 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOACT}	Input Offset Voltage CT Blocks (absolute value) Power = Low, Opamp bias = High Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 1.65 1.32 –	 8 8 –	 mV mV mV	
V_{OSOA}	Input Offset Voltage SC and AGND (absolute value)	–	1	6	mV	Applies to High and Low Opamp bias.
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common Mode Rejection Ratio Power = Low Power = Medium Power = High	 50 50 50	 – – –	 – – –	 dB dB dB	
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	 60 60 80	 – – –	 – – –	 dB dB dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High is 5 V only	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High	 – – –	 – – –	 0.2 0.2 0.2	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 200 400 700 1400 2400 4600	 300 600 1000 2000 3600 7500	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	50	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25\ V)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 32. 3.3 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	20	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 – –	 – –	 $0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	47	64	–	dB	$(0.5 \times V_{DD} - 1.0) \le V_{OUT} \le (0.5 \times V_{DD} + 0.9)$.

Table 35. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.226	P2[4] + 1.286	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.323	P2[4] – 1.293	P2[4] –1.262	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.232	P2[4] + 1.29	P2[4] + 1.344	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.296	P2[4] – 1.267	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.233	P2[4] + 1.291	P2[4] + 1.345	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.298	P2[4] – 1.269	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.234	P2[4] + 1.292	P2[4] +1.345	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.299	P2[4] – 1.270	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.504	2.595	2.672	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.013	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.593	2.674	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.008	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.594	2.675	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.007	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.507	2.595	2.675	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.005	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 43. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6[21]	MHz	Trimmed. Utilizing factory trim values. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[21]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. SLIMO Mode = 1.
F_{CPU1}	CPU Frequency (5 V Nominal)	0.091	24	24.6[21]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F_{CPU2}	CPU Frequency (3.3 V Nominal)	0.091	12	12.3[22]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F_{BLK5}	Digital PSoC Block Frequency	0	–	49.2[21, 23]	MHz	4.75 V< V_{DD} <5.25 V
F_{BLK33}	Digital PSoC Block Frequency	0	24	24.6[23]	MHz	3.0 V<V_{DD}<3.6 V
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	Trimmed. Utilizing factory trim values.
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	Internal Low Speed Oscillator Untrimmed Frequency	5	–	100	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference manual for details on timing this.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Multiple (x732) of crystal frequency.
$t_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$t_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{DD} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.

Notes
21. 4.75 V < V_{DD} < 5.25 V.
22. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
23. See the individual user module datasheets for information on maximum frequencies for user modules.

AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp bias = High is not supported at 3.3 V.

Table 45. 5 V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	
t_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	
SR_{FOA}	Falling Slew Rate (80% to 20%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	
E_{NOA}	Noise at 1 kHz Power = Medium, Opamp bias = High	–	100	–	nV/rt-Hz	

Figure 18. 28-pin SSOP (210 Mils) O28.21 Package Outline, 51-85079

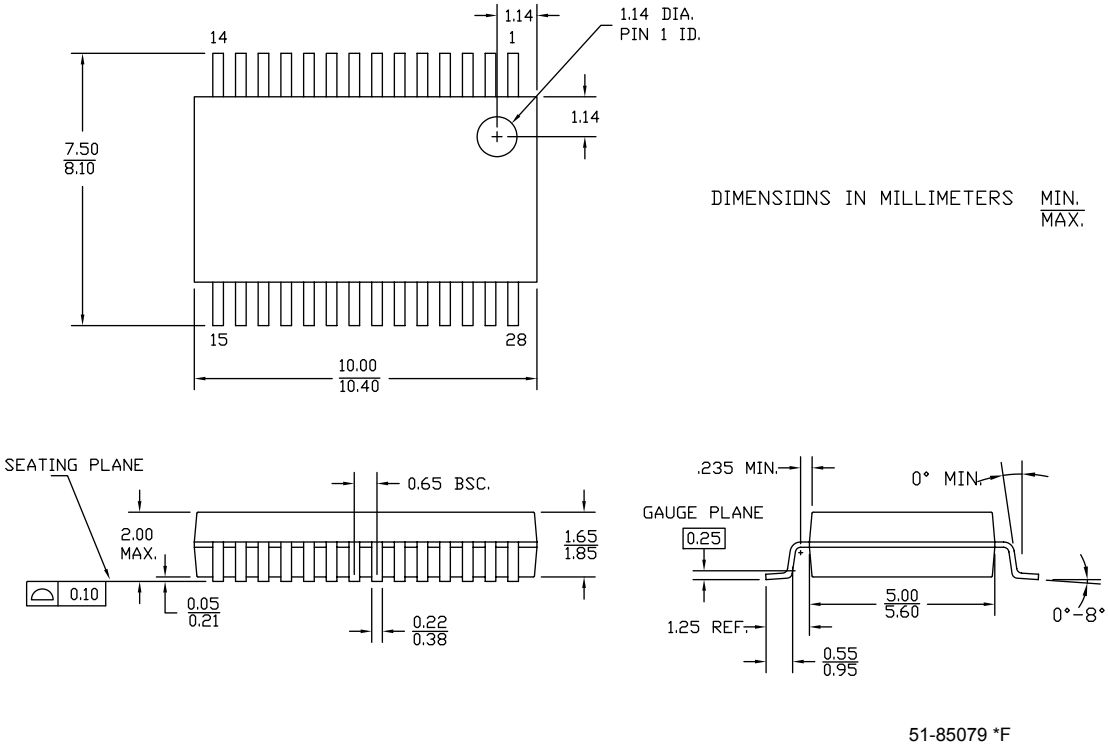
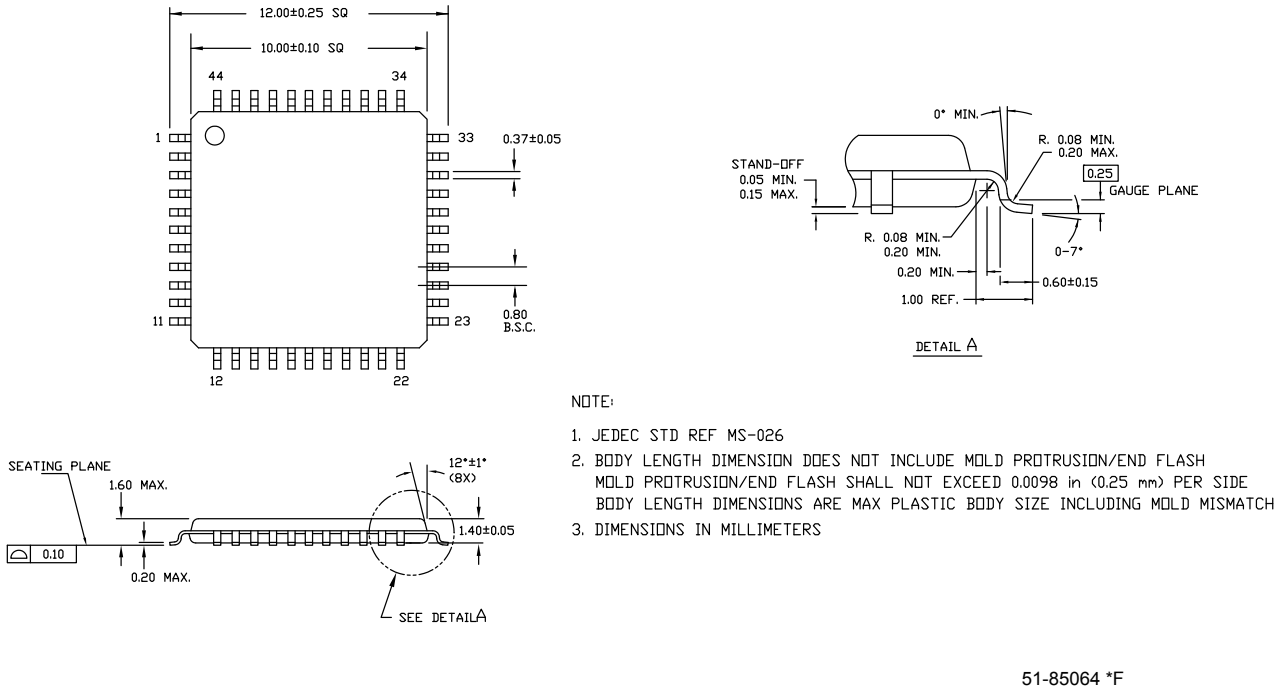


Figure 19. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064



Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C28xxx family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at http://www.cypress.com.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the content of specific memory locations. Advanced emulation features are supported in PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- Pod kit for CY8C29x66 PSoC Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Ordering Information

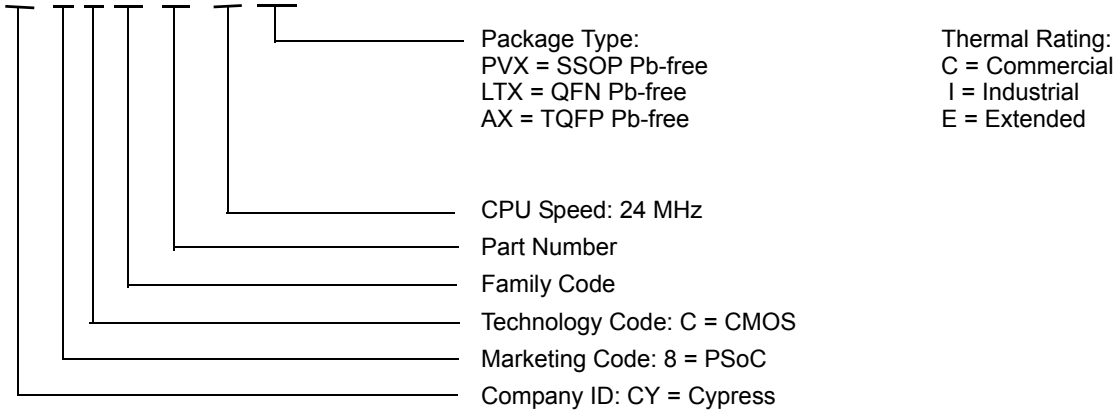
The following table lists the CY8C28xxx PSoC devices key package features and ordering codes.

Package	Ordering Code	Temperature Range	CapSense	Digital Blocks	Regular Analog Blocks	Limited Analog Blocks	HW I^2C	Decimators	10-bit SAR ADC	Digital I/O Pins	Analog Inputs	Analog Outputs	Flash (KBytes)	RAM (KBytes)	XRES Pin
28-Pin (210-Mil) SSOP	CY8C28403-24PVXI	–40 °C to 85 °C	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28403-24PVXIT	–40 °C to 85 °C	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28413-24PVXI	–40 °C to 85 °C	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28413-24PVXIT	–40 °C to 85 °C	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
44-Pin TQFP	CY8C28513-24AXI	–40 °C to 85 °C	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28513-24AXIT	–40 °C to 85 °C	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
48-Pin Sawn QFN	CY8C28623-24LTXI	–40 °C to 85 °C	N	12	6	0	2	2	N	44	10	2	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28623-24LTXIT	–40 °C to 85 °C	N	12	6	0	2	2	N	44	10	2	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28433-24PVXI	–40 °C to 85 °C	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28433-24PVXIT	–40 °C to 85 °C	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
20-Pin (210-Mil) SSOP	CY8C28243-24PVXI	–40 °C to 85 °C	N	12	12	0	2	4	Y	16	16	4	16	1	Y
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28243-24PVXIT	–40 °C to 85 °C	N	12	12	0	2	4	Y	16	16	4	16	1	Y
48-Pin Sawn QFN	CY8C28643-24LTXI	–40 °C to 85 °C	N	12	12	0	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28643-24LTXIT	–40 °C to 85 °C	N	12	12	0	2	4	Y	44	44	4	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28445-24PVXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28445-24PVXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
44-Pin TQFP	CY8C28545-24AXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28545-24AXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
48-Pin Sawn QFN	CY8C28645-24LTXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28645-24LTXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28452-24PVXI	–40 °C to 85 °C	Y	8	12	4	1	4	N	24	24	4	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28452-24PVXIT	–40 °C to 85 °C	Y	8	12	4	1	4	N	24	24	4	16	1	Y
56-Pin SSOP OCD	CY8C28000-24PVXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

CY 8 C 28 xxx - SP xxxx



Acronyms

Acronyms Used

Table 61 lists the acronyms that are used in this document.

Table 61. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC®	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SLIMO	slow IMO
IMO	internal main oscillator	SMP	switch mode pump
I/O	input/output	SOIC	small-outline integrated circuit
IrDA	infrared data association	SPI™	serial peripheral interface
ISSP	in-system serial programming	SRAM	static random access memory
LCD	liquid crystal display	SROM	supervisory read only memory
LED	light-emitting diode	SSOP	shrink small-outline package
LPC	low power comparator	UART	universal asynchronous receiver / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 available at http://www.cypress.com.

Document History Page *(continued)*

Document Title: CY8C28243/CY8C28403/CY8C28413/CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/ CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™
Document Number: 001-48111

Revision	ECN	Origin of Change	Submission Date	Description of Change
*L	3993399	GVH	05/08/2013	Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata.
*M	4138595	GVH	09/27/2013	Updated to new template. Completing Sunset Review.
*N	4476160	ASRI / SEG	09/04/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added More Information. Added PSoC Designer. Updated PSoC Functional Overview: Updated PSoC Device Characteristics: Updated Table 2: Added a column “Analog Mux Buses” at the end. Removed “Getting Started”. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC I2C Specifications: Updated Table 42: Added V_{OLI2C} parameter and its details. Updated Packaging Information: spec 51-85064 – Changed revision from *E to *F. Completing Sunset Review.
*O	4914758	ASRI	09/10/2015	Updated Document Title to read as “CY8C28243/CY8C28403/CY8C28413/ CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/ CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™”. Removed CY8C28533 related information in all instances across the document. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC SAR10 ADC Specifications: Updated Table 38: Updated details in “Description” column of DNL_{SAR10} parameter. Updated Packaging Information: Updated Packaging Dimensions: spec 51-85077 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. spec 001-45616 – Changed revision from *D to *E. Updated Development Tool Selection: Updated Accessories (Emulation and Programming): Updated Table 60: Updated details in “Part #” column corresponding to 44-pin TQFP package. Updated Ordering Information: Updated part numbers. Updated Errata: Updated Part Numbers Affected: Updated table. Updated Errata Summary: Updated table and also details below the table. Updated to new template. Completing Sunset Review.