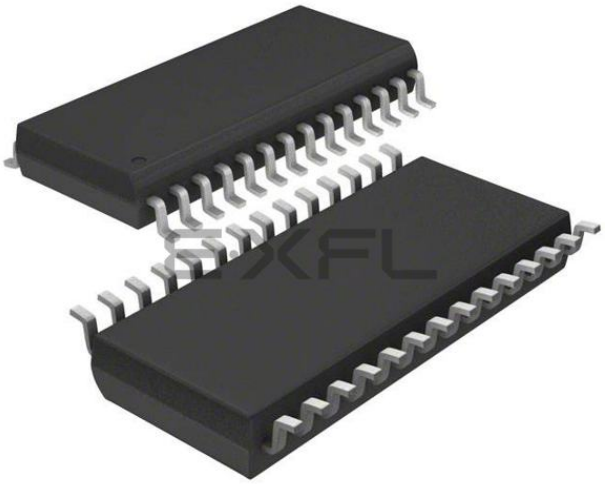

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28413-24pvxi

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

Note: For CY8C28xxx devices related Application note please click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C28xxx devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

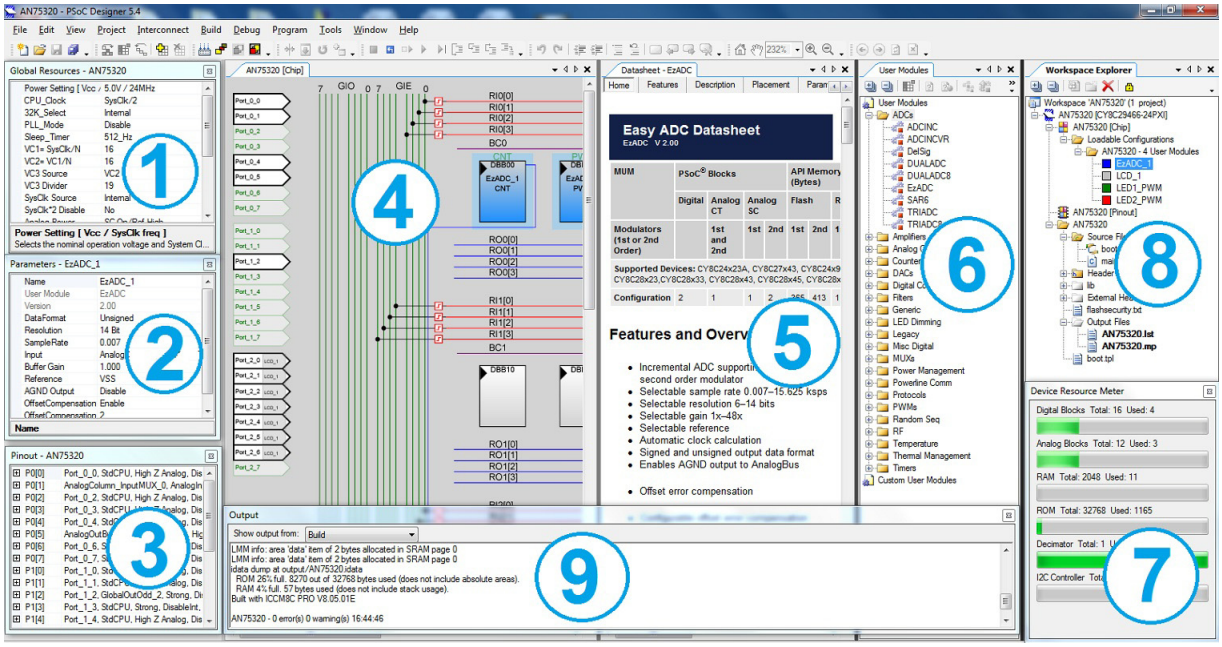
PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



PSoC Functional Overview

The PSoC family consists of many devices with On-Chip Controllers. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog blocks, digital blocks, and interconnections. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. In addition, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The CY8C28xxx group of PSoC devices described in this datasheet have multiple resource configuration options available. Therefore, not every resource mentioned in this datasheet is available for each CY8C28xxx subgroup. The CY8C28x45 subgroup has a full feature set of all resources described. There are six more segmented subgroups that allow designers to use a device with only the resources and functionality necessary for a specific application. See Table 2 on page 9 to determine the resources available for each CY8C28xxx subgroup. The same information is also presented in more detail in the Ordering Information section.

The architecture for this specific PSoC device family, as shown in the Logic Block Diagram on page 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. The configurable global bus system allows all the device resources to be combined into a complete custom system. PSoC CY8C28xxx family devices have up to six I/O ports that connect to the global digital and analog interconnects, providing access to up to 12 digital blocks and up to 16 analog blocks.

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general Purpose I/O (GPIO). The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microcontroller.

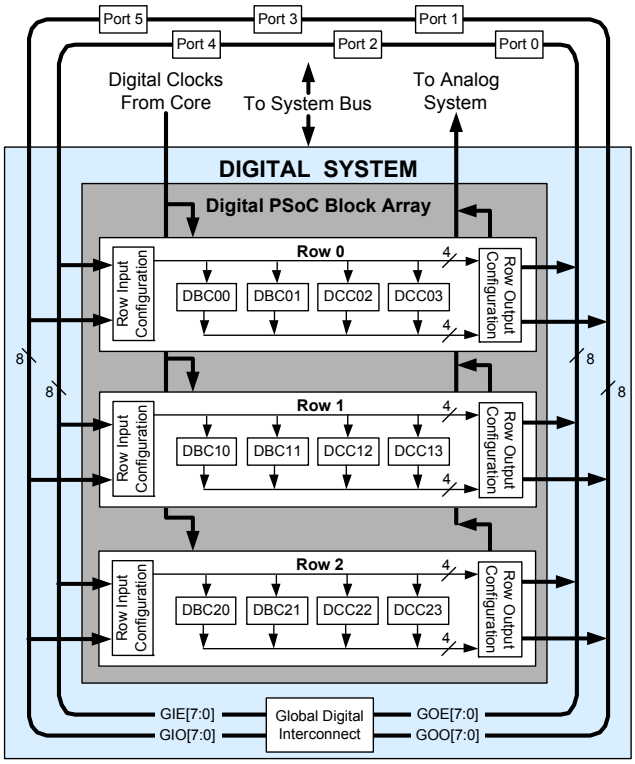
Memory encompasses 16K bytes of Flash for program storage, 1K bytes of SRAM for data storage. The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 2.5% over temperature and voltage. A low power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and watch dog timer (WDT). The 32.768 kHz external crystal oscillator (ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL.

PSoC GPIOs provide connections to the CPU, and digital and analog resources. Each pin's drive mode may be selected from 8 options, which allows great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of up to 12 configurable digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to create 8, 16, 24, and 32-bit peripherals, which are called user modules. The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin.

Figure 2. Digital System Block Diagram[1]



Digital peripheral configurations include:

- PWMs (8- and 16-bit, One-shot and Multi-shot capability)
- PWMs with Dead band/Kill (8- and 16-bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- Full-duplex 8-bit UARTs (up to 3) with selectable parity
- Half-duplex 8-bit UARTs (up to 6) with selectable parity
- Variable length SPI slave and master
  - Up to 6 total slaves and masters (8-bit)
  - Supports 8 to 16 bit operation
- I^2C slave, master, or multi-master (up to 2 available as System Resources)
- IrDA (up to 3)
- Pseudo Random Sequence Generators (8 to 32 bit)
- Cyclical Redundancy Checker/Generator (16 bit)
- Shift Register (2 to 32 bit)

Note
1. CY8C28x52 devices do not have digital block row 2. They have two digital rows with eight total digital blocks.

Pinouts

This section describes, lists, and illustrates the CY8C28xxx PSoC device pins and pinout configurations.

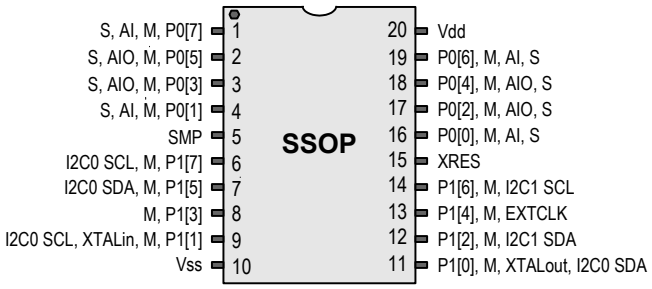
The CY8C28xxx PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

20-pin Part Pinout

Table 3. 20-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
5	Output		SMP	Switch Mode Pump (SMP) connection to external components.
6	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
7	I/O	M	P1[5]	I2C0 Serial Data (SDA).
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
10	Power		V_{SS}	Ground connection.
11	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
12	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
13	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
14	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
15	Input		XRES	Active high external reset with internal pull-down.
16	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
17	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
18	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
19	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
20	Power		V_{DD}	Supply voltage.

CY8C28243 20-pin PSoC Device



LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

Notes
4. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices for details.
5. CY8C28x52 and CY8C28x23 devices do not have a SAR ADC. Therefore, this pin does not function as a SAR ADC input for these devices.
6. CY8C28x13 and CY8C28x03 devices do not have any analog output buffers. Therefore, this pin does not function as an analog column output for these devices.
7. CY8C28x52, CY8C28x13, and CY8C28x33 devices only have one I2C block. Therefore, this GPIO does not function as an I2C pin for these devices.
8. CY8C28x33, CY8C28x23, CY8C28x13, and CY8C28x03 devices do not have an analog output buffer for this pin. Therefore, this pin does not function as an analog column output for these devices.

56-pin Part Pinout

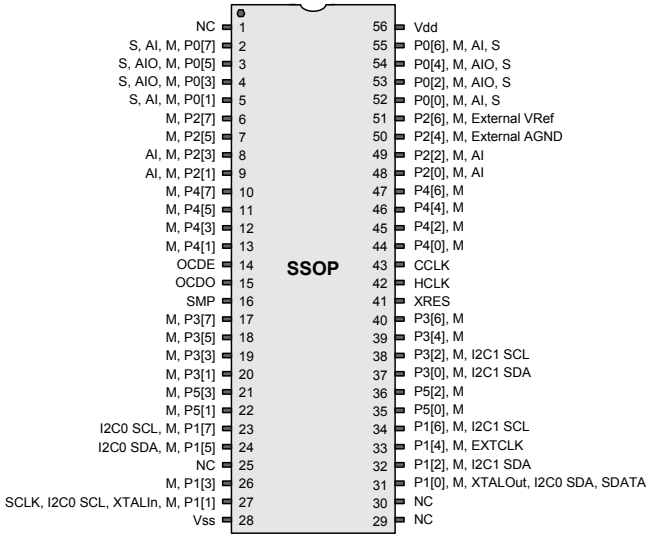
The 56-pin SSOP part is for the CY8C28000 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7. 56-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1			NC	No connection.
2	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.
3	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.
4	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.
5	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.
6	I/O	M	P2[7]	
7	I/O	M	P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input.
9	I/O	I	P2[1]	Direct switched capacitor block input.
10	I/O	M	P4[7]	
11	I/O	M	P4[5]	
12	I/O	I, M	P4[3]	
13	I/O	I, M	P4[1]	
14	OCD	M	OCDE	OCD even data I/O.
15	OCD	M	OCDO	OCD odd data output.
16	Output		SMP	Switch Mode Pump (SMP) connection to required external components.
17	I/O	M	P3[7]	
18	I/O	M	P3[5]	
19	I/O	M	P3[3]	
20	I/O	M	P3[1]	
21	I/O	M	P5[3]	
22	I/O	M	P5[1]	
23	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
24	I/O	M	P1[5]	I2C0 Serial Data (SDA).
25			NC	No connection.
26	I/O	M	P1[3]	
27	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
28	Power		V_{SS}	Ground connection.
29			NC	No connection.
30			NC	No connection.
31	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
32	I/O	M	P1[2]	I2C1 Serial Data (SDA).
33	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
34	I/O	M	P1[6]	I2C1 Serial Clock (SCL).
35	I/O	M	P5[0]	
36	I/O	M	P5[2]	
37	I/O	M	P3[0]	I2C1 Serial Data (SDA).
38	I/O	M	P3[2]	I2C1 Serial Clock (SCL).
39	I/O	M	P3[4]	
40	I/O	M	P3[6]	

CY8C28000 56-pin PSoC Device



Not for Production

Table 8. CY8C28x03 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#		80		RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W		81		RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW		82		RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#		83		RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#		84		RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W		85		RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW		86		RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#		87		RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
PRT4GS	12	RW		52			92			D2	
PRT4DM2	13	RW		53			93		IDX_PP	D3	RW
PRT5DR	14	RW		54			94		MVR_PP	D4	RW
PRT5IE	15	RW		55			95		MVW_PP	D5	RW
PRT5GS	16	RW		56			96		I2C0_CFG	D6	RW
PRT5DM2	17	RW		57			97		I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#		60			A0		INT_MSK0	E0	RW
DBC00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBC00DR2	22	RW		62			A2		INT_VC	E2	RC
DBC00CR0	23	#		63			A3		RES_WDT	E3	W
DBC01DR0	24	#		64			A4		I2C1_SCR	E4	#
DBC01DR1	25	W		65			A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW		66			A6			E6	
DBC01CR0	27	#	I2C1_DR	67	RW		A7			E7	
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RDI0RI	B0	RW		F0	
DBC10DR1	31	W		71		RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR0	33	#		73		RDI0LT0	B3	RW		F3	
DBC11DR0	34	#		74		RDI0LT1	B4	RW		F4	
DBC11DR1	35	W		75		RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR0	37	#		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 17. CY8C28x43 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW		E5	
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW		E6	
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW		E7	
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Absolute Maximum Ratings

Table 22. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See Package label	°C	
$t_{BAKETIME}$	Bake time	See package label	-	72	Hours	
T_A	Ambient temperature with power applied	-40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	-0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	-25	–	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	-50	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 23. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	-40	–	+85	°C	
T_J	Junction temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 72. The user must limit the power consumption to comply with this requirement.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD} – 1.0 V, see the limitations of the total current in the note for V_{OH}.
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25.
V_{IH}	Input high level	2.1	–	–	V	V_{DD} = 3.0 to 5.25.
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Type-E Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of the Limited Type E Analog PSoC blocks.

Table 28. 5 V DC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	For 0.2 V < V_{IN} < V_{DD} – 1.2 V.
		–	2.5	20	mV	For V_{IN} = 0 to 0.2 V and V_{IN} > V_{DD} – 1.2 V.
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}[13]	Input leakage current (Port 0 Analog Pins)	–	200	–	nA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0.0	–	V_{DD}	V	
I_{SOA}	Amplifier supply current	–	10	30	µA	

Table 29. 3.3 V DC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	For 0.2 V < V_{IN} < V_{DD} – 1.2 V.
		–	2.5	20	mV	For V_{IN} = 0 to 0.2 V and V_{IN} > V_{DD} – 1.2 V.
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}[13]	Input leakage current (Port 0 Analog Pins)	–	200	–	nA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0	–	V_{DD}	V	
I_{SOA}	Amplifier supply current	–	10	30	µA	

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 30. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1	V	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	
I_{SLPC}	LPC supply current	–	10	40	µA	

Note
13. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. 5 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	20	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 0.5 × V_{DD} + 1.3 0.5 × V_{DD} + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.0) ≤ V_{OUT} ≤ (0.5 × V_{DD} + 0.9).

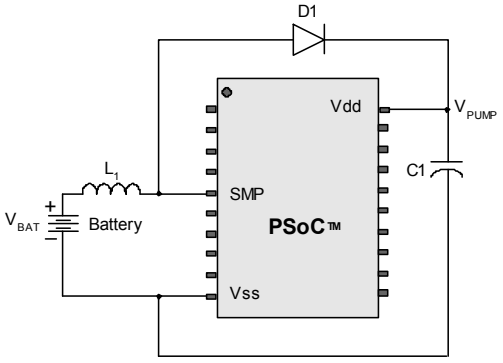
DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 33. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5 V	5 V output voltage	4.75	5.0	5.25	V	Configuration of footnote.[14] Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP} 3 V	3 V output voltage	3.00	3.25	3.60	V	Configuration of footnote.[14] Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
I_{PUMP}	Available output current V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V	 8 5	 – –	 – –	 mA mA	Configuration of footnote.[14] SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 5.0 V.
V_{BAT}5 V	Input voltage range from battery	1.8	–	5.0	V	Configuration of footnote.[14] SMP trip voltage is set to 5.0 V.
V_{BAT}3 V	Input voltage range from battery	1.5	–	3.3	V	Configuration of footnote.[14] SMP trip voltage is set to 3.25 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	2.6	–	–	V	Configuration of footnote.[14]
ΔV_{PUMP_Line}	Line regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configuration of footnote.[14] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 40 on page 52.
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configuration of footnote.[14] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 40 on page 52.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration of footnote.[14] Load is 5mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote.[14] Load is 5 mA. SMP trip voltage is set to 3.25 V.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Figure 9. Basic Switch Mode Pump Circuit



Note
14. L_1 = 2 µH inductor, C_1 = 10 µF capacitor, D_1 = Schottky diode. See Figure 9.

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.218	P2[4] + 1.283	P2[4] + 1.344	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.329	P2[4] – 1.297	P2[4] – 1.265	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.225	P2[4] + 1.287	P2[4] + 1.346	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.330	P2[4] – 1.301	P2[4] – 1.271	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.226	P2[4] + 1.288	P2[4] + 1.346	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.330	P2[4] – 1.302	P2[4] – 1.272	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.227	P2[4] + 1.289	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.303	P2[4] – 1.273	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.597	2.674	V
		V_{AGND}	AGND	Bandgap	1.263	1.302	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.014	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.508	2.595	2.675	V
		V_{AGND}	AGND	Bandgap	1.263	1.302	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.008	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.508	2.595	2.676	V
		V_{AGND}	AGND	Bandgap	1.263	1.302	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.005	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.508	2.596	2.677	V
		V_{AGND}	AGND	Bandgap	1.263	1.302	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.003	V

Table 35. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.226	P2[4] + 1.286	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.323	P2[4] – 1.293	P2[4] –1.262	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.232	P2[4] + 1.29	P2[4] + 1.344	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.296	P2[4] – 1.267	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.233	P2[4] + 1.291	P2[4] + 1.345	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.298	P2[4] – 1.269	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.234	P2[4] + 1.292	P2[4] +1.345	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.299	P2[4] – 1.270	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.504	2.595	2.672	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.013	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.593	2.674	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.008	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	2 × Bandgap	2.506	2.594	2.675	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.007	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	2 × Bandgap	2.507	2.595	2.675	V
		V_{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.005	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

Table 46. 3.3 V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High	 – –	 – –	 3.92 0.72	 µs µs	
t_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 – –	 – –	 5.41 0.72	 µs µs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 0.31 2.7	 – –	 – –	 V/µs V/µs	
SR_{FOA}	Falling Slew Rate (80% to 20%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 0.24 1.8	 – –	 – –	 V/µs V/µs	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 0.67 2.8	 – –	 – –	 MHz MHz	
E_{NOA}	Noise at 1 kHz Power = Medium, Opamp bias = High	 –	 100	 –	 nV/rt-Hz	

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 55. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
t_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
t_{WRITE}	Flash Block Write Time	–	40	–	ms	
t_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	55	ns	$V_{DD} > 3.6$
t_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	75	ns	$3.0 \le V_{DD} \le 3.6$
$t_{ERASEALL}$	Flash Erase Time (Bulk)	–	40	–	ms	Erase all blocks and protection fields at once.
$t_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100[30]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200[30]	ms	–40 °C ≤ Tj ≤ 0 °C

Note
30. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note, AN2015 at http://ww.cypress.com under Application Notes for more information.

Figure 18. 28-pin SSOP (210 Mils) O28.21 Package Outline, 51-85079

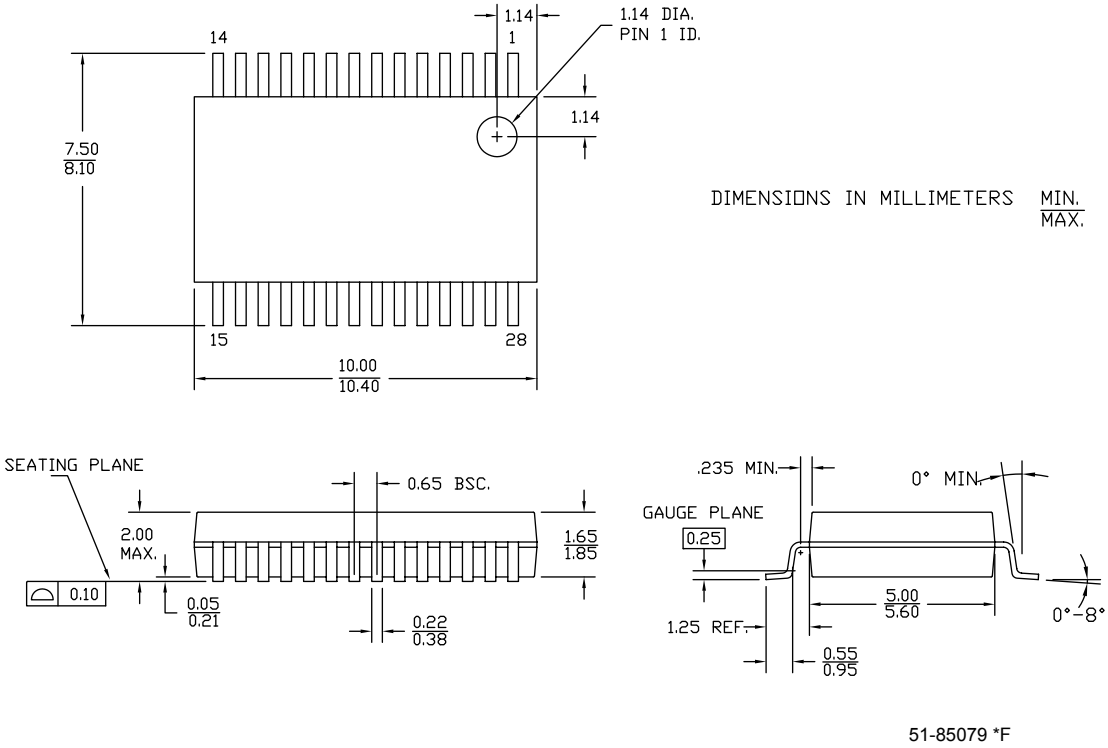
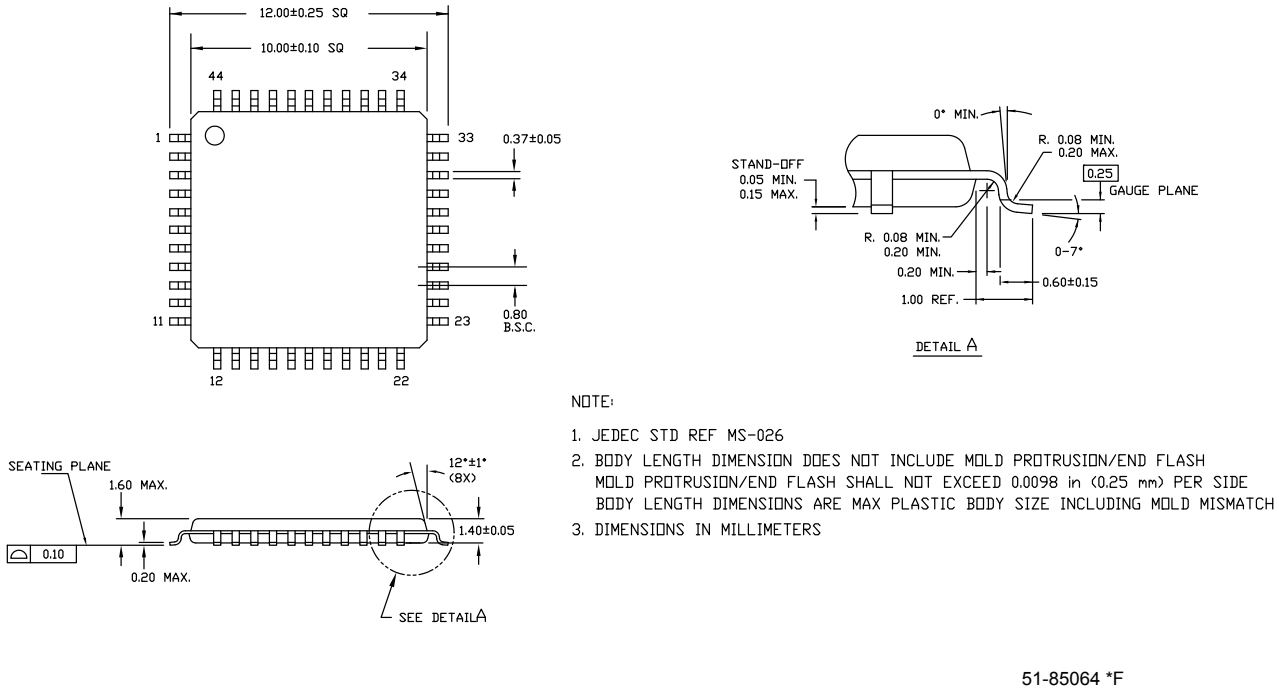


Figure 19. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064



Thermal Impedances

Table 57. Thermal Impedances per Package

Package	Typical θ_{JA} [32]
20-pin SSOP	80.8 °C/W
28-pin SSOP	45.4 °C/W
44-pin TQFP	24.0 °C/W
48-pin QFN[33]	16.7 °C/W
56-pin SSOP	67.5 °C/W

Capacitance on Crystal Pins

Table 58. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
20-pin SSOP	Pin9 = 0.0056 pF Pin11 = 0.006048 pF
28-pin SSOP	Pin13 = 0.006796 pF Pin15 = 0.006755 pF
44-pin TQFP	Pin16 = 0.009428 pF Pin18 = 0.008635 pF
48-pin QFN	Pin17 = 0.008493 pF Pin19 = 0.008742 pF
56-pin SSOP	Pin27 = 0.007916 pF Pin31 = 0.007132 pF

Solder Reflow Specifications

Table 59 shows the solder reflow temperature limits that must not be exceeded.

Table 59. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
20-pin SSOP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
56-pin SSOP	260 °C	30 seconds

Notes
32. $T_J = T_A + POWER \times \theta_{JA}$
33. To achieve the thermal impedance specified for the QFN package, refer to *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com for PCB requirements.
34. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

The following table lists the CY8C28xxx PSoC devices key package features and ordering codes.

Package	Ordering Code	Temperature Range	CapSense	Digital Blocks	Regular Analog Blocks	Limited Analog Blocks	HW I^2C	Decimators	10-bit SAR ADC	Digital I/O Pins	Analog Inputs	Analog Outputs	Flash (KBytes)	RAM (KBytes)	XRES Pin
28-Pin (210-Mil) SSOP	CY8C28403-24PVXI	–40 °C to 85 °C	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28403-24PVXIT	–40 °C to 85 °C	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28413-24PVXI	–40 °C to 85 °C	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28413-24PVXIT	–40 °C to 85 °C	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
44-Pin TQFP	CY8C28513-24AXI	–40 °C to 85 °C	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28513-24AXIT	–40 °C to 85 °C	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
48-Pin Sawn QFN	CY8C28623-24LTXI	–40 °C to 85 °C	N	12	6	0	2	2	N	44	10	2	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28623-24LTXIT	–40 °C to 85 °C	N	12	6	0	2	2	N	44	10	2	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28433-24PVXI	–40 °C to 85 °C	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28433-24PVXIT	–40 °C to 85 °C	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
20-Pin (210-Mil) SSOP	CY8C28243-24PVXI	–40 °C to 85 °C	N	12	12	0	2	4	Y	16	16	4	16	1	Y
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28243-24PVXIT	–40 °C to 85 °C	N	12	12	0	2	4	Y	16	16	4	16	1	Y
48-Pin Sawn QFN	CY8C28643-24LTXI	–40 °C to 85 °C	N	12	12	0	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28643-24LTXIT	–40 °C to 85 °C	N	12	12	0	2	4	Y	44	44	4	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28445-24PVXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28445-24PVXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
44-Pin TQFP	CY8C28545-24AXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28545-24AXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
48-Pin Sawn QFN	CY8C28645-24LTXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28645-24LTXIT	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
28-Pin (210-Mil) SSOP	CY8C28452-24PVXI	–40 °C to 85 °C	Y	8	12	4	1	4	N	24	24	4	16	1	Y
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C28452-24PVXIT	–40 °C to 85 °C	Y	8	12	4	1	4	N	24	24	4	16	1	Y
56-Pin SSOP OCD	CY8C28000-24PVXI	–40 °C to 85 °C	Y	12	12	4	2	4	Y	44	44	4	16	1	Y

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Glossary *(continued)*

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

1. 10-bit SAR ADC does not meet DNL/INL specification.

■ **Problem Definition**

The 10-bit hardware SAR ADC does not meet datasheet accuracy specifications for DNL and INL under some conditions.

■ **Parameters Affected**

INLSAR10: Integral nonlinearity

DNLSAR10: Differential nonlinearity

■ **Trigger Condition(S)**

The SAR ADC DNL has been measured greater than 2 LSB over temperature in all cases, as compared to the datasheet specification of 1.5 LSB.

When using the VPWR (Vdd) reference configuration, the SAR ADC DNL has been measured over temperature at 2 LSB for a supply voltage of 3.3 V. With a supply voltage of 5.5 V, the DNL has been measured greater than 3.5 LSB.

■ **Scope of Impact**

Inaccurate converted data.

■ **Workaround**

- Use an alternate ADC implementation (DelSig, ADCINC) available in CY8C28xxx devices.
- Avoid CPU operations that change the address and data buses while A-D conversion is running with internal Vpwr (Vdd) as Vref.
- Use un-buffered RefHi as ADC Vref. This may have a negative effect on the analog blocks in the analog array due to the noise introduced on RefHi reference.

■ **Fix Status**

Silicon fix is not planned. The workaround mentioned above should be used.

2. Wrong data read from IDAC_CRx and DACx_D registers.

■ **Problem Definition**

The CPU may read an incorrect value of bits 0, 3, 5, or 7 from the following registers:

- IDAC_CR0
- IDAC_CR1
- DAC0_D
- DAC1_D

■ **Parameters Affected**

F_{CPU1} and F_{CPU2} from the device data sheet.

■ **Trigger Condition(S)**

When CPU Clock is set at its highest frequency setting (24 MHz nominal).

■ **Scope of Impact**

Incorrect data read from affected registers.

■ **Workaround**

Temporarily slow down CPU Clock frequency to 12 MHz nominal (or lower) when affected registers are read.