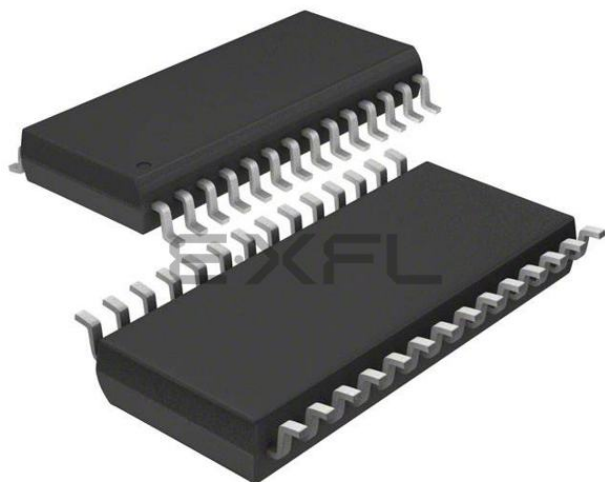




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Details

Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28413-24pvxit

Figure 4. Analog System Block Diagram for CY8C28x43 Devices

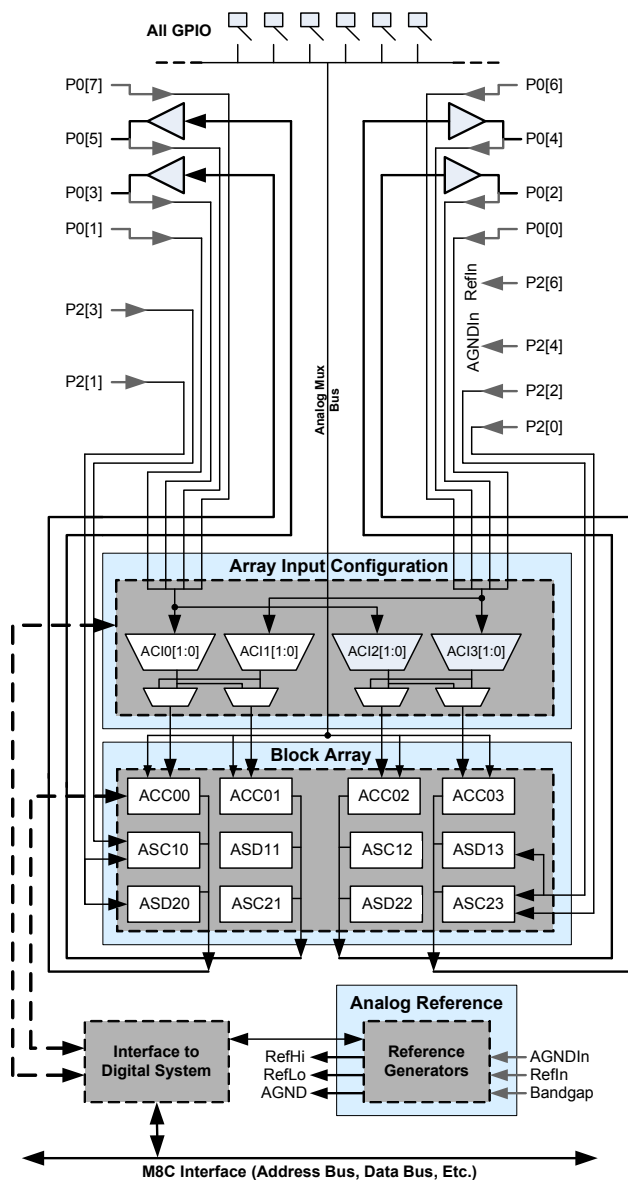
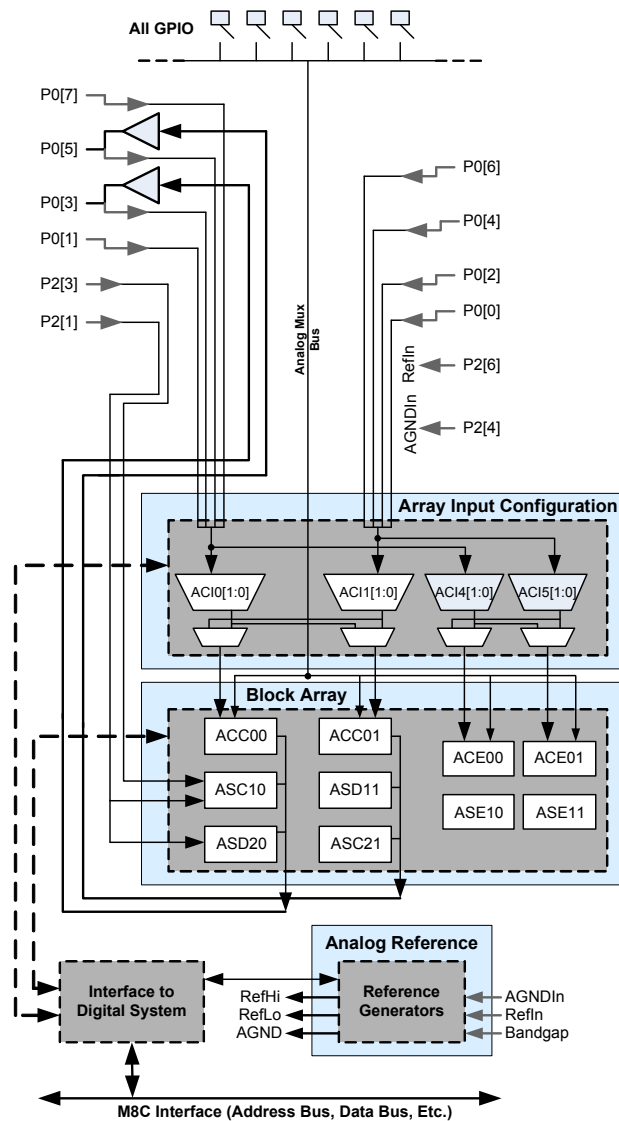


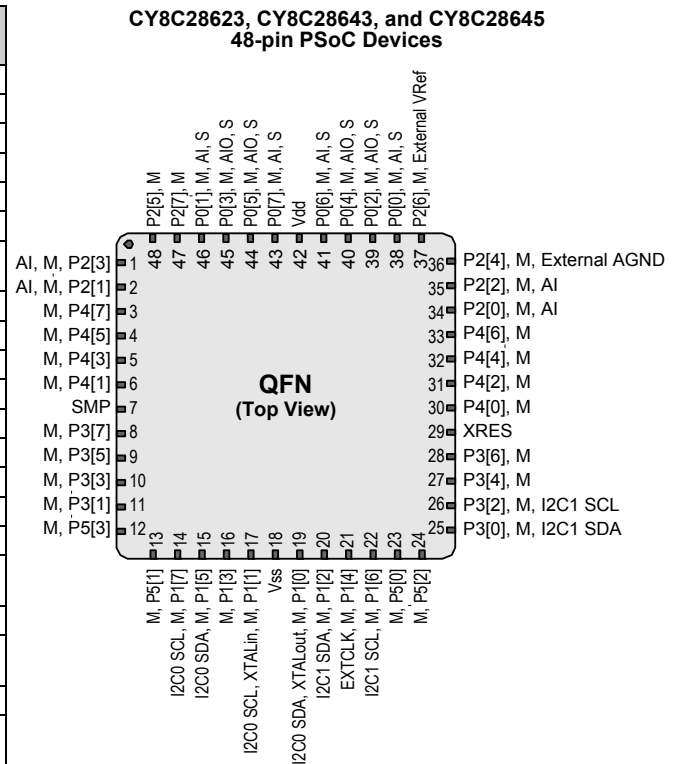
Figure 5. Analog System Block Diagram for CY8C28x33 Devices



48-pin Part Pinout

Table 6. 48-pin Part Pinout (QFN^[11])

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input. ^[9]
2	I/O	I, M	P2[1]	Direct switched capacitor block input. ^[9]
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	Output		SMP	Switch Mode Pump (SMP) connection to external components.
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[3]	
13	I/O	M	P5[1]	
14	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
15	I/O	M	P1[5]	I2C0 Serial Data (SDA).
16	I/O	M	P1[3]	
17	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK ^[4] .
18	Power		V _{SS}	Ground connection.
19	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA ^[4] .
20	I/O	M	P1[2]	I2C1 Serial Data (SDA). ^[1]
21	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
22	I/O	M	P1[6]	I2C1 Serial Clock (SCL). ^[1]
23	I/O	M	P5[0]	
24	I/O	M	P5[2]	
25	I/O	M	P3[0]	I2C1 Serial Data (SDA). ^[1]
26	I/O	M	P3[2]	I2C1 Serial Clock (SCL). ^[1]
27	I/O	M	P3[4]	
28	I/O	M	P3[6]	
29	Input		XRES	Active high external reset with internal pull-down.
30	I/O	M	P4[0]	
31	I/O	M	P4[2]	
32	I/O	M	P4[4]	
33	I/O	M	P4[6]	
34	I/O	I, M	P2[0]	Direct switched capacitor block input. ^[10]
35	I/O	I, M	P2[2]	Direct switched capacitor block input. ^[10]
36	I/O	M	P2[4]	External Analog Ground (AGND).
37	I/O	M	P2[6]	External Voltage Reference (VRef).
38	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input. ^[5]
39	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]
40	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]



Pin No.	Type		Pin Name	Description
	Digital	Analog		
41	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input. ^[5]
42	Power		V _{DD}	Supply voltage.
43	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input. ^[5]
44	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]
45	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]
46	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input. ^[5]
47	I/O	M	P2[7]	
48	I/O	M	P2[5]	

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

Note

11. The QFN package has a center pad that must be connected to ground (V_{SS}).

Register Reference

This section lists the registers of the CY8C28xxx PSoC devices. For detailed register information, reference the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices.

Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

CY8C28xxx PSoC devices have a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank of registers CPU instructions access. When the XIO bit is set the registers in Bank 1 are accessed by CPU instructions. When the XIO bit is cleared the registers in Bank 0 are accessed by CPU instructions.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 11. CY8C28x13 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RD12RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RD12SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RD12IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RD12LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RD12LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RD12RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RD12RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RD12DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C	RW		CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW		60		GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW		61		GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW		62		GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW		63		GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW		64		RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW		66		RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW		67		RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW		69		SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RD10RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RD10SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RD10LT0	B3	RW		F3	
DBC11FN	34	RW		74	RW	RD10LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RD10RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RD10RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RD11RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GL_EN	79	RW	RD11SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RD11IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RD11LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RD11LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RD11RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 13. CY8C28x23 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RD12RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW		81		RD12SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW		82		RD12IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RD12LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RD12LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RD12RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RD12RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RD12DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94	RW	DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A		DEC_CR5	9A	RW		DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW		E5	
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW		E6	
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW		E7	
DCC02FN	28	RW		68			A8		IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCC02OU	2A	RW		6A			AA		BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW		AB		ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RD10RI	B0	RW		F0	
DBC10IN	31	RW		71		RD10SYN	B1	RW		F1	
DBC10OU	32	RW		72		RD10IS	B2	RW		F2	
DBC10CR1	33	RW		73		RD10LT0	B3	RW		F3	
DBC11FN	34	RW		74		RD10LT1	B4	RW		F4	
DBC11IN	35	RW		75		RD10RO0	B5	RW		F5	
DBC11OU	36	RW		76		RD10RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RD10DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RD11RI	B8	RW		F8	
DCC12IN	39	RW		79		RD11SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RD11IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RD11LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RD11LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RD11RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 15. CY8C28x33 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RD12RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RD12SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RD12IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RD12LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RD12LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RD12RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RD12RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RD12DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RD10RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RD10SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RD10LT0	B3	RW		F3	
DBC11FN	34	RW		74		RD10LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RD10RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RD10RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RD11RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RD11SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RD11IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RD11LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RD11LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RD11RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 18. CY8C28x45 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RD12RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RD12SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RD12IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RD12LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RD12LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RD12RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RD12RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RD12DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#	ASC12CR0	88	RW		C8	
PRT2IE	09	RW	DCC22DR1	49	W	ASC12CR1	89	RW		C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW	ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#	ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW	DCC23DR0	4C	#	ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW	DCC23DR1	4D	W	ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW	ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC	I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC	I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW	DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RD11RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RD11IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RD11LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RD11LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RD11RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 21. CY8C28x52 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43		ACE_AMD_CR1	83	RW		C3	
PRT1DM0	04	RW		44			84			C4	
PRT1DM1	05	RW		45		ACE_PWM_CR	85	RW		C5	
PRT1IC0	06	RW		46		ACE_ADC0_CR	86	RW		C6	
PRT1IC1	07	RW		47		ACE_ADC1_CR	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49		ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW		4A		ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW		4B		ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D		ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW		4E		ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW		4F		ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW		AA		BDG_TR	EA	RW
DCC02CR1	2B	RW		6B			AB		ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW		AC		MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RD10RI	B0	RW		F0	
DBC10IN	31	RW		71		RD10SYN	B1	RW		F1	
DBC10OU	32	RW		72		RD10IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RD10LT0	B3	RW		F3	
DBC11FN	34	RW		74		RD10LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RD10RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RD10RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RD11RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RD11SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RD11IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RD11LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RD11LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RD11RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Absolute Maximum Ratings

Table 22. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T _{STG}	Storage temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T _{BAKETEMP}	Bake temperature	–	125	See Package label	°C	
t _{BAKETIME}	Bake time	See package label	–	72	Hours	
T _A	Ambient temperature with power applied	-40	–	+85	°C	
V _{DD}	Supply voltage on V _{DD} relative to V _{SS}	-0.5	–	+6.0	V	
V _{IO}	DC input voltage	V _{SS} – 0.5	–	V _{DD} + 0.5	V	
V _{IOZ}	DC voltage applied to tri-state	V _{SS} – 0.5	–	V _{DD} + 0.5	V	
I _{MIO}	Maximum current into any port pin	-25	–	+50	mA	
I _{MAIO}	Maximum current into any port pin configured as analog driver	-50	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 23. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T _A	Ambient temperature	-40	–	+85	°C	
T _J	Junction temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 72. The user must limit the power consumption to comply with this requirement.

Table 27. 3.3 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOACT}	Input Offset Voltage CT Blocks (absolute value)	—	1.65	8	mV	
	Power = Low, Opamp bias = High	—	1.32	8	mV	
	Power = Medium, Opamp bias = High	—	—	—	mV	
V_{OSOA}	Input Offset Voltage SC and AGND (absolute value)	—	1	6	mV	Applies to High and Low Opamp bias.
TCV_{OSOA}	Average Input Offset Voltage Drift	—	7.0	35.0	$\mu V/^{\circ}C$	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	—	200	—	pA	Gross tested to 1 μA .
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	—	4.5	9.5	pF	Package and pin dependent. Temp = 25 $^{\circ}C$.
V_{CMOA}	Common Mode Voltage Range	0.2	—	$V_{DD} - 0.2$	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common Mode Rejection Ratio	50	—	—	dB	
	Power = Low	50	—	—	dB	
	Power = Medium	50	—	—	dB	
G_{OLOA}	Open Loop Gain	60	—	—	dB	
	Power = Low	60	—	—	dB	
	Power = Medium	80	—	—	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals)	$V_{DD} - 0.2$	—	—	V	
	Power = Low	$V_{DD} - 0.2$	—	—	V	
	Power = Medium	$V_{DD} - 0.2$	—	—	V	
V_{OLOWA}	Low Output Voltage Swing (internal signals)	—	—	0.2	V	
	Power = Low	—	—	0.2	V	
	Power = Medium	—	—	0.2	V	
I_{SOA}	Supply Current (including associated AGND buffer)	—	200	300	μA	
	Power = Low, Opamp bias = Low	—	400	600	μA	
	Power = Low, Opamp bias = High	—	700	1000	μA	
	Power = Medium, Opamp bias = Low	—	1400	2000	μA	
	Power = Medium, Opamp bias = High	—	2400	3600	μA	
	Power = High, Opamp bias = Low	—	4600	7500	μA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	50	80	—	dB	$V_{SS} \leq V_{IN} \leq (V_{DD} - 2.25 V)$ or $(V_{DD} - 1.25 V) \leq V_{IN} \leq V_{DD}$.

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 31. 5 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	20	$\mu\text{V}/^{\circ}\text{C}$	
V_{CMOB}	Common-mode input voltage range	0.5	–	$V_{DD} - 1.0$	V	
R_{OUTOB}	Output resistance Power = Low Power = High	– –	1 1	– –	Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = $32\ \Omega$ to $V_{DD}/2$) Power = Low Power = High	$0.5 \times V_{DD} + 1.3$ $0.5 \times V_{DD} + 1.3$	– –	– –	V V	
V_{LOWOB}	Low output voltage swing (Load = $32\ \Omega$ to $V_{DD}/2$) Power = Low Power = High	– –	– –	$0.5 \times V_{DD} - 1.3$ $0.5 \times V_{DD} - 1.3$	V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	– –	1.1 2.6	5.1 8.8	mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	$(0.5 \times V_{DD} - 1.0) \leq V_{OUT} \leq (0.5 \times V_{DD} + 0.9)$.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

The guaranteed specifications for RefHi and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 34. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.214	V _{DD} /2 + 1.279	V _{DD} /2 + 1.341	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.018	V _{DD} /2 – 0.004	V _{DD} /2 + 0.01	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.328	V _{DD} /2 – 1.301	V _{DD} /2 – 1.273	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 0.228	V _{DD} /2 + 1.284	V _{DD} /2 + 1.344	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.015	V _{DD} /2 – 0.002	V _{DD} /2 + 0.011	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.329	V _{DD} /2 – 1.303	V _{DD} /2 – 1.275	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.224	V _{DD} /2 + 1.287	V _{DD} /2 + 1.345	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.001	V _{DD} /2 + 0.012	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.328	V _{DD} /2 – 1.304	V _{DD} /2 – 1.275	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.226	V _{DD} /2 + 1.288	V _{DD} /2 + 1.346	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.001	V _{DD} /2 + 0.012	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.328	V _{DD} /2 – 1.304	V _{DD} /2 – 1.276	V

Note

15. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 34. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b111	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	3.2 × Bandgap	4.056	4.155	4.222	V
		V _{AGND}	AGND	1.6 × Bandgap	2.012	2.083	2.168	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.01	V _{SS} + 0.035	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	3.2 × Bandgap	4.061	4.153	4.223	V
		V _{AGND}	AGND	1.6 × Bandgap	2.023	2.082	2.145	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.022	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	3.2 × Bandgap	4.063	4.154	4.224	V
		V _{AGND}	AGND	1.6 × Bandgap	2.020	2.083	2.152	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.024	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	3.2 × Bandgap	4.061	4.154	4.225	V
		V _{AGND}	AGND	1.6 × Bandgap	2.026	2.081	2.140	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.017	V

Table 35. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.223	V _{DD} /2 + 1.283	V _{DD} /2 + 1.343	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.013	V _{DD} /2 – 0.003	V _{DD} /2 + 0.005	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.322	V _{DD} /2 – 1.297	V _{DD} /2 – 1.270	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.228	V _{DD} /2 + 1.288	V _{DD} /2 + 1.345	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.008	V _{DD} /2 – 0.002	V _{DD} /2 + 0.005	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.322	V _{DD} /2 – 1.298	V _{DD} /2 – 1.271	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.232	V _{DD} /2 + 1.290	V _{DD} /2 + 1.346	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.008	V _{DD} /2 – 0.001	V _{DD} /2 + 0.006	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.322	V _{DD} /2 – 1.299	V _{DD} /2 – 1.272	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.233	V _{DD} /2 + 1.291	V _{DD} /2 + 1.347	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.006	V _{DD} /2	V _{DD} /2 + 0.006	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.322	V _{DD} /2 – 1.299	V _{DD} /2 – 1.272	V

Table 35. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.045	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.016	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.019	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.023	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.036	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.013	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.021	P2[4] – P2[6] – 0.001	P2[4] – P2[6] + 0.021	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.034	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.013	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.023	P2[4] – P2[6] – 0.002	P2[4] – P2[6] + 0.016	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.033	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.014	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] – 0.003	P2[4] – P2[6] + 0.020	V
0b010	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	V _{DD}	V _{DD} – 0.042	V _{DD} – 0.008	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.035	V _{DD} /2 – 0.001	V _{DD} /2 + 0.031	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.0165	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	V _{DD}	V _{DD} – 0.035	V _{DD} – 0.005	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.031	V _{DD} /2 – 0.001	V _{DD} /2 + 0.028	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.012	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	V _{DD}	V _{DD} – 0.044	V _{DD} – 0.005	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.052	V _{DD} /2	V _{DD} /2 + 0.046	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.014	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	V _{DD}	V _{DD} – 0.036	V _{DD} – 0.004	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.032	V _{DD} /2	V _{DD} /2 + 0.029	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.001	V _{SS} + 0.012	V
0b011	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC I²C Specifications

Table 42 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 42. DC I²C Specifications^[20]

Symbol	Description	Min	Typ	Max	Units	Notes
V _{IL} I ² C	Input low level	–	–	$0.3 \times V_{DD}$	V	$3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$
		–	–	$0.25 \times V_{DD}$	V	$4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$
V _{IH} I ² C	Input high level	$0.7 \times V_{DD}$	–	–	V	$3.0\text{ V} \leq V_{DD} \leq 5.25\text{ V}$
V _{OL} I ² C	Output low level	–	–	0.4	V	at sink current of 3 mA
		–	–	0.6	V	at sink current of 6 mA

Note

20. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the above specs.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 43. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6 ^[21]	MHz	Trimmed. Utilizing factory trim values. SLIMO Mode = 0.
F _{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5 ^[21]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. SLIMO Mode = 1.
F _{CPU1}	CPU Frequency (5 V Nominal)	0.091	24	24.6 ^[21]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F _{CPU2}	CPU Frequency (3.3 V Nominal)	0.091	12	12.3 ^[22]	MHz	Trimmed. Utilizing factory trim values. SLIMO mode = 0.
F _{BLK5}	Digital PSoC Block Frequency	0	–	49.2 ^[21, 23]	MHz	4.75 V < V _{DD} < 5.25 V
F _{BLK33}	Digital PSoC Block Frequency	0	24	24.6 ^[23]	MHz	3.0 V < V _{DD} < 3.6 V
F _{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	Trimmed. Utilizing factory trim values.
F _{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F _{32K_U}	Internal Low Speed Oscillator Untrimmed Frequency	5	–	100	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference manual for details on timing this.
F _{PLL}	PLL Frequency	–	23.986	–	MHz	Multiple (x732) of crystal frequency.
t _{PLLSLEW}	PLL Lock Time	0.5	–	10	ms	
t _{PLLSLEWSLOW}	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T _{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T _{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T _{OSACC} period. Correct operation assumes a properly loaded 1 μ W maximum drive level 32.768 kHz crystal. 3.0 V $\leq$ V _{DD} $\leq$ 5.5 V, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.

Notes

21. 4.75 V < V_{DD} < 5.25 V.

22. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.

23. See the individual user module datasheets for information on maximum frequencies for user modules.

Figure 10. PLL Lock Timing Diagram

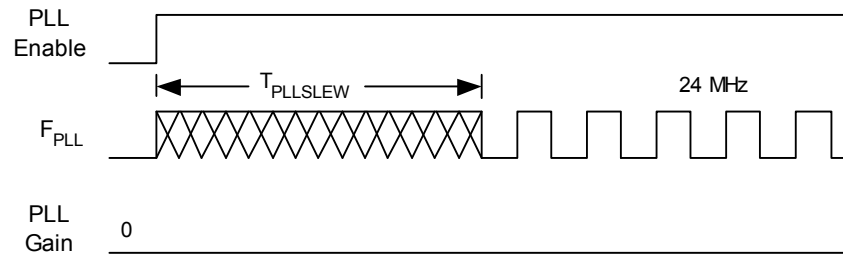


Figure 11. PLL Lock for Low Gain Setting Timing Diagram

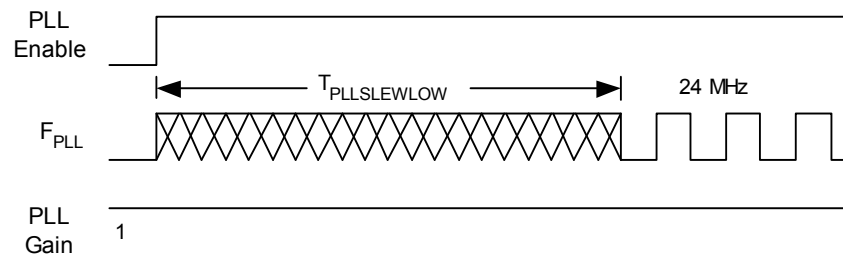
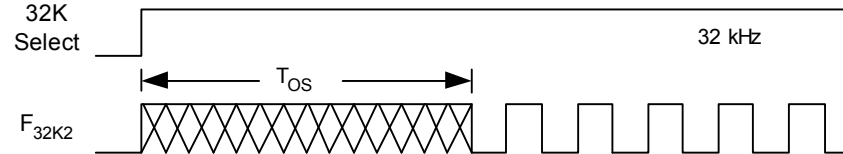


Figure 12. External Crystal Oscillator Startup Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp bias = High is not supported at 3.3 V.

Table 45. 5 V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain)					
	Power = Low, Opamp bias = Low	—	—	3.9	μs	
	Power = Medium, Opamp bias = High	—	—	0.72	μs	
	Power = High, Opamp bias = High	—	—	0.62	μs	
t_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain)					
	Power = Low, Opamp bias = Low	—	—	5.9	μs	
	Power = Medium, Opamp bias = High	—	—	0.92	μs	
	Power = High, Opamp bias = High	—	—	0.72	μs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(Active Probe Loading, Unity Gain)					
	Power = Low, Opamp bias = Low	0.15	—	—	$\text{V}/\mu\text{s}$	
	Power = Medium, Opamp bias = High	1.7	—	—	$\text{V}/\mu\text{s}$	
	Power = High, Opamp bias = High	6.5	—	—	$\text{V}/\mu\text{s}$	
SR_{FOA}	Falling Slew Rate (80% to 20%)(Active Probe Loading, Unity Gain)					
	Power = Low, Opamp bias = Low	0.01	—	—	$\text{V}/\mu\text{s}$	
	Power = Medium, Opamp bias = High	0.5	—	—	$\text{V}/\mu\text{s}$	
	Power = High, Opamp bias = High	4.0	—	—	$\text{V}/\mu\text{s}$	
BW_{OA}	Gain Bandwidth Product					
	Power = Low, Opamp bias = Low	0.75	—	—	MHz	
	Power = Medium, Opamp bias = High	3.1	—	—	MHz	
	Power = High, Opamp bias = High	5.4	—	—	MHz	
E_{NOA}	Noise at 1 kHz	—	100	—	$\text{nV}/\text{rt-Hz}$	
	Power = Medium, Opamp bias = High					

AC Type-E Operational Amplifier Specifications

Table 47 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25°C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of the Limited Type E Analog PSoC blocks.

Table 47. AC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator Mode Response Time	–	75	100	ns	50 mV overdrive.

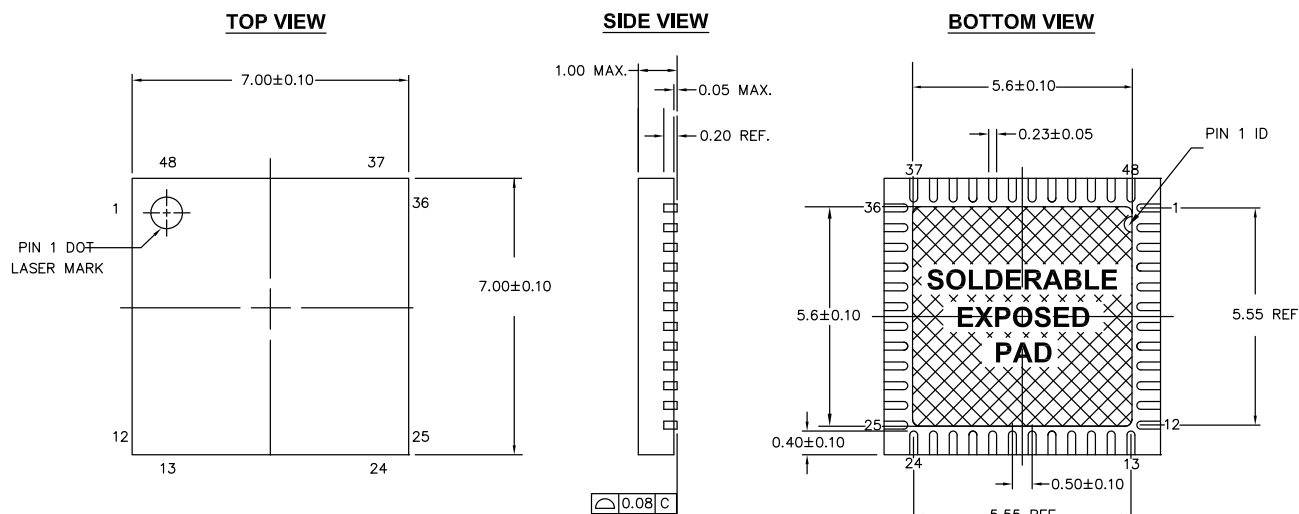
AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V at 25°C and are for design guidance only.

Table 48. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC Response Time	–	–	50	μs	≥ 50 mV overdrive.

Figure 20. 48-pin QFN (7 × 7 × 1.0 mm) LT48D 5.6 × 5.6 E-Pad (Sawn Type) Package Outline, 001-45616



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001-45616 *E

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at <http://www.cypress.com>.