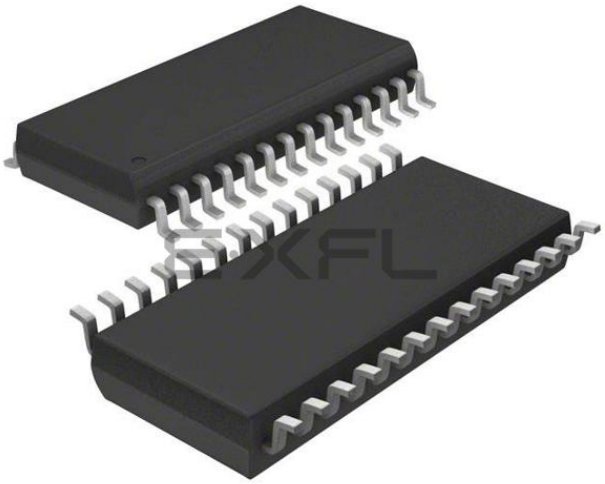

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28433-24pvxit

System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, multiple decimators, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- Up to four decimators provide custom hardware filters for digital signal processing applications such as Delta-Sigma ADCs and CapSense capacitive sensor measurement.
- Up to two I^2C resources provide 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported. I^2C resources have hardware address detection capability.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.5 V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in this table.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[2]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[2]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[2]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[2]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[2]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[2,3]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[2,3]	up to 2 K	up to 32 K

Notes
2. Limited analog functionality.
3. Two analog blocks and one CapSense®.

Pinouts

This section describes, lists, and illustrates the CY8C28xxx PSoC device pins and pinout configurations.

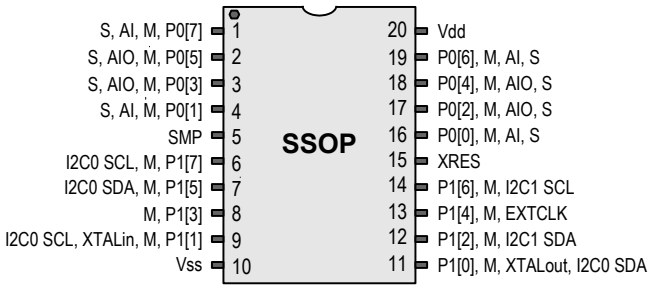
The CY8C28xxx PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

20-pin Part Pinout

Table 3. 20-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
5	Output		SMP	Switch Mode Pump (SMP) connection to external components.
6	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
7	I/O	M	P1[5]	I2C0 Serial Data (SDA).
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
10	Power		V_{SS}	Ground connection.
11	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
12	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
13	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
14	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
15	Input		XRES	Active high external reset with internal pull-down.
16	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
17	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
18	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
19	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
20	Power		V_{DD}	Supply voltage.

CY8C28243 20-pin PSoC Device



LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

Notes
4. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices for details.
5. CY8C28x52 and CY8C28x23 devices do not have a SAR ADC. Therefore, this pin does not function as a SAR ADC input for these devices.
6. CY8C28x13 and CY8C28x03 devices do not have any analog output buffers. Therefore, this pin does not function as an analog column output for these devices.
7. CY8C28x52, CY8C28x13, and CY8C28x33 devices only have one I2C block. Therefore, this GPIO does not function as an I2C pin for these devices.
8. CY8C28x33, CY8C28x23, CY8C28x13, and CY8C28x03 devices do not have an analog output buffer for this pin. Therefore, this pin does not function as an analog column output for these devices.

44-pin Part Pinout

Table 5. 44-pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	M	P2[5]	
2	I/O	I, M	P2[3]	Direct switched capacitor block input.[9]
3	I/O	I, M	P2[1]	Direct switched capacitor block input.[9]
4	I/O	M	P4[7]	
5	I/O	M	P4[5]	
6	I/O	M	P4[3]	
7	I/O	M	P4[1]	
8	Output		SMP	Switch Mode Pump (SMP) connection to external components.
9	I/O	M	P3[7]	
10	I/O	M	P3[5]	
11	I/O	M	P3[3]	
12	I/O	M	P3[1]	
13	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
14	I/O	M	P1[5]	I2C0 Serial Data (SDA).
15	I/O	M	P1[3]	
16	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
17	Power		V_{SS}	Ground connection.
18	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
19	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
20	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
21	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
22	I/O	M	P3[0]	I2C1 Serial Data (SDA).[7]
23	I/O	M	P3[2]	I2C1 Serial Clock (SCL).[7]
24	I/O	M	P3[4]	
25	I/O	M	P3[6]	
26	Input		XRES	Active high external reset with internal pull-down.
27	I/O	M	P4[0]	
28	I/O	M	P4[2]	
29	I/O	M	P4[4]	
30	I/O	M	P4[6]	
31	I/O	I, M	P2[0]	Direct switched capacitor block input.[10]
32	I/O	I, M	P2[2]	Direct switched capacitor block input.[10]
33	I/O	M	P2[4]	External Analog Ground (AGND).
34	I/O	M	P2[6]	External Voltage Reference (VRef).
35	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
36	I/O	I/O, M S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
37	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
38	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
39	Power		V_{DD}	Supply voltage.
40	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
41	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
42	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
43	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
44	I/O		P2[7]	

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

CY8C28513, and CY8C28545
44-pin PSoC Devices

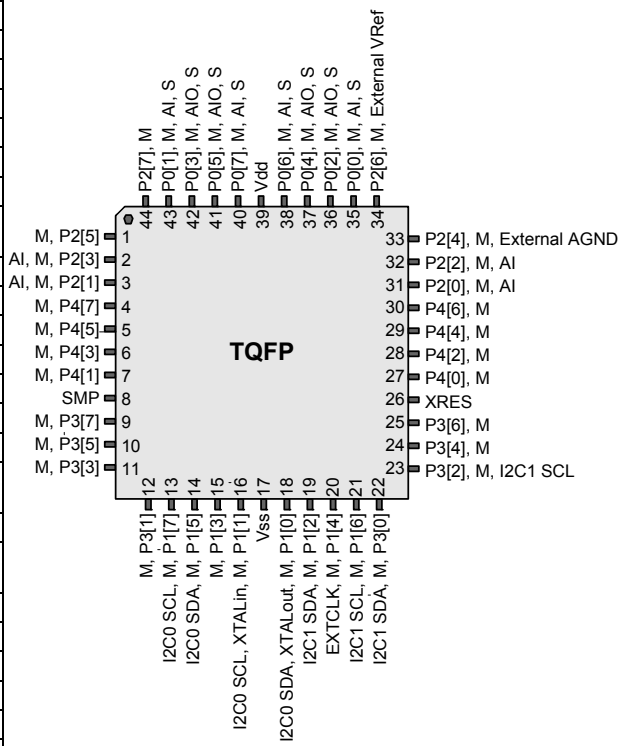


Table 12. CY8C28x23 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4		I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#		A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW		A7		DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 20. CY8C28x52 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Absolute Maximum Ratings

Table 22. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See Package label	°C	
$t_{BAKETIME}$	Bake time	See package label	-	72	Hours	
T_A	Ambient temperature with power applied	-40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	-0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	-25	–	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	-50	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 23. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	-40	–	+85	°C	
T_J	Junction temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 72. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.00	–	5.25	V	
I_{DD}	Supply current	–	8	14	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DD3}	Supply current	–	5	9	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DDP}	Supply current when IMO = 6 MHz using SLIMO mode=1	–	2	3	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT.[12]	–	3	10	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C.
I_{SBH}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT at high temperature.[12]	–	4	25	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, sleep timer, WDT, and external crystal.[12]	–	4	13	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C.
I_{SBXTLH}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and external crystal at high temperature.[12]	–	5	26	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
I_{SBRTC}	Current consumed by RTC during sleep	–	0.5	1	µA	Extra current consumed by the RTC during sleep. This number is typical at 25 °C and 5 V.
V_{REF}	Reference voltage (Bandgap)	1.280	1.300	1.320	V	Trimmed for appropriate V_{DD}.
I_{SXRES}	Supply current with XRES asserted 5 V	–	0.65	3	mA	Max is peak current after XRES; Typical value is the steady state current value. T_A = 25 °C.
	Supply current with XRES asserted 3.3 V	-	0.4	1.5	mA	

Note
12. Standby (sleep) current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. 5 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	20	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 0.5 × V_{DD} + 1.3 0.5 × V_{DD} + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.0) ≤ V_{OUT} ≤ (0.5 × V_{DD} + 0.9).

Table 32. 3.3 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	20	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 – –	 – –	 $0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	47	64	–	dB	$(0.5 \times V_{DD} - 1.0) \le V_{OUT} \le (0.5 \times V_{DD} + 0.9)$.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 34. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.214	$V_{DD}/2$ + 1.279	$V_{DD}/2$ + 1.341	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.018	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.01	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.301	$V_{DD}/2$ – 1.273	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 0.228	$V_{DD}/2$ + 1.284	$V_{DD}/2$ + 1.344	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.015	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.011	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.303	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.287	$V_{DD}/2$ + 1.345	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.276	V

Note
15. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.055	P2[4] + P2[6] – 0.019	P2[4] + P2[6] + 0.019	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.035	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.05	P2[4] + P2[6] – 0.015	P2[4] + P2[6] + 0.021	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.001	P2[4] – P2[6] + 0.031	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.048	P2[4] + P2[6] – 0.013	P2[4] + P2[6] + 0.022	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] – 0.001	P2[4] – P2[6] + 0.031	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.047	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.023	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.036	P2[4] – P2[6] – 0.002	P2[4] – P2[6] + 0.030	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.028	V_{DD} – 0.010	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.002	V_{DD}/2 + 0.012	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.008	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.021	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.001	V_{DD}/2 + 0.012	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.005	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.019	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.001	V_{DD}/2 + 0.012	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.004	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.017	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.014	V_{DD}/2 – 0.001	V_{DD}/2 + 0.013	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.003	V

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b111	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	3.2 × Bandgap	4.056	4.155	4.222	V
		V_{AGND}	AGND	1.6 × Bandgap	2.012	2.083	2.168	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.01	V_{SS} + 0.035	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	3.2 × Bandgap	4.061	4.153	4.223	V
		V_{AGND}	AGND	1.6 × Bandgap	2.023	2.082	2.145	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.022	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	3.2 × Bandgap	4.063	4.154	4.224	V
		V_{AGND}	AGND	1.6 × Bandgap	2.020	2.083	2.152	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	3.2 × Bandgap	4.061	4.154	4.225	V
		V_{AGND}	AGND	1.6 × Bandgap	2.026	2.081	2.140	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V

Table 35. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.223	$V_{DD}/2$ + 1.283	$V_{DD}/2$ + 1.343	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.013	$V_{DD}/2$ – 0.003	$V_{DD}/2$ + 0.005	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.270	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.345	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.008	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.005	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.271	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.232	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.008	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.006	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.272	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.233	$V_{DD}/2$ + 1.291	$V_{DD}/2$ + 1.347	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.006	$V_{DD}/2$	$V_{DD}/2$ + 0.006	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.272	V

Table 35. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.045	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.016	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.019	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.023	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.036	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.013	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.021	P2[4] – P2[6] – 0.001	P2[4] – P2[6] + 0.021	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.034	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.013	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.023	P2[4] – P2[6] – 0.002	P2[4] – P2[6] + 0.016	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.033	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.014	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] – 0.003	P2[4] – P2[6] + 0.020	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.008	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.035	V_{DD}/2 – 0.001	V_{DD}/2 + 0.031	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.0165 V	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.035	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.031	V_{DD}/2 – 0.001	V_{DD}/2 + 0.028	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.012	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.044	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.052	V_{DD}/2	V_{DD}/2 + 0.046	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.014	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.036	V_{DD} – 0.004	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.032	V_{DD}/2	V_{DD}/2 + 0.029	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.012	V
0b011	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC IDAC Specifications

Table 39. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_INL	Integral nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_Gain	Gain per bit – Range 1 (91 µA)	283	357	447	nA	Measured at full scale
	Gain per bit – Range 2 (318 µA)	985	1250	1532	nA	
	Gain per bit – Range 3 (637 µA)	1959	2500	3056	nA	
IDACOffset	Offset at Code 0 vs LSB Ideal – Range 1 (91 µA)		2.0%	20%	%	Measured as a % of LSB (Current @ Code 0)/(LSB Ideal Current)
	Offset at Code 0 vs LSB Ideal – Range 2 (318 µA)		1.0%	10%	%	
	Offset at Code 0 vs LSB Ideal – Range 3 (637 µA)		1.0%	10%	%	

Figure 10. PLL Lock Timing Diagram

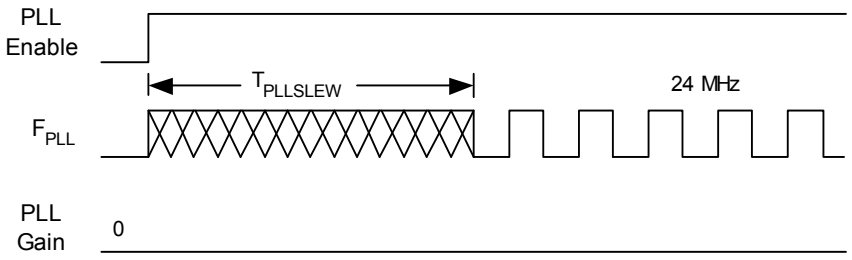


Figure 11. PLL Lock for Low Gain Setting Timing Diagram

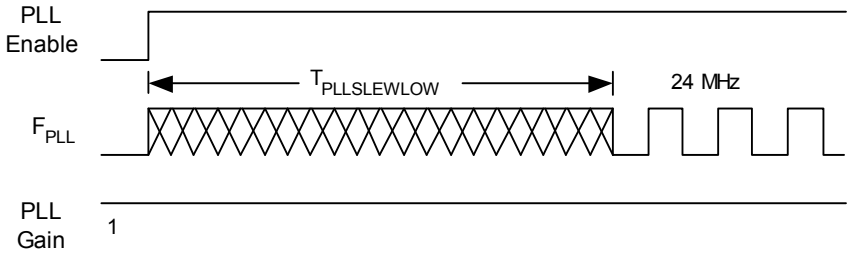
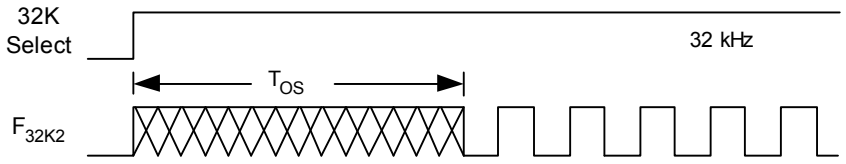


Figure 12. External Crystal Oscillator Startup Timing Diagram



AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 44. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
t_{RiseF}	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% – 90%
t_{FallF}	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% – 90%
t_{RiseS}	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% – 90%
t_{FallS}	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% – 90%

Figure 13. GPIO Timing Diagram

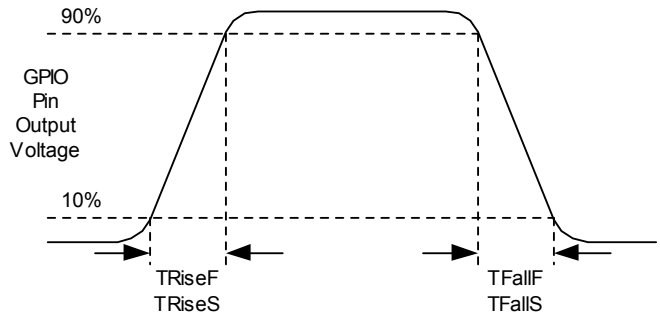
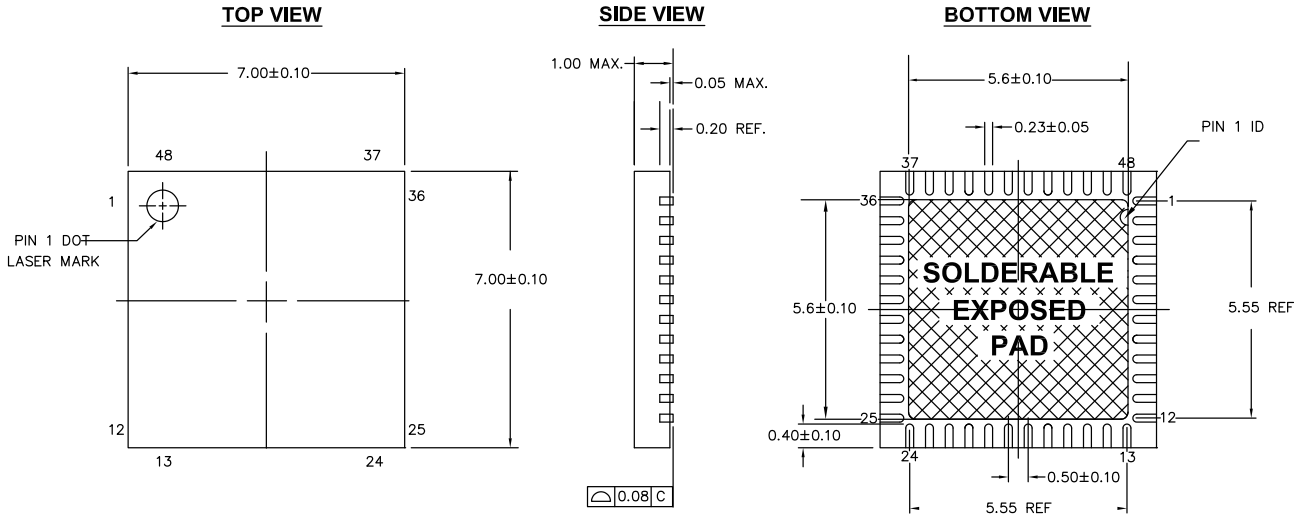


Figure 20. 48-pin QFN (7 × 7 × 1.0 mm) LT48D 5.6 × 5.6 E-Pad (Sawn Type) Package Outline, 001-45616



NOTES:
1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001-45616 *E

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Glossary *(continued)*

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Document History Page *(continued)*

Document Title: CY8C28243/CY8C28403/CY8C28413/CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/ CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™
Document Number: 001-48111

Revision	ECN	Origin of Change	Submission Date	Description of Change
*L	3993399	GVH	05/08/2013	Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata.
*M	4138595	GVH	09/27/2013	Updated to new template. Completing Sunset Review.
*N	4476160	ASRI / SEG	09/04/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added More Information. Added PSoC Designer. Updated PSoC Functional Overview: Updated PSoC Device Characteristics: Updated Table 2: Added a column “Analog Mux Buses” at the end. Removed “Getting Started”. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC I2C Specifications: Updated Table 42: Added V_{OLI2C} parameter and its details. Updated Packaging Information: spec 51-85064 – Changed revision from *E to *F. Completing Sunset Review.
*O	4914758	ASRI	09/10/2015	Updated Document Title to read as “CY8C28243/CY8C28403/CY8C28413/ CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/ CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™”. Removed CY8C28533 related information in all instances across the document. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC SAR10 ADC Specifications: Updated Table 38: Updated details in “Description” column of DNL_{SAR10} parameter. Updated Packaging Information: Updated Packaging Dimensions: spec 51-85077 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. spec 001-45616 – Changed revision from *D to *E. Updated Development Tool Selection: Updated Accessories (Emulation and Programming): Updated Table 60: Updated details in “Part #” column corresponding to 44-pin TQFP package. Updated Ordering Information: Updated part numbers. Updated Errata: Updated Part Numbers Affected: Updated table. Updated Errata Summary: Updated table and also details below the table. Updated to new template. Completing Sunset Review.

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