



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28513-24axi

Figure 4. Analog System Block Diagram for CY8C28x43 Devices

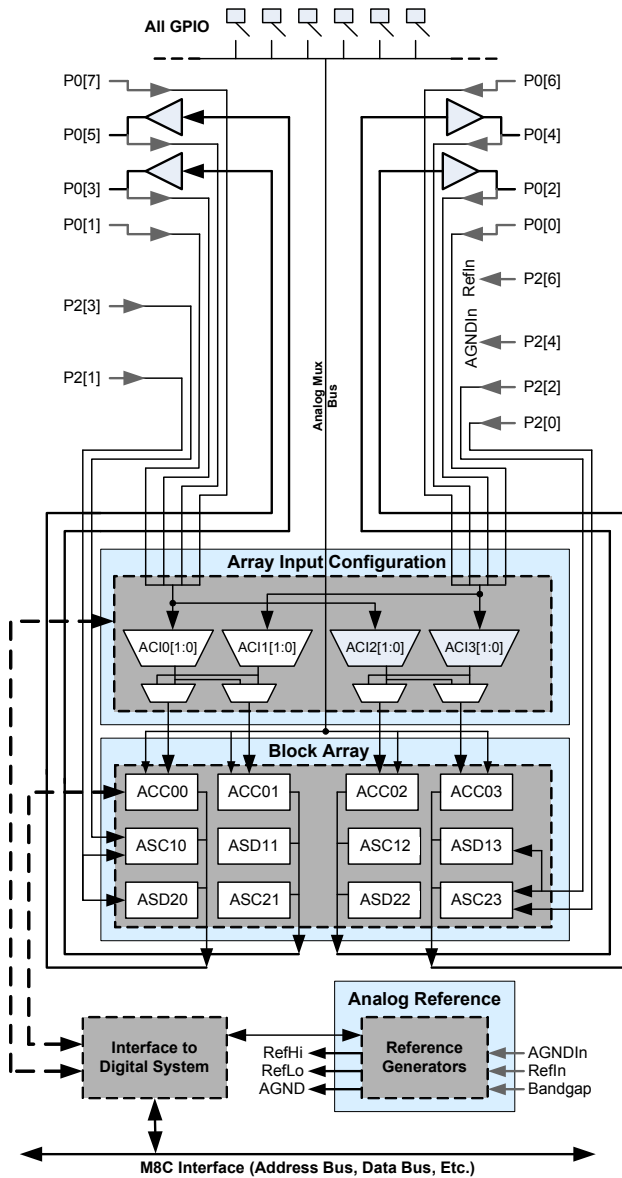


Figure 5. Analog System Block Diagram for CY8C28x33 Devices

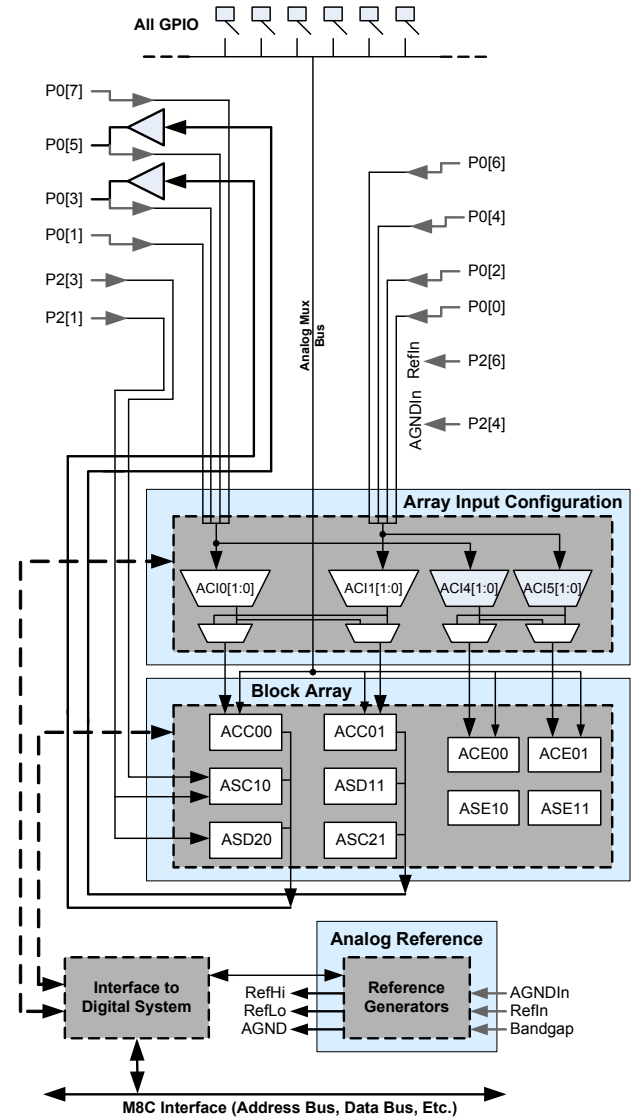


Figure 6. Analog System Block Diagram for CY8C28x23 Devices

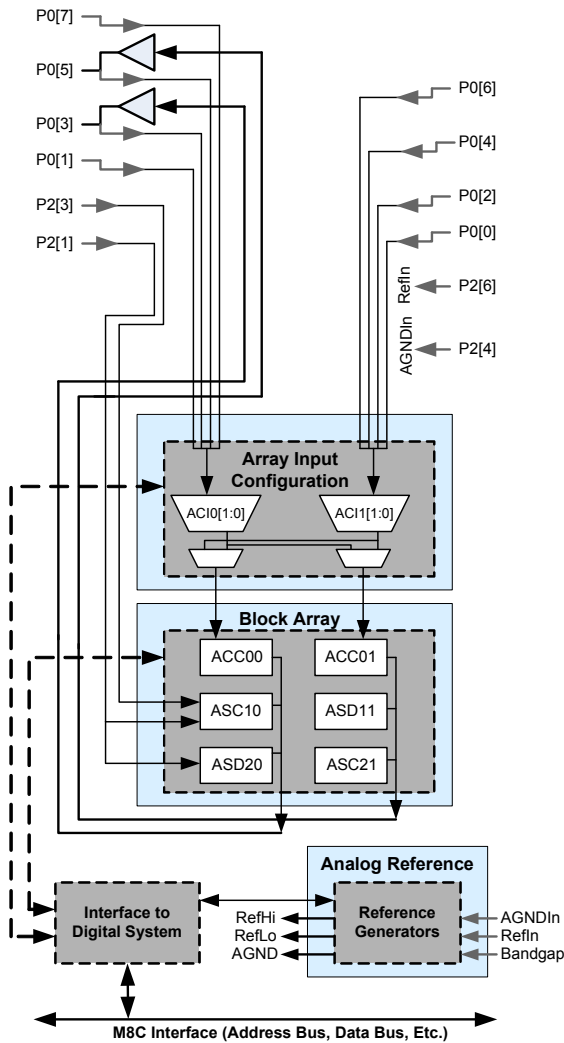
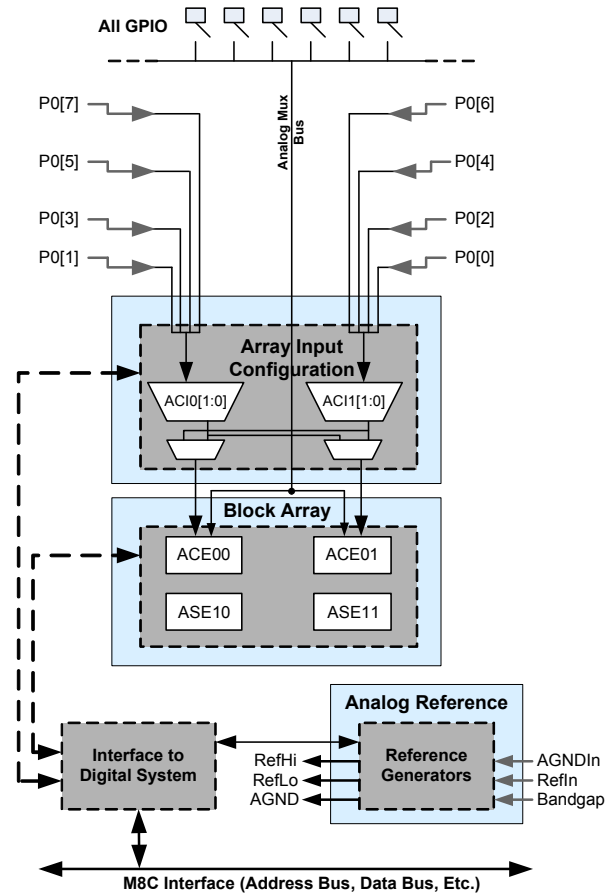


Figure 7. Analog System Block Diagram for CY8C28x13 Devices



Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance

specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

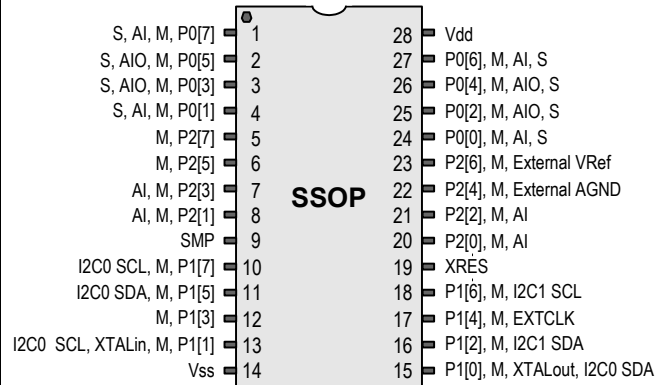
28-pin Part Pinout

Table 4. 28-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input. ^[5]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input. ^[5]
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	I, M	P2[3]	Direct switched capacitor block input. ^[9]
8	I/O	I, M	P2[1]	Direct switched capacitor block input. ^[9]
9	Output		SMP	Switch Mode Pump (SMP) connection to external components.
10	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
11	I/O	M	P1[5]	I2C0 Serial Data (SDA).
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK ^[4] .
14	Power		V _{SS}	Ground connection.
15	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA ^[4] .
16	I/O	M	P1[2]	I2C1 Serial Data (SDA). ^[7]
17	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
18	I/O	M	P1[6]	I2C1 Serial Clock (SCL). ^[7]
19	Input		XRES	Active high external reset with internal pull-down.
20	I/O	I, M	P2[0]	Direct switched capacitor block input. ^[10]
21	I/O	I, M	P2[2]	Direct switched capacitor block input. ^[10]
22	I/O	M	P2[4]	External Analog Ground (AGND).
23	I/O	M	P2[6]	External Voltage Reference (VRef).
24	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input. ^[5]
25	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output. ^[5, 8]
26	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output. ^[5, 8]
27	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input. ^[5]
28	Power		V _{DD}	Supply voltage.

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input

CY8C28403, CY8C28413, CY8C28433, CY8C28445, and CY8C28452 28-pin PSoc Devices



Notes

- This pin is not a direct switched capacitor block analog input for CY8C28x03 and CY8C28x13 devices.
- This pin is not a direct switched capacitor block analog input for CY8C28x03, CY8C28x13, CY8C28x23, and CY8C28x33 devices.

Table 14. CY8C28x33 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RD12RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RD12SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RD12IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RD12LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RD12LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RD12RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RD12RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RD12DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RD11RI	B8	RW		F8	
DCC12DR1	39	W		79		RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RD11IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RD11LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RD11LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D		RD11RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E		RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 15. CY8C28x33 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RD12RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RD12SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RD12IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RD12LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RD12LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RD12RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RD12RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RD12DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RD10RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RD10SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RD10LT0	B3	RW		F3	
DBC11FN	34	RW		74		RD10LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RD10RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RD10RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RD11RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RD11SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RD11IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RD11LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RD11LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RD11RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 18. CY8C28x45 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RD12RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RD12SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RD12IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RD12LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RD12LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RD12RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RD12RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RD12DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#	ASC12CR0	88	RW		C8	
PRT2IE	09	RW	DCC22DR1	49	W	ASC12CR1	89	RW		C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW	ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#	ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW	DCC23DR0	4C	#	ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW	DCC23DR1	4D	W	ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW	ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC	I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC	I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW	DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RD11RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RD11IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RD11LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RD11LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RD11RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

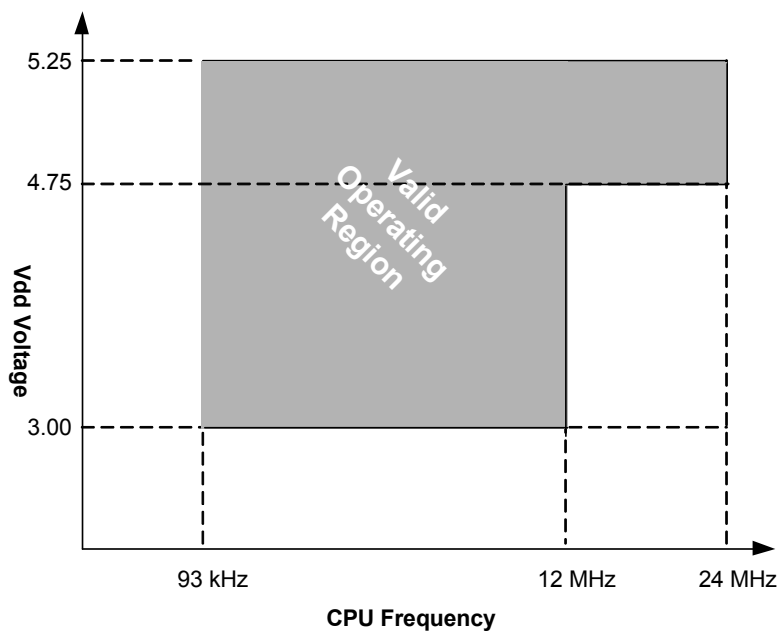
*Address has a dual purpose, see "Mapping Exceptions" on page 251

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C28xxx PSoC devices. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at <http://www.cypress.com>.

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ and $T_J \leq 82^{\circ}\text{C}$.

Figure 8. Voltage versus CPU Frequency



DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 26. 5 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOACT}	Input Offset Voltage CT Block (absolute value) Power = Low, Opamp bias = High Power = Medium, Opamp bias = High Power = High, Opamp bias = High	– – –	1.6 1.3 1.2	8 8 8	mV mV mV	
V_{OSOA}	Input Offset Voltage SC and AGND Opamps (absolute value)	–	1	6	mV	Applies to High and Low Opamp bias.
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	$\mu\text{V}/^{\circ}\text{C}$	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to $1\ \mu\text{A}$.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C .
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high Opamp bias)	0.0 0.5	– –	V_{DD} $V_{\text{DD}} - 0.5$	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
CMRR_{OA}	Common Mode Rejection Ratio Power = Low Power = Medium Power = High	60 60 60	– – –	– – –	dB dB dB	
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	60 60 80	– – –	– – –	dB dB dB	
V_{OHIGHOA}	High Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High	$V_{\text{DD}} - 0.2$ $V_{\text{DD}} - 0.2$ $V_{\text{DD}} - 0.5$	– – –	– – –	V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High	– – –	– – –	0.2 0.2 0.5	V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	– – – – – –	200 400 700 1400 2400 4600	300 600 1100 2000 3600 7700	μA μA μA μA μA μA	
PSRR_{OA}	Supply Voltage Rejection Ratio	60	–	–	dB	$V_{\text{SS}} \leq V_{\text{IN}} \leq (V_{\text{DD}} - 2.25)$ or $(V_{\text{DD}} - 1.25\text{ V}) \leq V_{\text{IN}} \leq V_{\text{DD}}$.

Table 32. 3.3 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	20	$\mu V/^{\circ}C$	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	$V_{DD} - 1.0$	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	– –	1 1	– –	Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1 k Ω to $V_{DD}/2$) Power = Low Power = High	$0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	– –	– –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1 k Ω to $V_{DD}/2$) Power = Low Power = High	– –	– –	$0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	– –	0.8 2.0	2.0 4.3	mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	47	64	–	dB	$(0.5 \times V_{DD} - 1.0) \leq V_{OUT} \leq (0.5 \times V_{DD} + 0.9)$.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

The guaranteed specifications for RefHi and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 34. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.214	V _{DD} /2 + 1.279	V _{DD} /2 + 1.341	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.018	V _{DD} /2 – 0.004	V _{DD} /2 + 0.01	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.328	V _{DD} /2 – 1.301	V _{DD} /2 – 1.273	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 0.228	V _{DD} /2 + 1.284	V _{DD} /2 + 1.344	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.015	V _{DD} /2 – 0.002	V _{DD} /2 + 0.011	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.329	V _{DD} /2 – 1.303	V _{DD} /2 – 1.275	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.224	V _{DD} /2 + 1.287	V _{DD} /2 + 1.345	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.001	V _{DD} /2 + 0.012	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.328	V _{DD} /2 – 1.304	V _{DD} /2 – 1.275	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.226	V _{DD} /2 + 1.288	V _{DD} /2 + 1.346	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.001	V _{DD} /2 + 0.012	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.328	V _{DD} /2 – 1.304	V _{DD} /2 – 1.276	V

Note

15. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 35. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.226	P2[4] + 1.286	P2[4] + 1.343	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.323	P2[4] – 1.293	P2[4] – 1.262	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.232	P2[4] + 1.29	P2[4] + 1.344	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.324	P2[4] – 1.296	P2[4] – 1.267	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.233	P2[4] + 1.291	P2[4] + 1.345	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.324	P2[4] – 1.298	P2[4] – 1.269	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.234	P2[4] + 1.292	P2[4] + 1.345	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.324	P2[4] – 1.299	P2[4] – 1.270	V
0b110	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	2 × Bandgap	2.504	2.595	2.672	V
		V _{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.013	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	2 × Bandgap	2.506	2.593	2.674	V
		V _{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.008	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	2 × Bandgap	2.506	2.594	2.675	V
		V _{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.007	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	2 × Bandgap	2.507	2.595	2.675	V
		V _{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.001	V _{SS} + 0.005	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC IDAC Specifications

Table 39. DC IDAC Specifications

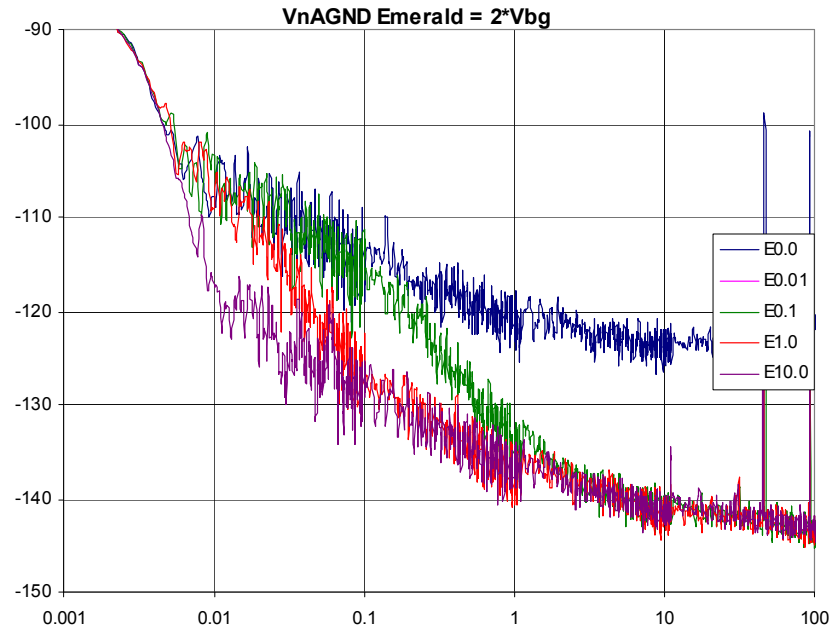
Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_INL	Integral nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_Gain	Gain per bit – Range 1 (91 μ A)	283	357	447	nA	Measured at full scale
	Gain per bit – Range 2 (318 μ A)	985	1250	1532	nA	
	Gain per bit – Range 3 (637 μ A)	1959	2500	3056	nA	
IDACOffset	Offset at Code 0 vs LSB Ideal – Range 1 (91 μ A)		2.0%	20%	%	Measured as a % of LSB (Current @ Code 0)/(LSB Ideal Current)
	Offset at Code 0 vs LSB Ideal – Range 2 (318 μ A)		1.0%	10%	%	
	Offset at Code 0 vs LSB Ideal – Range 3 (637 μ A)		1.0%	10%	%	

Table 46. 3.3 V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High	— —	— —	3.92 0.72	μs μs	
t_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	— —	— —	5.41 0.72	μs μs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	0.31 2.7	— —	— —	$V/\mu s$ $V/\mu s$	
SR_{FOA}	Falling Slew Rate (80% to 20%)(Active Probe Loading, Unity Gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	0.24 1.8	— —	— —	$V/\mu s$ $V/\mu s$	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	0.67 2.8	— —	— —	MHz MHz	
E_{NOA}	Noise at 1 kHz Power = Medium, Opamp bias = High	—	100	—	nV/rt-Hz	

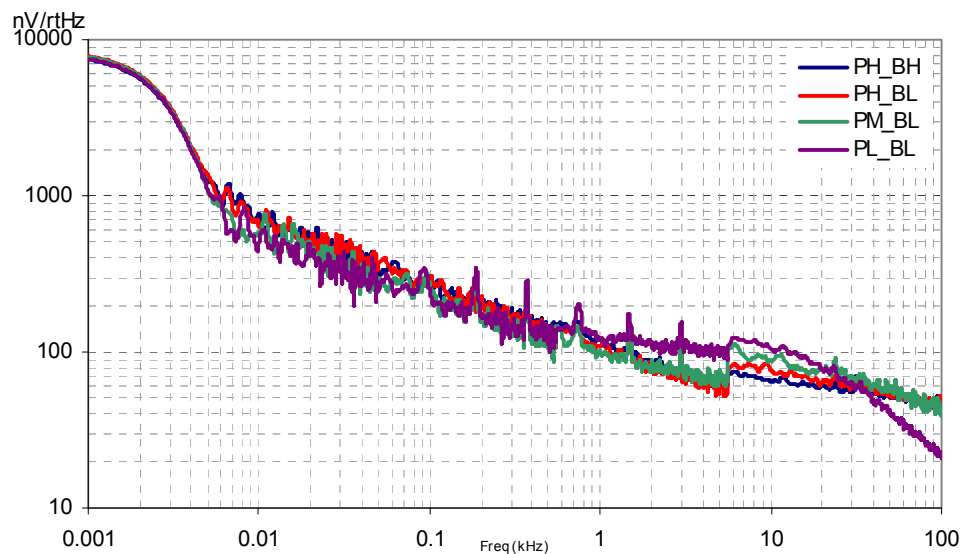
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 14. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to $1/f$, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 15. Typical Opamp Noise



AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 49. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block Input Clock Frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
Timer	Input Clock Frequency					
	No Capture, $V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	No Capture, $V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
	With Capture	–	–	25	MHz	
	Capture Pulse Width	50 ^[27]	–	–	ns	
Counter	Input Clock Frequency					
	No Enable Input, $V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	No Enable Input, $V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
	With Enable Input	–	–	25	MHz	
	Enable Input Pulse Width	50 ^[27]	–	–	ns	
Dead Band	Kill Pulse Width					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50 ^[27]	–	–	ns	
	Disable Mode	50 ^[27]	–	–	ns	
	Input Clock Frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
CRCPRS (PRS Mode)	Input Clock Frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
CRCPRS (CRC Mode)	Input Clock Frequency	–	–	25	MHz	
SPIM	Input Clock Frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated Between Transmissions	50 ^[13]	–	–	ns	
Transmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75\text{ V}$, 2 Stop Bits	–	–	49	MHz	
	$V_{DD} \geq 4.75\text{ V}$, 1 Stop Bit	–	–	25	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75\text{ V}$, 2 Stop Bits	–	–	49	MHz	
	$V_{DD} \geq 4.75\text{ V}$, 1 Stop Bit	–	–	25	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	

Note

27. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC SAR10 ADC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 52. AC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{INSAR10}	Input clock frequency for SAR10 ADC	–	–	2.0	MHz	
F_{SSAR10}	Sample rate for SAR10 ADC SAR10 ADC Resolution = 10 bits	–	–	142.9	ksps	For 10-bit resolution, the sample rate is the ADC's input clock divided by 14.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 53. 5 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power-up IMO to Switch	150	–	–	μs	

Table 54. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1 ^[28]	0.093	–	12.3	MHz	
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater ^[29]	0.186	–	24.6	MHz	
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to Switch	150	–	–	μs	

Notes

28. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
 29. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

Thermal Impedances

Table 57. Thermal Impedances per Package

Package	Typical θ_{JA} ^[32]
20-pin SSOP	80.8 °C/W
28-pin SSOP	45.4 °C/W
44-pin TQFP	24.0 °C/W
48-pin QFN ^[33]	16.7 °C/W
56-pin SSOP	67.5 °C/W

Capacitance on Crystal Pins

Table 58. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
20-pin SSOP	Pin9 = 0.0056 pF Pin11 = 0.006048 pF
28-pin SSOP	Pin13 = 0.006796 pF Pin15 = 0.006755 pF
44-pin TQFP	Pin16 = 0.009428 pF Pin18 = 0.008635 pF
48-pin QFN	Pin17 = 0.008493 pF Pin19 = 0.008742 pF
56-pin SSOP	Pin27 = 0.007916 pF Pin31 = 0.007132 pF

Solder Reflow Specifications

Table 59 shows the solder reflow temperature limits that must not be exceeded.

Table 59. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above $T_C - 5^\circ\text{C}$
20-pin SSOP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
56-pin SSOP	260 °C	30 seconds

Notes

32. $T_J = T_A + \text{POWER} \times \theta_{JA}$

33. To achieve the thermal impedance specified for the QFN package, refer to *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at <http://www.cypress.com> for PCB requirements.

34. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are $220 \pm 5^\circ\text{C}$ with Sn-Pb or $245 \pm 5^\circ\text{C}$ with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Document Conventions

Units of Measure

Table 62 lists the unit sof measures.

Table 62. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	μs	microsecond
dB	decibels	ms	millisecond
°C	degree Celsius	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	μV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohm	V	volts
Ω	ohm	μW	microwatts
μA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
mH	millihenry		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

Glossary

active high	5. A logic signal having its asserted state as the logic 1 state. 6. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary *(continued)*

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V _{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V _{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.