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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28513-24axit

System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, multiple decimators, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- Up to four decimators provide custom hardware filters for digital signal processing applications such as Delta-Sigma ADCs and CapSense capacitive sensor measurement.
- Up to two I^2C resources provide 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported. I^2C resources have hardware address detection capability.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.5 V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in this table.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[2]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[2]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[2]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[2]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[2]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[2,3]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[2,3]	up to 2 K	up to 32 K

Notes
2. Limited analog functionality.
3. Two analog blocks and one CapSense®.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

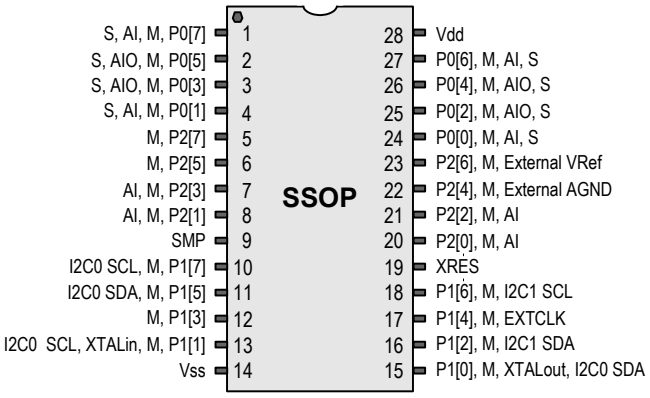
The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

28-pin Part Pinout

Table 4. 28-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	I, M	P2[3]	Direct switched capacitor block input.[9]
8	I/O	I, M	P2[1]	Direct switched capacitor block input.[9]
9	Output		SMP	Switch Mode Pump (SMP) connection to external components.
10	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
11	I/O	M	P1[5]	I2C0 Serial Data (SDA).
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
14	Power		V_{SS}	Ground connection.
15	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
16	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
17	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
18	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
19	Input		XRES	Active high external reset with internal pull-down.
20	I/O	I, M	P2[0]	Direct switched capacitor block input.[10]
21	I/O	I, M	P2[2]	Direct switched capacitor block input.[10]
22	I/O	M	P2[4]	External Analog Ground (AGND).
23	I/O	M	P2[6]	External Voltage Reference (VRef).
24	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
25	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
26	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
27	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
28	Power		V_{DD}	Supply voltage.

CY8C28403, CY8C28413, CY8C28433, CY8C28445, and CY8C28452 28-pin PSoC Devices



LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input

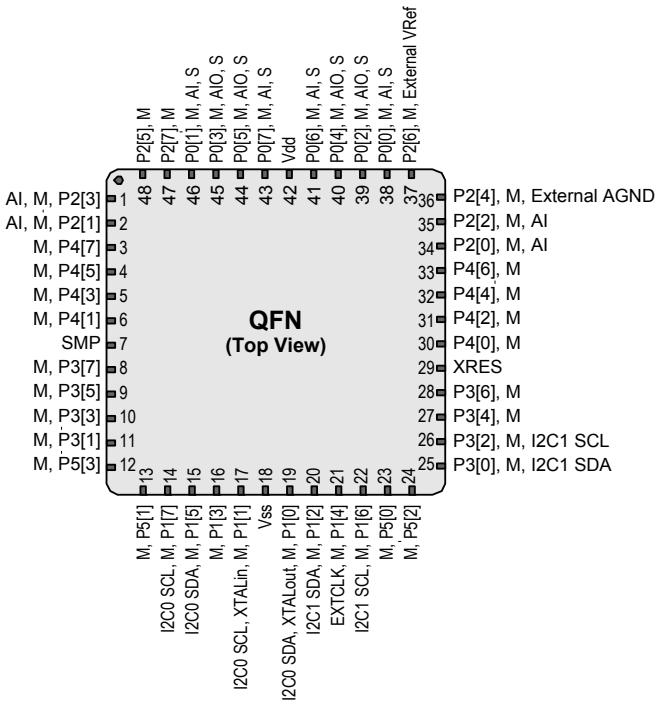
Notes
9. This pin is not a direct switched capacitor block analog input for CY8C28x03 and CY8C28x13 devices.
10. This pin is not a direct switched capacitor block analog input for CY8C28x03, CY8C28x13, CY8C28x23, and CY8C28x33 devices.

48-pin Part Pinout

Table 6. 48-pin Part Pinout (QFN[11])

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input.[9]
2	I/O	I, M	P2[1]	Direct switched capacitor block input.[9]
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	Output		SMP	Switch Mode Pump (SMP) connection to external components.
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[3]	
13	I/O	M	P5[1]	
14	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
15	I/O	M	P1[5]	I2C0 Serial Data (SDA).
16	I/O	M	P1[3]	
17	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
18	Power		V_{SS}	Ground connection.
19	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
20	I/O	M	P1[2]	I2C1 Serial Data (SDA).[7]
21	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
22	I/O	M	P1[6]	I2C1 Serial Clock (SCL).[7]
23	I/O	M	P5[0]	
24	I/O	M	P5[2]	
25	I/O	M	P3[0]	I2C1 Serial Data (SDA).[7]
26	I/O	M	P3[2]	I2C1 Serial Clock (SCL).[7]
27	I/O	M	P3[4]	
28	I/O	M	P3[6]	
29	Input		XRES	Active high external reset with internal pull-down.
30	I/O	M	P4[0]	
31	I/O	M	P4[2]	
32	I/O	M	P4[4]	
33	I/O	M	P4[6]	
34	I/O	I, M	P2[0]	Direct switched capacitor block input.[10]
35	I/O	I, M	P2[2]	Direct switched capacitor block input.[10]
36	I/O	M	P2[4]	External Analog Ground (AGND).
37	I/O	M	P2[6]	External Voltage Reference (VRef).
38	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.[5]
39	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.[5, 8]
40	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.[5, 8]

CY8C28623, CY8C28643, and CY8C28645
48-pin PSoC Devices



Pin No.	Type		Pin Name	Description
	Digital	Analog		
41	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.[5]
42	Power		V_{DD}	Supply voltage.
43	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.[5]
44	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
45	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.[5, 6]
46	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.[5]
47	I/O	M	P2[7]	
48	I/O	M	P2[5]	

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

Note
11. The QFN package has a center pad that must be connected to ground (V_{SS})

56-pin Part Pinout

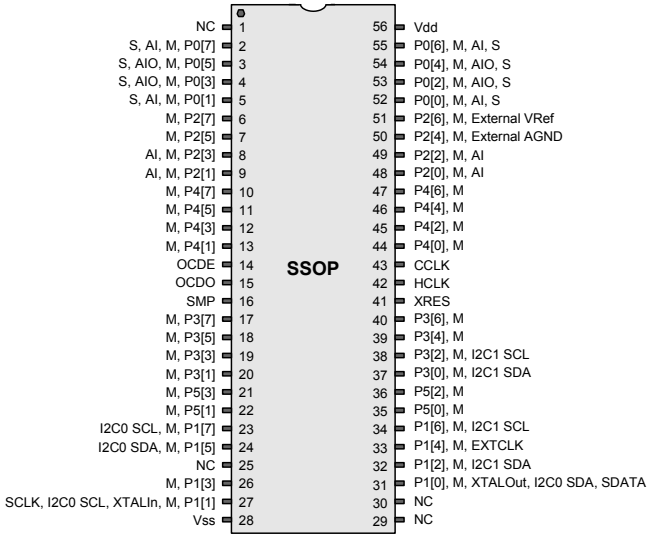
The 56-pin SSOP part is for the CY8C28000 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7. 56-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1			NC	No connection.
2	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.
3	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.
4	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.
5	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.
6	I/O	M	P2[7]	
7	I/O	M	P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input.
9	I/O	I	P2[1]	Direct switched capacitor block input.
10	I/O	M	P4[7]	
11	I/O	M	P4[5]	
12	I/O	I, M	P4[3]	
13	I/O	I, M	P4[1]	
14	OCD	M	OCDE	OCD even data I/O.
15	OCD	M	OCDO	OCD odd data output.
16	Output		SMP	Switch Mode Pump (SMP) connection to required external components.
17	I/O	M	P3[7]	
18	I/O	M	P3[5]	
19	I/O	M	P3[3]	
20	I/O	M	P3[1]	
21	I/O	M	P5[3]	
22	I/O	M	P5[1]	
23	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
24	I/O	M	P1[5]	I2C0 Serial Data (SDA).
25			NC	No connection.
26	I/O	M	P1[3]	
27	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK[4].
28	Power		V_{SS}	Ground connection.
29			NC	No connection.
30			NC	No connection.
31	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA[4].
32	I/O	M	P1[2]	I2C1 Serial Data (SDA).
33	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
34	I/O	M	P1[6]	I2C1 Serial Clock (SCL).
35	I/O	M	P5[0]	
36	I/O	M	P5[2]	
37	I/O	M	P3[0]	I2C1 Serial Data (SDA).
38	I/O	M	P3[2]	I2C1 Serial Clock (SCL).
39	I/O	M	P3[4]	
40	I/O	M	P3[6]	

CY8C28000 56-pin PSoC Device



Not for Production

Table 10. CY8C28x13 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#		80		RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W		81		RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW		82		RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#		83		RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#		84		RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W		85		RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW		86		RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#		87		RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
PRT4GS	12	RW		52			92			D2	
PRT4DM2	13	RW		53			93		IDX_PP	D3	RW
PRT5DR	14	RW		54			94		MVR_PP	D4	RW
PRT5IE	15	RW		55			95		MVW_PP	D5	RW
PRT5GS	16	RW		56			96		I2C0_CFG	D6	RW
PRT5DM2	17	RW		57			97		I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#		60		DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW		62		DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#		63		DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#		64			A4			E4	
DBC01DR1	25	W		65			A5			E5	
DBC01DR2	26	RW		66			A6		DEC_CR0*	E6	RW
DBC01CR0	27	#		67			A7		DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RDI0RI	B0	RW		F0	
DBC10DR1	31	W		71		RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR0	33	#		73		RDI0LT0	B3	RW		F3	
DBC11DR0	34	#		74		RDI0LT1	B4	RW		F4	
DBC11DR1	35	W		75		RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR0	37	#		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 26. 5 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOACT}	Input Offset Voltage CT Block (absolute value) Power = Low, Opamp bias = High Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 1.6 1.3 1.2	 8 8 8	 mV mV mV	
V_{OSOA}	Input Offset Voltage SC and AGND Opamps (absolute value)	–	1	6	mV	Applies to High and Low Opamp bias.
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high Opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common Mode Rejection Ratio Power = Low Power = Medium Power = High	 60 60 60	 – – –	 – – –	 dB dB dB	
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	 60 60 80	 – – –	 – – –	 dB dB dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low Power = Medium Power = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 200 400 700 1400 2400 4600	 300 600 1100 2000 3600 7700	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	60	–	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. 5 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	20	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 0.5 × V_{DD} + 1.3 0.5 × V_{DD} + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.0) ≤ V_{OUT} ≤ (0.5 × V_{DD} + 0.9).

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 34. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.214	$V_{DD}/2$ + 1.279	$V_{DD}/2$ + 1.341	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.018	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.01	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.301	$V_{DD}/2$ – 1.273	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 0.228	$V_{DD}/2$ + 1.284	$V_{DD}/2$ + 1.344	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.015	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.011	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.303	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.287	$V_{DD}/2$ + 1.345	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.276	V

Note
15. AGND tolerance includes the offsets of the local buffer in the PSoC block.

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 36. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.24	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 37. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	400	Ω	V_{DD} ≥ 3.0 V
R_{VSS}	Resistance of Initialization Switch to V_{SS}	–	–	800	Ω	

DC SAR10 ADC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 38. DC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
INL_{SAR10}	Integral nonlinearity for VREF ≥ 3 V	–2.5	–	2.5	LSB	10-bit resolution
	Integral nonlinearity for VREF < 3 V	–5	–	5	LSB	10-bit resolution
DNL_{SAR10}	Differential nonlinearity for VREF ≥ 3 V	–1.5	–	1.5	LSB	10-bit resolution
	Differential nonlinearity for VREF < 3 V	–4	–	4	LSB	10-bit resolution
I_{SAR10}	Active current consumption	0.08	0.5	0.497	mA	
$I_{VREFSAR10}$	Input current into P2[5] when configured as the SAR10 ADC's VREF input.	–	–	0.5	mA	The internal voltage reference buffer is disabled in this configuration.
$V_{VREFSAR10}$	Input reference voltage at P2[5] when configured as the SAR10 ADC's external voltage reference.	2.7	–	V_{DD} – 0.3 V	V	When VREF is buffered inside the SAR10 ADC, the voltage level at P2[5] (when configured as the external reference voltage) must always be at least 300 mV less than the chip supply voltage level on the V_{DD} pin. ($V_{VREFSAR10}$ < (V_{DD} – 300 mV)).
$V_{OSSAR10}$	Offset voltage	5	7.7	10	mV	
SAR_{IMP}	SAR input impedence	–	1.64	–	MΩ	Frequency dependant = 1/ Fs °C. 142.9 kHz (maximum) and Cin = 4.28 pF (typical)

DC IDAC Specifications

Table 39. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_INL	Integral nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_Gain	Gain per bit – Range 1 (91 µA)	283	357	447	nA	Measured at full scale
	Gain per bit – Range 2 (318 µA)	985	1250	1532	nA	
	Gain per bit – Range 3 (637 µA)	1959	2500	3056	nA	
IDACOffset	Offset at Code 0 vs LSB Ideal – Range 1 (91 µA)		2.0%	20%	%	Measured as a % of LSB (Current @ Code 0)/(LSB Ideal Current)
	Offset at Code 0 vs LSB Ideal – Range 2 (318 µA)		1.0%	10%	%	
	Offset at Code 0 vs LSB Ideal – Range 3 (637 µA)		1.0%	10%	%	

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 41. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	3	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply Voltage for Flash write operation	3	–	5.25	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.21	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000[18]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[19]	1,800,000	–	–	–	Erase/write cycles. Must be programmed and read at the same voltage to meet this.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Notes

18. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
19. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Type-E Operational Amplifier Specifications

Table 47 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of the Limited Type E Analog PSoC blocks.

Table 47. AC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator Mode Response Time	–	75	100	ns	50 mV overdrive.

AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 48. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC Response Time	–	–	50	µs	≥ 50 mV overdrive.

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 50. 5 V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	2.5	µs	
	Power = High	–	–	2.9	µs	
t_{SOB}	Falling Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	2.3	µs	
	Power = High	–	–	2.3	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1 V Step, 100 pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1 V Step, 100 pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	0.8	–	–	MHz	
	Power = High	0.8	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1 V$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	300	–	–	kHz	
	Power = High	300	–	–	kHz	

Table 51. 3.3 V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	3.8	µs	
	Power = High	–	–	3.8	µs	
t_{SOB}	Falling Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	3.2	µs	
	Power = High	–	–	2.9	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1 V Step, 100 pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1 V Step, 100 pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	0.64	–	–	MHz	
	Power = High	0.64	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1 V$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	200	–	–	kHz	
	Power = High	200	–	–	kHz	

AC SAR10 ADC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 52. AC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{INSAR10}$	Input clock frequency for SAR10 ADC	–	–	2.0	MHz	
F_{SSAR10}	Sample rate for SAR10 ADC SAR10 ADC Resolution = 10 bits	–	–	142.9	ksps	For 10-bit resolution, the sample rate is the ADC's input clock divided by 14.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 53. 5 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power-up IMO to Switch	150	–	–	µs	

Table 54. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1[28]	0.093	–	12.3	MHz	
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[29]	0.186	–	24.6	MHz	
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to Switch	150	–	–	µs	

Notes
28. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
29. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 55. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
t_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
t_{WRITE}	Flash Block Write Time	–	40	–	ms	
t_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	55	ns	$V_{DD} > 3.6$
t_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	75	ns	$3.0 \le V_{DD} \le 3.6$
$t_{ERASEALL}$	Flash Erase Time (Bulk)	–	40	–	ms	Erase all blocks and protection fields at once.
$t_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100[30]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200[30]	ms	–40 °C ≤ Tj ≤ 0 °C

Note
30. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note, AN2015 at http://ww.cypress.com under Application Notes for more information.

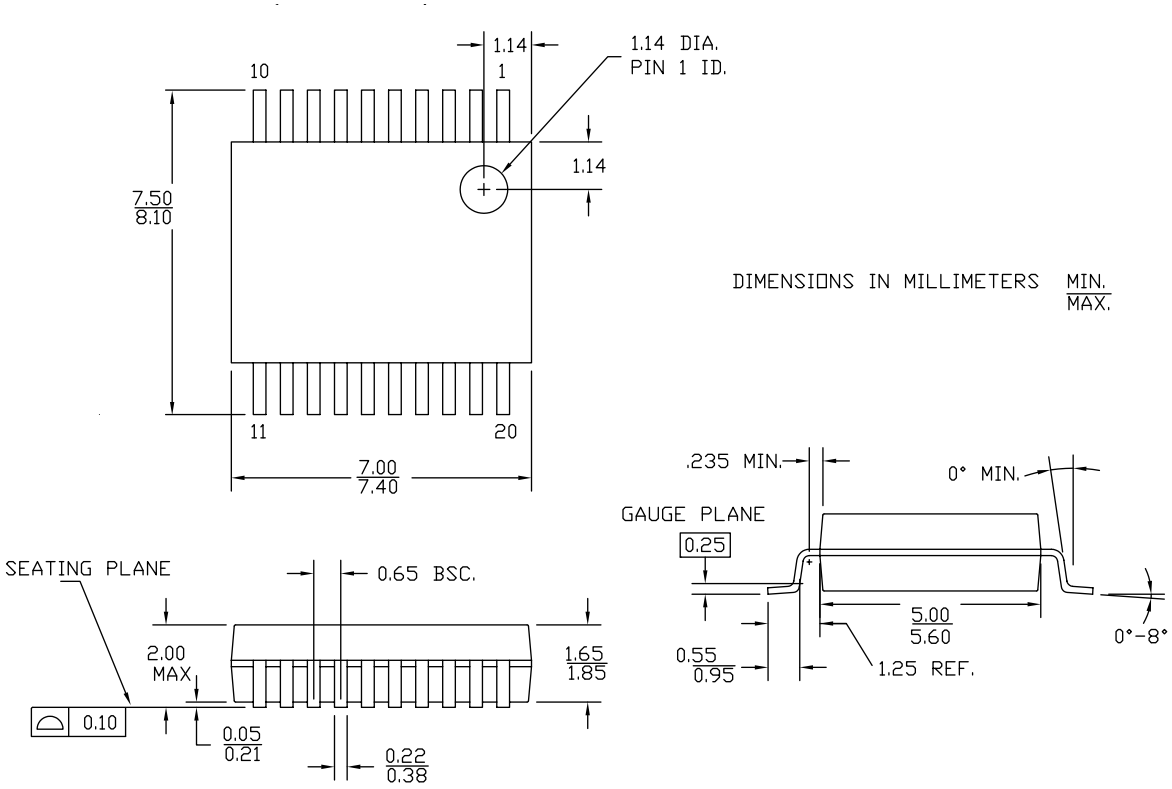
Packaging Information

This section illustrates the packaging specifications for the CY8C28xxx PSoC devices, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the Emulator Pod Dimension drawings at http://www.cypress.com.

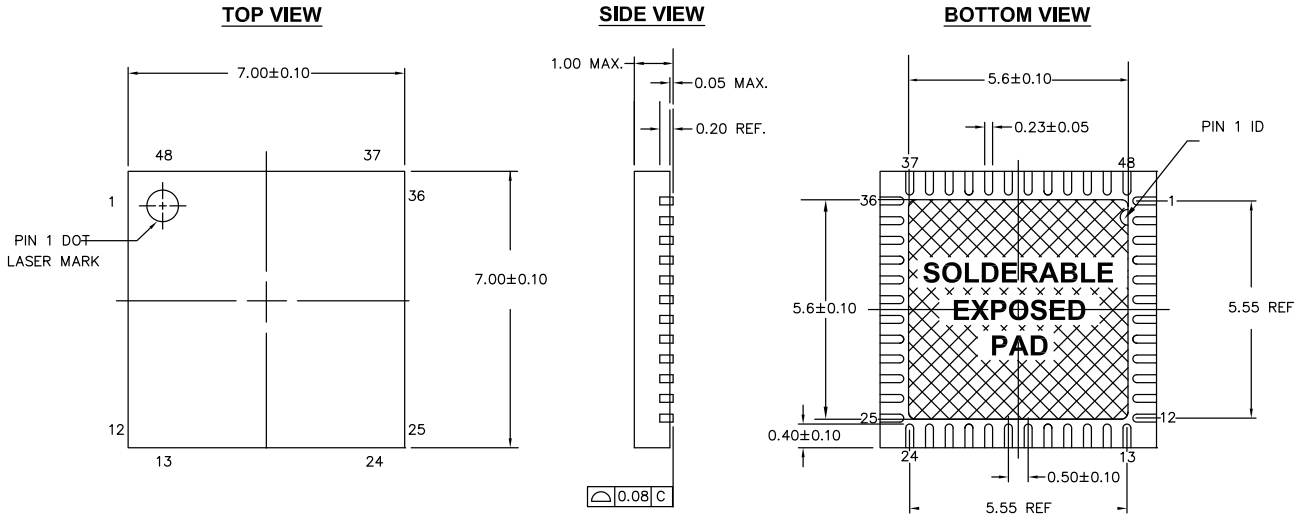
Packaging Dimensions

Figure 17. 20-pin SSOP (210 Mils) Package Outline O20.21, 51-85077



51-85077 *F

Figure 20. 48-pin QFN (7 × 7 × 1.0 mm) LT48D 5.6 × 5.6 E-Pad (Sawn Type) Package Outline, 001-45616



NOTES:
1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

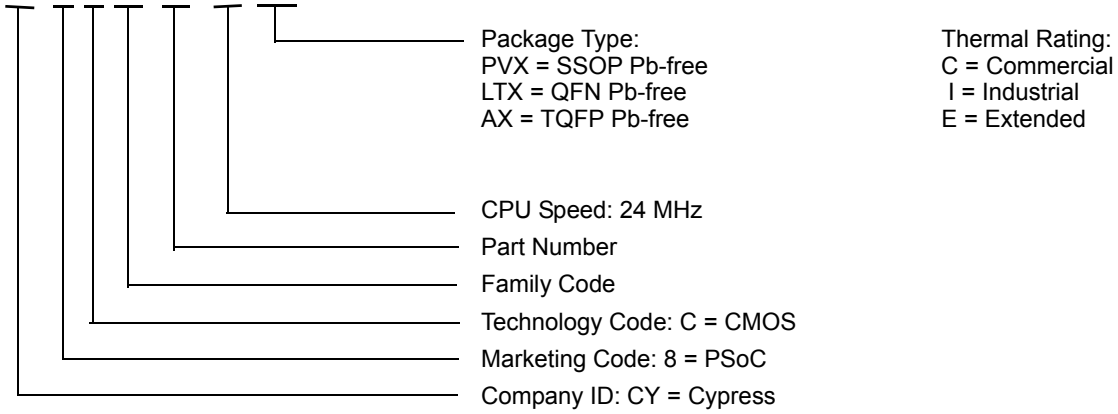
PART #	DESCRIPTION
LT48D	LEAD FREE

001-45616 *E

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Ordering Code Definitions

CY 8 C 28 xxx - SP xxxx



Glossary *(continued)*

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.