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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28533-24axi

System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, multiple decimators, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- Up to four decimators provide custom hardware filters for digital signal processing applications such as Delta-Sigma ADCs and CapSense capacitive sensor measurement.
- Up to two I²C resources provide 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported. I²C resources have hardware address detection capability.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.5 V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in this table.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 ^[2]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6 ^[2]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6 ^[2]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4 ^[2]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4 ^[2]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3 ^[2,3]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3 ^[2,3]	up to 2 K	up to 32 K

Notes

2. Limited analog functionality.
3. Two analog blocks and one CapSense®.

Table 10. CY8C28x13 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#		80		RD12RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W		81		RD12SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW		82		RD12IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#		83		RD12LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#		84		RD12LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W		85		RD12RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW		86		RD12RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#		87		RD12DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
PRT4GS	12	RW		52			92			D2	
PRT4DM2	13	RW		53			93		IDX_PP	D3	RW
PRT5DR	14	RW		54			94		MVR_PP	D4	RW
PRT5IE	15	RW		55			95		MVW_PP	D5	RW
PRT5GS	16	RW		56			96		I2C0_CFG	D6	RW
PRT5DM2	17	RW		57			97		I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#		60		DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW		62		DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#		63		DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#		64			A4			E4	
DBC01DR1	25	W		65			A5			E5	
DBC01DR2	26	RW		66			A6		DEC_CR0*	E6	RW
DBC01CR0	27	#		67			A7		DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RD10RI	B0	RW		F0	
DBC10DR1	31	W		71		RD10SYN	B1	RW		F1	
DBC10DR2	32	RW		72		RD10IS	B2	RW		F2	
DBC10CR0	33	#		73		RD10LT0	B3	RW		F3	
DBC11DR0	34	#		74		RD10LT1	B4	RW		F4	
DBC11DR1	35	W		75		RD10RO0	B5	RW		F5	
DBC11DR2	36	RW		76		RD10RO1	B6	RW		F6	
DBC11CR0	37	#		77		RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RD11RI	B8	RW		F8	
DCC12DR1	39	W		79		RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RD11IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RD11LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RD11LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D		RD11RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E		RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 11. CY8C28x13 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RD12RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RD12SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RD12IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RD12LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RD12LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RD12RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RD12RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RD12DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C	RW		CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW		60		GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW		61		GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW		62		GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW		63		GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW		64		RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW		66		RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW		67		RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW		69		SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RD10RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RD10SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RD10LT0	B3	RW		F3	
DBC11FN	34	RW		74	RW	RD10LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RD10RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RD10RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RD11RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GL_EN	79	RW	RD11SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RD11IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RD11LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RD11LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RD11RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 15. CY8C28x33 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RD12RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RD12SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RD12IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RD12LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RD12LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RD12RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RD12RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RD12DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RD10RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RD10SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RD10LT0	B3	RW		F3	
DBC11FN	34	RW		74		RD10LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RD10RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RD10RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RD11RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RD11SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RD11IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RD11LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RD11LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RD11RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 17. CY8C28x43 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RD12RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RD12SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RD12IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RD12LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RD12LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RD12RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RD12RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RD12DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW		E5	
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW		E6	
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW		E7	
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	EDO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RD10RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RD10SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR1	33	RW		73		RD10LT0	B3	RW		F3	
DBC11FN	34	RW		74		RD10LT1	B4	RW		F4	
DBC11IN	35	RW		75		RD10RO0	B5	RW		F5	
DBC11OU	36	RW		76		RD10RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RD10DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RD11RI	B8	RW		F8	
DCC12IN	39	RW		79		RD11SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RD11IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RD11LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RD11LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RD11RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

DC Electrical Characteristics

DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 24. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.00	–	5.25	V	
I_{DD}	Supply current	–	8	14	mA	Conditions are $V_{DD} = 5.0\text{ V}$, $T_A = 25^{\circ}\text{C}$, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DD3}	Supply current	–	5	9	mA	Conditions are $V_{DD} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DDP}	Supply current when IMO = 6 MHz using SLIMO mode=1	–	2	3	mA	Conditions are $V_{DD} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz.
I_{SB}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT. ^[12]	–	3	10	μA	Conditions are with internal slow speed oscillator, $V_{DD} = 3.3\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$.
I_{SBH}	Sleep (Mode) current with POR, LVD, sleep timer, and WDT at high temperature. ^[12]	–	4	25	μA	Conditions are with internal slow speed oscillator, $V_{DD} = 3.3\text{ V}$, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, sleep timer, WDT, and external crystal. ^[12]	–	4	13	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. $V_{DD} = 3.3\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$.
I_{SBXTLH}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and external crystal at high temperature. ^[12]	–	5	26	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. $V_{DD} = 3.3\text{ V}$, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$.
I_{SBRTC}	Current consumed by RTC during sleep	–	0.5	1	μA	Extra current consumed by the RTC during sleep. This number is typical at 25°C and 5 V.
V_{REF}	Reference voltage (Bandgap)	1.280	1.300	1.320	V	Trimmed for appropriate V_{DD} .
I_{SXRES}	Supply current with XRES asserted 5 V	–	0.65	3	mA	Max is peak current after XRES;
	Supply current with XRES asserted 3.3 V	–	0.4	1.5	mA	Typical value is the steady state current value. $T_A = 25^{\circ}\text{C}$.

Note

12. Standby (sleep) current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 25. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	$k\Omega$	
R_{PD}	Pull-down resistor	4	5.6	8	$k\Omega$	
V_{OH}	High output level	$V_{DD} - 1.0$	—	—	V	$I_{OH} = 10\text{ mA}$, $V_{DD} = 4.75\text{ to }5.25\text{ V}$ (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	—	—	0.75	V	$I_{OL} = 25\text{ mA}$, $V_{DD} = 4.75\text{ to }5.25\text{ V}$ (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	—	—	mA	$V_{OH} = V_{DD} - 1.0\text{ V}$, see the limitations of the total current in the note for V_{OH} .
I_{OL}	Low level sink current	25	—	—	mA	$V_{OL} = 0.75\text{ V}$, see the limitations of the total current in the note for V_{OL} .
V_{IL}	Input low level	—	—	0.8	V	$V_{DD} = 3.0\text{ to }5.25$.
V_{IH}	Input high level	2.1	—	—	V	$V_{DD} = 3.0\text{ to }5.25$.
V_H	Input hysteresis	—	60	—	mV	
I_{IL}	Input leakage (absolute value)	—	1	—	nA	Gross tested to $1\text{ }\mu\text{A}$.
C_{IN}	Capacitive load on pins as input	—	3.5	10	pF	Package and pin dependent. Temp = 25°C .
C_{OUT}	Capacitive load on pins as output	—	3.5	10	pF	Package and pin dependent. Temp = 25°C .

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 31. 5 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	20	$\mu\text{V}/^{\circ}\text{C}$	
V_{CMOB}	Common-mode input voltage range	0.5	–	$V_{DD} - 1.0$	V	
R_{OUTOB}	Output resistance Power = Low Power = High	– –	1 1	– –	Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = $32\ \Omega$ to $V_{DD}/2$) Power = Low Power = High	$0.5 \times V_{DD} + 1.3$ $0.5 \times V_{DD} + 1.3$	– –	– –	V V	
V_{LOWOB}	Low output voltage swing (Load = $32\ \Omega$ to $V_{DD}/2$) Power = Low Power = High	– –	– –	$0.5 \times V_{DD} - 1.3$ $0.5 \times V_{DD} - 1.3$	V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	– –	1.1 2.6	5.1 8.8	mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	$(0.5 \times V_{DD} - 1.0) \leq V_{OUT} \leq (0.5 \times V_{DD} + 0.9)$.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

The guaranteed specifications for RefHi and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 34. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.214	V _{DD} /2 + 1.279	V _{DD} /2 + 1.341	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.018	V _{DD} /2 – 0.004	V _{DD} /2 + 0.01	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.328	V _{DD} /2 – 1.301	V _{DD} /2 – 1.273	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 0.228	V _{DD} /2 + 1.284	V _{DD} /2 + 1.344	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.015	V _{DD} /2 – 0.002	V _{DD} /2 + 0.011	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.329	V _{DD} /2 – 1.303	V _{DD} /2 – 1.275	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.224	V _{DD} /2 + 1.287	V _{DD} /2 + 1.345	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.001	V _{DD} /2 + 0.012	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.328	V _{DD} /2 – 1.304	V _{DD} /2 – 1.275	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	V _{DD} /2 + Bandgap	V _{DD} /2 + 1.226	V _{DD} /2 + 1.288	V _{DD} /2 + 1.346	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.001	V _{DD} /2 + 0.012	V
		V _{REFLO}	Ref low	V _{DD} /2 – Bandgap	V _{DD} /2 – 1.328	V _{DD} /2 – 1.304	V _{DD} /2 – 1.276	V

Note

15. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 34. 5-V DC Analog Reference Specifications (continued)

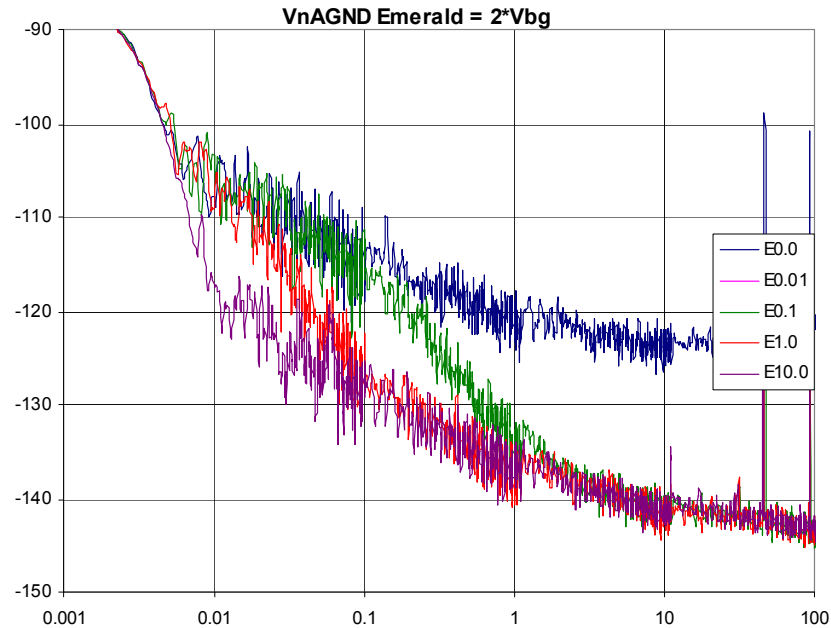
Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.055	P2[4] + P2[6] – 0.019	P2[4] + P2[6] + 0.019	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.035	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.05	P2[4] + P2[6] – 0.015	P2[4] + P2[6] + 0.021	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.001	P2[4] – P2[6] + 0.031	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.048	P2[4] + P2[6] – 0.013	P2[4] + P2[6] + 0.022	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] – 0.001	P2[4] – P2[6] + 0.031	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.047	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.023	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.036	P2[4] – P2[6] – 0.002	P2[4] – P2[6] + 0.030	V
0b010	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	V _{DD}	V _{DD} – 0.028	V _{DD} – 0.010	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.002	V _{DD} /2 + 0.012	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.008	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	V _{DD}	V _{DD} – 0.021	V _{DD} – 0.007	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.001	V _{DD} /2 + 0.012	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.005	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	V _{DD}	V _{DD} – 0.019	V _{DD} – 0.006	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.001	V _{DD} /2 + 0.012	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.004	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	V _{DD}	V _{DD} – 0.017	V _{DD} – 0.005	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.014	V _{DD} /2 – 0.001	V _{DD} /2 + 0.013	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.001	V _{SS} + 0.003	V

Table 35. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.226	P2[4] + 1.286	P2[4] + 1.343	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.323	P2[4] – 1.293	P2[4] – 1.262	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.232	P2[4] + 1.29	P2[4] + 1.344	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.324	P2[4] – 1.296	P2[4] – 1.267	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.233	P2[4] + 1.291	P2[4] + 1.345	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.324	P2[4] – 1.298	P2[4] – 1.269	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	P2[4] + Bandgap (P2[4] = V _{DD} /2)	P2[4] + 1.234	P2[4] + 1.292	P2[4] + 1.345	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref low	P2[4] – Bandgap (P2[4] = V _{DD} /2)	P2[4] – 1.324	P2[4] – 1.299	P2[4] – 1.270	V
0b110	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	2 × Bandgap	2.504	2.595	2.672	V
		V _{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.006	V _{SS} + 0.013	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	2 × Bandgap	2.506	2.593	2.674	V
		V _{AGND}	AGND	Bandgap	1.262	1.301	1.336	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.003	V _{SS} + 0.008	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	2 × Bandgap	2.506	2.594	2.675	V
		V _{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.002	V _{SS} + 0.007	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	2 × Bandgap	2.507	2.595	2.675	V
		V _{AGND}	AGND	Bandgap	1.262	1.301	1.335	V
		V _{REFLO}	Ref low	V _{SS}	V _{SS}	V _{SS} + 0.001	V _{SS} + 0.005	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

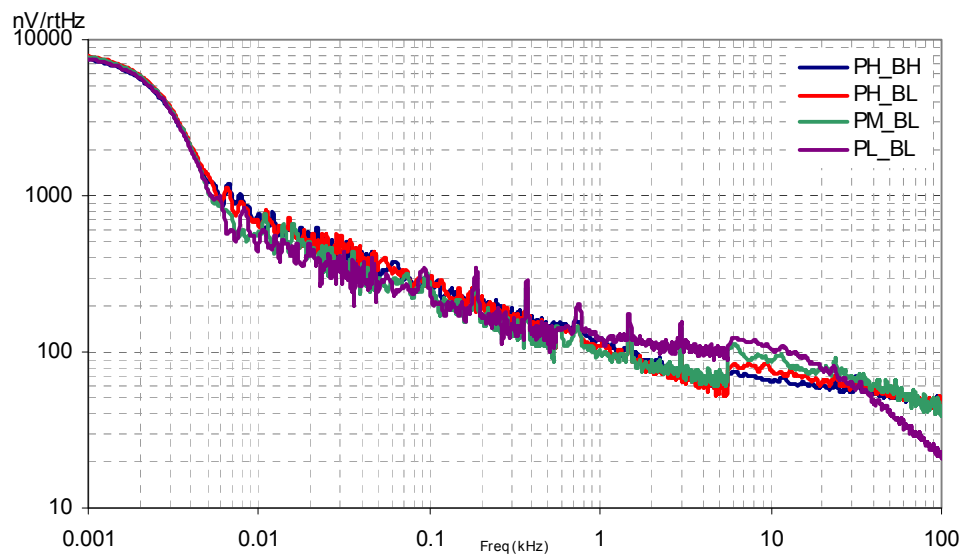
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 14. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to $1/f$, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 15. Typical Opamp Noise



AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 49. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block Input Clock Frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
Timer	Input Clock Frequency					
	No Capture, $V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	No Capture, $V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
	With Capture	–	–	25	MHz	
	Capture Pulse Width	50 ^[27]	–	–	ns	
Counter	Input Clock Frequency					
	No Enable Input, $V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	No Enable Input, $V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
	With Enable Input	–	–	25	MHz	
	Enable Input Pulse Width	50 ^[27]	–	–	ns	
Dead Band	Kill Pulse Width					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50 ^[27]	–	–	ns	
	Disable Mode	50 ^[27]	–	–	ns	
	Input Clock Frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
CRCPRS (PRS Mode)	Input Clock Frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
CRCPRS (CRC Mode)	Input Clock Frequency	–	–	25	MHz	
SPIM	Input Clock Frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_Negated Between Transmissions	50 ^[13]	–	–	ns	
Transmitter	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75\text{ V}$, 2 Stop Bits	–	–	49	MHz	
	$V_{DD} \geq 4.75\text{ V}$, 1 Stop Bit	–	–	25	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	
Receiver	Input Clock Frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75\text{ V}$, 2 Stop Bits	–	–	49	MHz	
	$V_{DD} \geq 4.75\text{ V}$, 1 Stop Bit	–	–	25	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	25	MHz	

Note

27. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Figure 18. 28-pin SSOP (210 Mils) O28.21 Package Outline, 51-85079

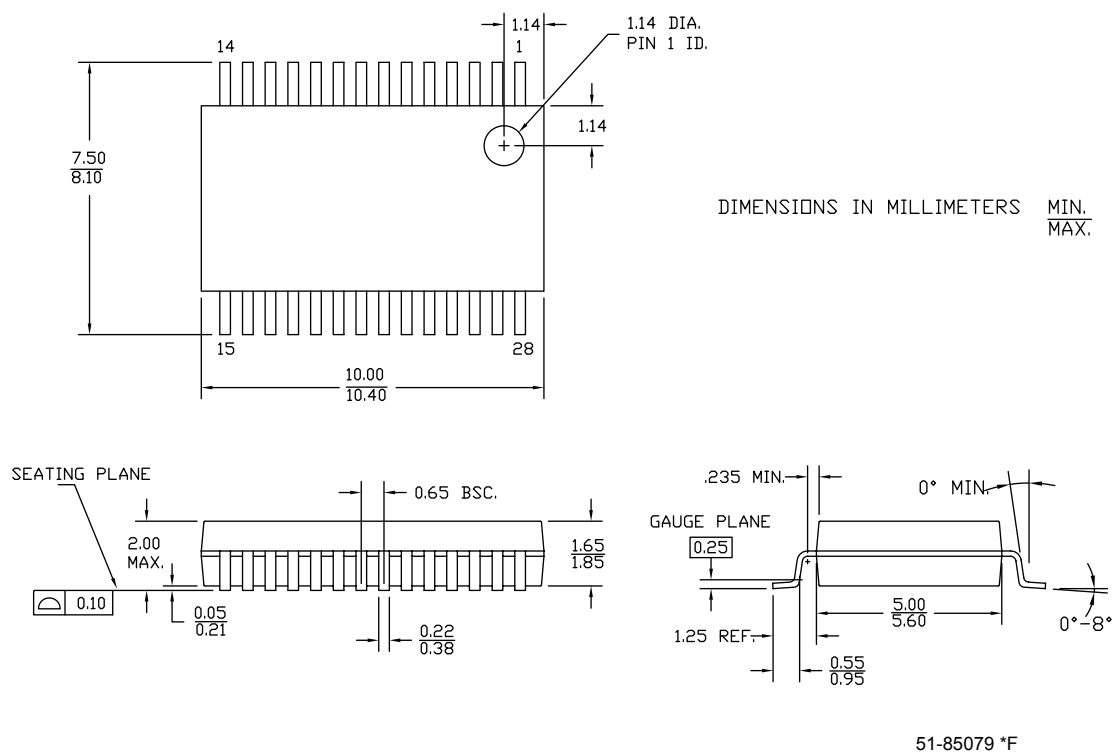


Figure 19. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064

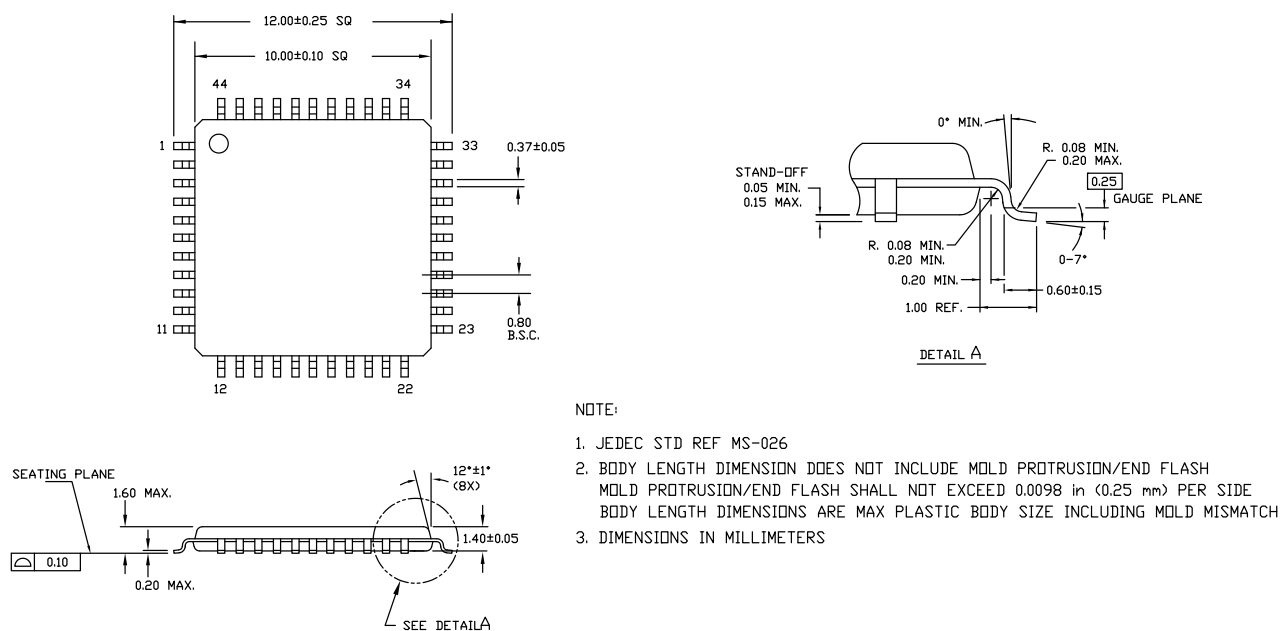
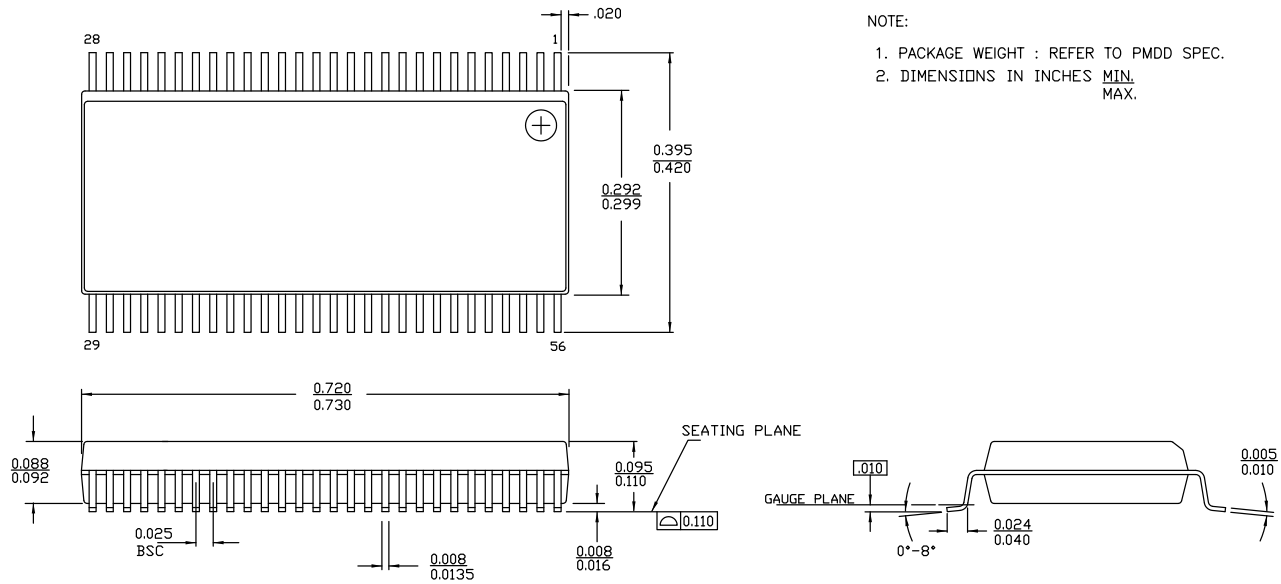


Figure 21. 56-pin SSOP (300 Mils) O563 Package Outline, 51-85062



51-85062 *F

Acronyms

Acronyms Used

Table 61 lists the acronyms that are used in this document.

Table 61. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC®	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SLIMO	slow IMO
IMO	internal main oscillator	SMP	switch mode pump
I/O	input/output	SOIC	small-outline integrated circuit
IrDA	infrared data association	SPI™	serial peripheral interface
ISSP	in-system serial programming	SRAM	static random access memory
LCD	liquid crystal display	SROM	supervisory read only memory
LED	light-emitting diode	SSOP	shrink small-outline package
LPC	low power comparator	UART	universal asynchronous receiver / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 available at <http://www.cypress.com>.

Glossary *(continued)*

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary *(continued)*

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

1. 10-bit SAR ADC does not meet DNL/INL specification.

■ Problem Definition

The 10-bit hardware SAR ADC does not meet datasheet accuracy specifications for DNL and INL under some conditions.

■ Parameters Affected

INLSAR10: Integral nonlinearity

DNLSAR10: Differential nonlinearity

■ Trigger Condition(S)

The SAR ADC DNL has been measured greater than 2 LSB over temperature in all cases, as compared to the datasheet specification of 1.5 LSB.

When using the VPWR (Vdd) reference configuration, the SAR ADC DNL has been measured over temperature at 2 LSB for a supply voltage of 3.3 V. With a supply voltage of 5.5 V, the DNL has been measured greater than 3.5 LSB.

■ Scope of Impact

Inaccurate converted data.

■ Workaround

- Use an alternate ADC implementation (DelSig, ADCINC) available in CY8C28xxx devices.
- Avoid CPU operations that change the address and data buses while A-D conversion is running with internal Vpwr (Vdd) as Vref.
- Use un-buffered RefHi as ADC Vref. This may have a negative effect on the analog blocks in the analog array due to the noise introduced on RefHi reference.

■ Fix Status

Silicon fix is not planned. The workaround mentioned above should be used.

2. Wrong data read from IDAC_CRx and DACx_D registers.

■ Problem Definition

The CPU may read an incorrect value of bits 0, 3, 5, or 7 from the following registers:

- IDAC_CR0
- IDAC_CR1
- DAC0_D
- DAC1_D

■ Parameters Affected

F_{CPU1} and F_{CPU2} from the device data sheet.

■ Trigger Condition(S)

When CPU Clock is set at its highest frequency setting (24 MHz nominal).

■ Scope of Impact

Incorrect data read from affected registers.

■ Workaround

Temporarily slow down CPU Clock frequency to 12 MHz nominal (or lower) when affected registers are read.

Document History Page *(continued)*

Document Title: CY8C28243/CY8C28403/CY8C28413/CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/ CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™ Document Number: 001-48111				
Revision	ECN	Origin of Change	Submission Date	Description of Change
*L	3993399	GVH	05/08/2013	Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata .
*M	4138595	GVH	09/27/2013	Updated to new template. Completing Sunset Review.
*N	4476160	ASRI / SEG	09/04/2014	Replaced references of "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" with "Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845" in all instances across the document. Added More Information . Added PSoC Designer . Updated PSoC Functional Overview : Updated PSoC Device Characteristics : Updated Table 2 : Added a column "Analog Mux Buses" at the end. Removed "Getting Started". Updated Electrical Specifications : Updated DC Electrical Characteristics : Updated DC I2C Specifications : Updated Table 42 : Added V_{OLI2C} parameter and its details. Updated Packaging Information : spec 51-85064 – Changed revision from *E to *F. Completing Sunset Review.
*O	4914758	ASRI	09/10/2015	Updated Document Title to read as "CY8C28243/CY8C28403/CY8C28413/CY8C28433/CY8C28445/CY8C28452/CY8C28513/CY8C28545/CY8C28623/CY8C28643/CY8C28645, PSoC® Programmable System-on-Chip™". Removed CY8C28533 related information in all instances across the document. Updated Electrical Specifications : Updated DC Electrical Characteristics : Updated DC SAR10 ADC Specifications : Updated Table 38 : Updated details in "Description" column of DNL_{SAR10} parameter. Updated Packaging Information : Updated Packaging Dimensions : spec 51-85077 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. spec 001-45616 – Changed revision from *D to *E. Updated Development Tool Selection : Updated Accessories (Emulation and Programming) : Updated Table 60 : Updated details in "Part #" column corresponding to 44-pin TQFP package. Updated Ordering Information : Updated part numbers. Updated Errata : Updated Part Numbers Affected : Updated table. Updated Errata Summary : Updated table and also details below the table. Updated to new template. Completing Sunset Review.