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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28533-24axit

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article “How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292”. Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
 - [Getting Started with PSoC® 1 – AN75320](#)
 - [PSoC® 1 - Getting Started with GPIO – AN2094](#)
 - [PSoC® 1 Analog Structure and Configuration – AN74170](#)
 - [PSoC® 1 Switched Capacitor Analog Blocks – AN2041](#)
 - [Selecting Analog Ground and Reference – AN2219](#)

Note: For CY8C28xxx devices related Application note please click [here](#).

- Development Kits:
 - [CY3210-PSocEval1](#) supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
 - [CY3214-PSocEvalUSB](#) features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C28xxx devices related Development Kits please click [here](#).

The [MiniProg1](#) and [MiniProg3](#) devices provide interfaces for flash programming and debug.

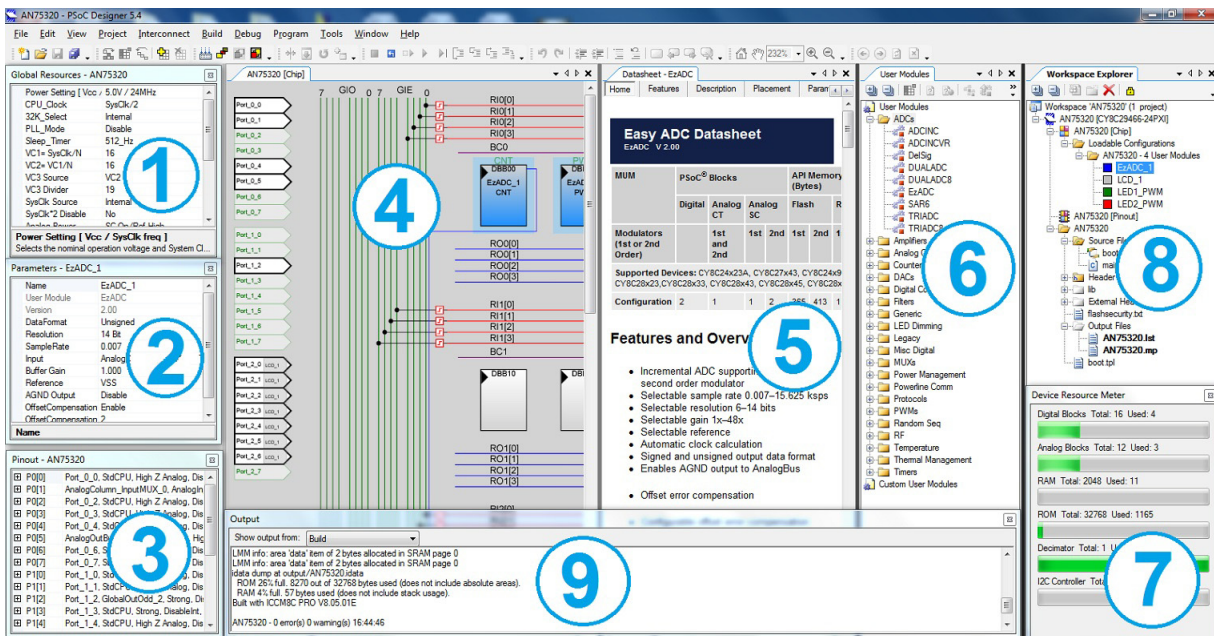
PSoC Designer

[PSoC Designer](#) is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. [Figure 1](#) shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources** – all device hardware settings.
2. **Parameters** – the parameters of the currently selected User Modules.
3. **Pinout** – information related to device pins.
4. **Chip-Level Editor** – a diagram of the resources available on the selected chip.
5. **Datasheet** – the datasheet for the currently selected UM
6. **User Modules** – all available User Modules for the selected device.
7. **Device Resource Meter** – device resource usage for the current project configuration.
8. **Workspace** – a tree level diagram of files associated with the project.
9. **Output** – output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



PSoC Functional Overview

The PSoC family consists of many devices with On-Chip Controllers. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog blocks, digital blocks, and interconnections. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. In addition, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The CY8C28xxx group of PSoC devices described in this datasheet have multiple resource configuration options available. Therefore, not every resource mentioned in this datasheet is available for each CY8C28xxx subgroup. The CY8C28x45 subgroup has a full feature set of all resources described. There are six more segmented subgroups that allow designers to use a device with only the resources and functionality necessary for a specific application. See [Table 2](#) on page 9 to determine the resources available for each CY8C28xxx subgroup. The same information is also presented in more detail in the [Ordering Information](#) section.

The architecture for this specific PSoC device family, as shown in the [Logic Block Diagram](#) on page 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. The configurable global bus system allows all the device resources to be combined into a complete custom system. PSoC CY8C28xxx family devices have up to six I/O ports that connect to the global digital and analog interconnects, providing access to up to 12 digital blocks and up to 16 analog blocks.

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general Purpose I/O (GPIO). The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microcontroller.

Memory encompasses 16K bytes of Flash for program storage, 1K bytes of SRAM for data storage. The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 2.5% over temperature and voltage. A low power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and watch dog timer (WDT). The 32.768 kHz external crystal oscillator (ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL.

PSoC GPIOs provide connections to the CPU, and digital and analog resources. Each pin's drive mode may be selected from 8 options, which allows great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

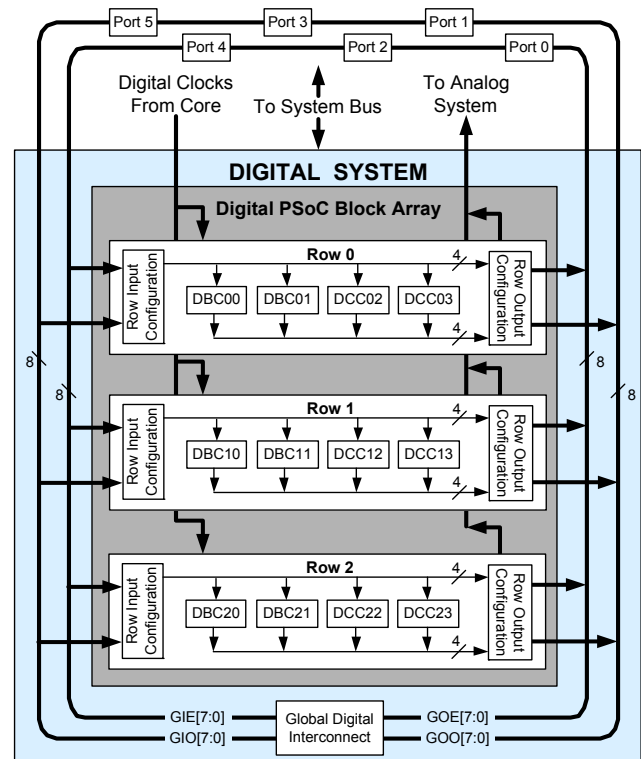
The Digital System is composed of up to 12 configurable digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to create 8, 16, 24, and

Note

1. CY8C28x52 devices do not have digital block row 2. They have two digital rows with eight total digital blocks.

32-bit peripherals, which are called user modules. The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin.

Figure 2. Digital System Block Diagram^[1]



Digital peripheral configurations include:

- PWMs (8- and 16-bit, One-shot and Multi-shot capability)
- PWMs with Dead band/Kill (8- and 16-bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- Full-duplex 8-bit UARTs (up to 3) with selectable parity
- Half-duplex 8-bit UARTs (up to 6) with selectable parity
- Variable length SPI slave and master
 - Up to 6 total slaves and masters (8-bit)
 - Supports 8 to 16 bit operation
- I²C slave, master, or multi-master (up to 2 available as System Resources)
- IrDA (up to 3)
- Pseudo Random Sequence Generators (8 to 32 bit)
- Cyclical Redundancy Checker/Generator (16 bit)
- Shift Register (2 to 32 bit)

Pinouts

This section describes, lists, and illustrates the CY8C28xxx PSoC device pins and pinout configurations.

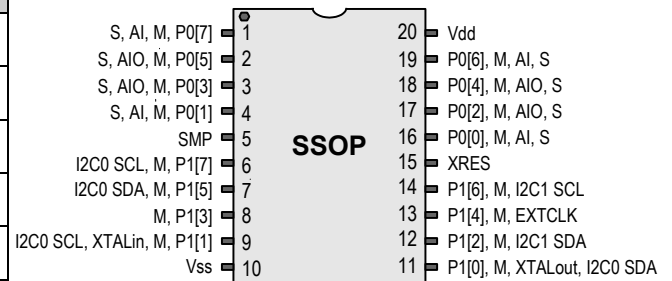
The CY8C28xxx PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of Digital I/O. However, V_{SS} , V_{DD} , SMP, and XRES are not capable of Digital I/O.

20-pin Part Pinout

Table 3. 20-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input. ^[5]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input. ^[5]
5	Output		SMP	Switch Mode Pump (SMP) connection to external components.
6	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
7	I/O	M	P1[5]	I2C0 Serial Data (SDA).
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK ^[4] .
10	Power		V_{SS}	Ground connection.
11	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA ^[4] .
12	I/O	M	P1[2]	I2C1 Serial Data (SDA). ^[7]
13	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
14	I/O	M	P1[6]	I2C1 Serial Clock (SCL). ^[7]
15	Input		XRES	Active high external reset with internal pull-down.
16	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input. ^[5]
17	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output. ^[5, 8]
18	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output. ^[5, 8]
19	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input. ^[5]
20	Power		V_{DD}	Supply voltage.

CY8C28243 20-pin PSoC Device



LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

Notes

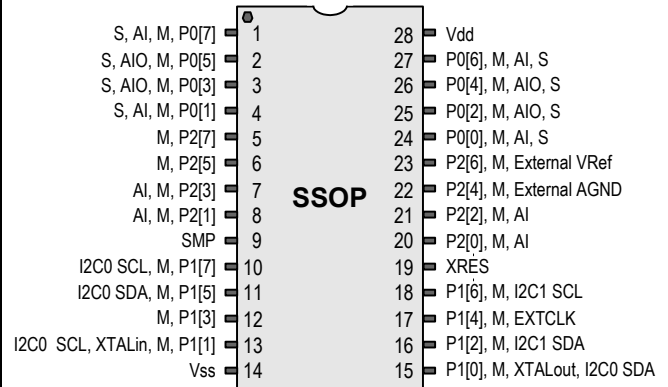
- These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices for details.
- CY8C28x52 and CY8C28x23 devices do not have a SAR ADC. Therefore, this pin does not function as a SAR ADC input for these devices.
- CY8C28x13 and CY8C28x03 devices do not have any analog output buffers. Therefore, this pin does not function as an analog column output for these devices.
- CY8C28x52, CY8C28x13, and CY8C28x33 devices only have one I2C block. Therefore, this GPIO does not function as an I2C pin for these devices.
- CY8C28x33, CY8C28x23, CY8C28x13, and CY8C28x03 devices do not have an analog output buffer for this pin. Therefore, this pin does not function as an analog column output for these devices.

28-pin Part Pinout

Table 4. 28-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input. ^[5]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output. ^[5, 6]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input. ^[5]
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	I, M	P2[3]	Direct switched capacitor block input. ^[9]
8	I/O	I, M	P2[1]	Direct switched capacitor block input. ^[9]
9	Output		SMP	Switch Mode Pump (SMP) connection to external components.
10	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
11	I/O	M	P1[5]	I2C0 Serial Data (SDA).
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK ^[4] .
14	Power		V _{SS}	Ground connection.
15	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA ^[4] .
16	I/O	M	P1[2]	I2C1 Serial Data (SDA). ^[7]
17	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
18	I/O	M	P1[6]	I2C1 Serial Clock (SCL). ^[7]
19	Input		XRES	Active high external reset with internal pull-down.
20	I/O	I, M	P2[0]	Direct switched capacitor block input. ^[10]
21	I/O	I, M	P2[2]	Direct switched capacitor block input. ^[10]
22	I/O	M	P2[4]	External Analog Ground (AGND).
23	I/O	M	P2[6]	External Voltage Reference (VRef).
24	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input. ^[5]
25	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output. ^[5, 8]
26	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output. ^[5, 8]
27	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input. ^[5]
28	Power		V _{DD}	Supply voltage.

CY8C28403, CY8C28413, CY8C28433, CY8C28445, and CY8C28452 28-pin PSoC Devices



LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input

Notes

- This pin is not a direct switched capacitor block analog input for CY8C28x03 and CY8C28x13 devices.
- This pin is not a direct switched capacitor block analog input for CY8C28x03, CY8C28x13, CY8C28x23, and CY8C28x33 devices.

Table 7. 56-pin Part Pinout (SSOP) (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
41	Input		XRES	Active high external reset with internal pull-down.
42	OCD	M	HCLK	OCD high speed clock output.
43	OCD	M	CCLK	OCD CPU clock output.
44	I/O	M	P4[0]	
45	I/O	M	P4[2]	
46	I/O	M	P4[4]	
47	I/O	M	P4[6]	
48	I/O	I, M	P2[0]	Direct switched capacitor block input.
49	I/O	I, M	P2[2]	Direct switched capacitor block input.
50	I/O	M	P2[4]	External Analog Ground (AGND).
51	I/O	M	P2[6]	External Voltage Reference (VRef).
52	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.
53	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.
54	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.
55	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.
56	Power		V _{DD}	Supply voltage.

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, M = Analog Mux Bus Input, and OCD = On-Chip Debug.

Table 13. CY8C28x23 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW		81		RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW		82		RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94	RW	DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A		DEC_CR5	9A	RW		DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VL_T_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VL_T_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW		E5	
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW		E6	
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW		E7	
DCC02FN	28	RW		68			A8		IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCC02OU	2A	RW		6A			AA		BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW		AB		ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW		71		RDI0SYN	B1	RW		F1	
DBC10OU	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251



Table 16. CY8C28x43 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#	ASC12CR0	88	RW		C8	
PRT2IE	09	RW	DCC22DR1	49	W	ASC12CR1	89	RW		C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW	ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#	ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW	DCC23DR0	4C	#	ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW	DCC23DR1	4D	W	ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW	ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC	I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC	I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW	DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251



Table 19. CY8C28x45 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C	RW		CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

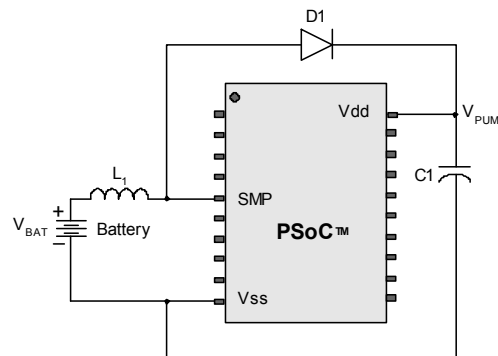
DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 $^{\circ}\text{C}$ and are for design guidance only.

Table 33. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{\text{PUMP } 5\text{ V}}$	5 V output voltage	4.75	5.0	5.25	V	Configuration of footnote. ^[14] Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
$V_{\text{PUMP } 3\text{ V}}$	3 V output voltage	3.00	3.25	3.60	V	Configuration of footnote. ^[14] Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
I_{PUMP}	Available output current $V_{\text{BAT}} = 1.5\text{ V}$, $V_{\text{PUMP}} = 3.25\text{ V}$ $V_{\text{BAT}} = 1.8\text{ V}$, $V_{\text{PUMP}} = 5.0\text{ V}$	8 5	– –	– –	mA mA	Configuration of footnote. ^[14] SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 5.0 V.
$V_{\text{BAT}5\text{ V}}$	Input voltage range from battery	1.8	–	5.0	V	Configuration of footnote. ^[14] SMP trip voltage is set to 5.0 V.
$V_{\text{BAT}3\text{ V}}$	Input voltage range from battery	1.5	–	3.3	V	Configuration of footnote. ^[14] SMP trip voltage is set to 3.25 V.
V_{BATSTART}	Minimum input voltage from battery to start pump	2.6	–	–	V	Configuration of footnote. ^[14]
$\Delta V_{\text{PUMP_Line}}$	Line regulation (over V_{BAT} range)	–	5	–	% V_{O}	Configuration of footnote. ^[14] V_{O} is the “ V_{DD} Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 40 on page 52.
$\Delta V_{\text{PUMP_Load}}$	Load regulation	–	5	–	% V_{O}	Configuration of footnote. ^[14] V_{O} is the “ V_{DD} Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 40 on page 52.
$\Delta V_{\text{PUMP_Ripple}}$	Output voltage ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration of footnote. ^[14] Load is 5mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote. ^[14] Load is 5 mA. SMP trip voltage is set to 3.25 V.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Figure 9. Basic Switch Mode Pump Circuit



Note

14. $L_1 = 2\text{ }\mu\text{H}$ inductor, $C_1 = 10\text{ }\mu\text{F}$ capacitor, $D_1 =$ Schottky diode. See [Figure 9](#).

Table 34. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b011	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	3 × Bandgap	3.736	3.887	4.030	V
		V _{AGND}	AGND	2 × Bandgap	2.525	2.598	2.667	V
		V _{REFLO}	Ref low	Bandgap	1.265	1.302	1.335	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	3 × Bandgap	3.747	3.894	4.034	V
		V _{AGND}	AGND	2 × Bandgap	2.528	2.601	2.668	V
		V _{REFLO}	Ref low	Bandgap	1.264	1.302	1.335	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	3 × Bandgap	3.749	3.897	4.035	V
		V _{AGND}	AGND	2 × Bandgap	2.529	2.602	2.668	V
		V _{REFLO}	Ref low	Bandgap	1.264	1.302	1.335	V
RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	3 × Bandgap	3.751	3.899	4.037	V	
	V _{AGND}	AGND	2 × Bandgap	2.530	2.603	2.669	V	
	V _{REFLO}	Ref low	Bandgap	1.264	1.302	1.335	V	
0b100	RefPower = High Opamp bias = High	V _{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.483 – P2[6]	2.578 – P2[6]	2.669 – P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.525	2.598	2.666	V
		V _{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.512 – P2[6]	2.602 – P2[6]	2.684 – P2[6]	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 – P2[6]	2.586 – P2[6]	2.673 – P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.528	2.601	2.668	V
		V _{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.510 – P2[6]	2.602 – P2[6]	2.685 – P2[6]	V
	RefPower = Medium Opamp bias = High	V _{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.498 – P2[6]	2.589 – P2[6]	2.674 – P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.529	2.601	2.668	V
		V _{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.509 – P2[6]	2.601 – P2[6]	2.685 – P2[6]	V
	RefPower = Medium Opamp bias = Low	V _{REFHI}	Ref high	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 – P2[6]	2.591 – P2[6]	2.675 – P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.530	2.603	2.669	V
		V _{REFLO}	Ref low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.508 – P2[6]	2.601 – P2[6]	2.686 – P2[6]	V

DC IDAC Specifications

Table 39. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	-5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_INL	Integral nonlinearity	-5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_Gain	Gain per bit – Range 1 (91 μ A)	283	357	447	nA	Measured at full scale
	Gain per bit – Range 2 (318 μ A)	985	1250	1532	nA	
	Gain per bit – Range 3 (637 μ A)	1959	2500	3056	nA	
IDACOffset	Offset at Code 0 vs LSB Ideal – Range 1 (91 μ A)		2.0%	20%	%	Measured as a % of LSB (Current @ Code 0)/(LSB Ideal Current)
	Offset at Code 0 vs LSB Ideal – Range 2 (318 μ A)		1.0%	10%	%	
	Offset at Code 0 vs LSB Ideal – Range 3 (637 μ A)		1.0%	10%	%	

DC I²C Specifications

Table 42 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 42. DC I²C Specifications^[20]

Symbol	Description	Min	Typ	Max	Units	Notes
V _{IL} I2C	Input low level	–	–	$0.3 \times V_{DD}$	V	$3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$
		–	–	$0.25 \times V_{DD}$	V	$4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$
V _{IH} I2C	Input high level	$0.7 \times V_{DD}$	–	–	V	$3.0\text{ V} \leq V_{DD} \leq 5.25\text{ V}$
V _{OL} I2C	Output low level	–	–	0.4	V	at sink current of 3 mA
		–	–	0.6	V	at sink current of 6 mA

Note

20. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the above specs.

Figure 10. PLL Lock Timing Diagram

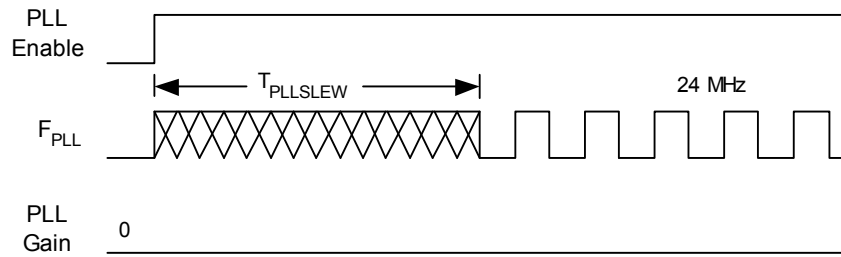


Figure 11. PLL Lock for Low Gain Setting Timing Diagram

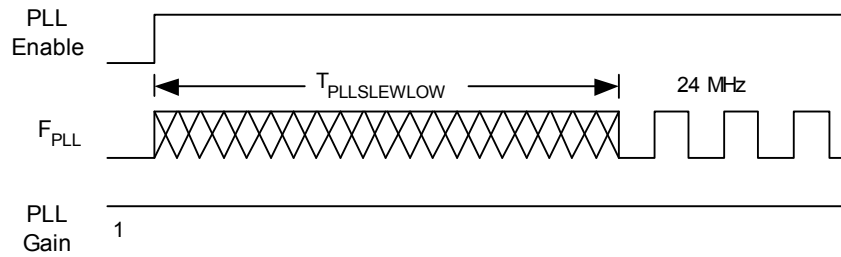


Figure 12. External Crystal Oscillator Startup Timing Diagram

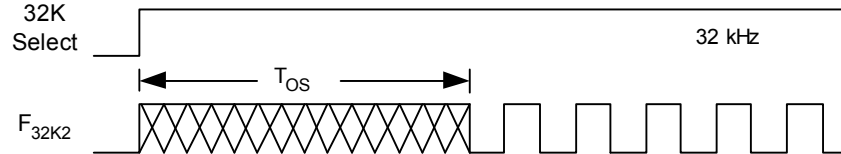
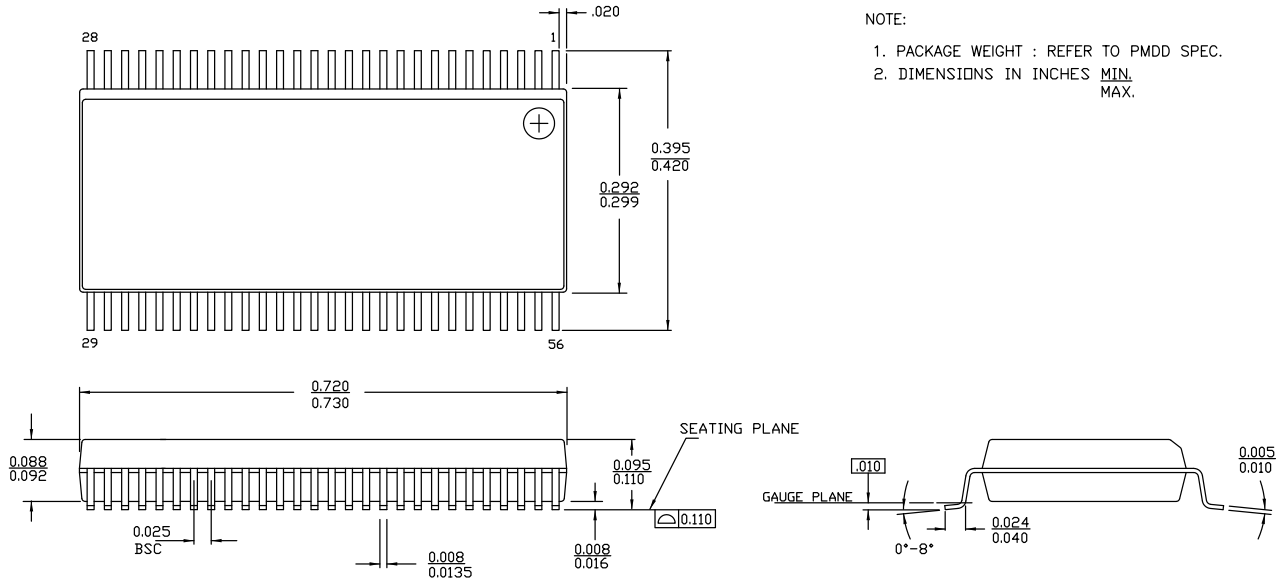


Figure 21. 56-pin SSOP (300 Mils) O563 Package Outline, 51-85062



NOTE:
 1. PACKAGE WEIGHT : REFER TO PMDD SPEC.
 2. DIMENSIONS IN INCHES MIN.
 MAX.

51-85062 *F

Thermal Impedances

Table 57. Thermal Impedances per Package

Package	Typical θ_{JA} [32]
20-pin SSOP	80.8 °C/W
28-pin SSOP	45.4 °C/W
44-pin TQFP	24.0 °C/W
48-pin QFN [33]	16.7 °C/W
56-pin SSOP	67.5 °C/W

Capacitance on Crystal Pins

Table 58. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
20-pin SSOP	Pin9 = 0.0056 pF Pin11 = 0.006048 pF
28-pin SSOP	Pin13 = 0.006796 pF Pin15 = 0.006755 pF
44-pin TQFP	Pin16 = 0.009428 pF Pin18 = 0.008635 pF
48-pin QFN	Pin17 = 0.008493 pF Pin19 = 0.008742 pF
56-pin SSOP	Pin27 = 0.007916 pF Pin31 = 0.007132 pF

Solder Reflow Specifications

Table 59 shows the solder reflow temperature limits that must not be exceeded.

Table 59. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above $T_C - 5\text{ °C}$
20-pin SSOP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
56-pin SSOP	260 °C	30 seconds

Notes

32. $T_J = T_A + \text{POWER} \times \theta_{JA}$

33. To achieve the thermal impedance specified for the QFN package, refer to *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at <http://www.cypress.com> for PCB requirements.

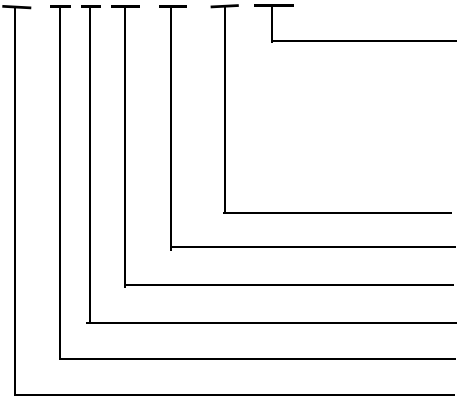
34. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are $220 \pm 5\text{ °C}$ with Sn-Pb or $245 \pm 5\text{ °C}$ with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.



CY8C28243/CY8C28403/CY8C28413
CY8C28433/CY8C28445/CY8C28452
CY8C28513/CY8C28545
CY8C28623/CY8C28643/CY8C28645

Ordering Code Definitions

CY 8 C 28 xxx - SP xxxx



Package Type:
PVX = SSOP Pb-free
LTX = QFN Pb-free
AX = TQFP Pb-free

Thermal Rating:
C = Commercial
I = Industrial
E = Extended

CPU Speed: 24 MHz
Part Number
Family Code
Technology Code: C = CMOS
Marketing Code: 8 = PSoC
Company ID: CY = Cypress

Acronyms

Acronyms Used

Table 61 lists the acronyms that are used in this document.

Table 61. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC [®]	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SLIMO	slow IMO
IMO	internal main oscillator	SMP	switch mode pump
I/O	input/output	SOIC	small-outline integrated circuit
IrDA	infrared data association	SPI [™]	serial peripheral interface
ISSP	in-system serial programming	SRAM	static random access memory
LCD	liquid crystal display	SROM	supervisory read only memory
LED	light-emitting diode	SSOP	shrink small-outline package
LPC	low power comparator	UART	universal asynchronous receiver / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC[®] Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC[®] Flash – AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 available at <http://www.cypress.com>.

Document Conventions

Units of Measure

Table 62 lists the unit sof measures.

Table 62. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	μs	microsecond
dB	decibels	ms	millisecond
°C	degree Celsius	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	μV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kiloohm	V	volts
Ω	ohm	μW	microwatts
μA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
mH	millihenry		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

Glossary

active high	<ol style="list-style-type: none"> 5. A logic signal having its asserted state as the logic 1 state. 6. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	<ol style="list-style-type: none"> 1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

1. 10-bit SAR ADC does not meet DNL/INL specification.

■ Problem Definition

The 10-bit hardware SAR ADC does not meet datasheet accuracy specifications for DNL and INL under some conditions.

■ Parameters Affected

INLSAR10: Integral nonlinearity

DNLSAR10: Differential nonlinearity

■ Trigger Condition(S)

The SAR ADC DNL has been measured greater than 2 LSB over temperature in all cases, as compared to the datasheet specification of 1.5 LSB.

When using the VPWR (Vdd) reference configuration, the SAR ADC DNL has been measured over temperature at 2 LSB for a supply voltage of 3.3 V. With a supply voltage of 5.5 V, the DNL has been measured greater than 3.5 LSB.

■ Scope of Impact

Inaccurate converted data.

■ Workaround

- Use an alternate ADC implementation (DeISig, ADCINC) available in CY8C28xxx devices.
- Avoid CPU operations that change the address and data buses while A-D conversion is running with internal Vpwr (Vdd) as Vref.
- Use un-buffered RefHi as ADC Vref. This may have a negative effect on the analog blocks in the analog array due to the noise introduced on RefHi reference.

■ Fix Status

Silicon fix is not planned. The workaround mentioned above should be used.

2. Wrong data read from IDAC_CRx and DACx_D registers.

■ Problem Definition

The CPU may read an incorrect value of bits 0, 3, 5, or 7 from the following registers:

- IDAC_CR0
- IDAC_CR1
- DAC0_D
- DAC1_D

■ Parameters Affected

F_{CPU1} and F_{CPU2} from the device data sheet.

■ Trigger Condition(S)

When CPU Clock is set at its highest frequency setting (24 MHz nominal).

■ Scope of Impact

Incorrect data read from affected registers.

■ Workaround

Temporarily slow down CPU Clock frequency to 12 MHz nominal (or lower) when affected registers are read.



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