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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c28545-24axi

PSoC Functional Overview

The PSoC family consists of many devices with On-Chip Controllers. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog blocks, digital blocks, and interconnections. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. In addition, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The CY8C28xxx group of PSoC devices described in this datasheet have multiple resource configuration options available. Therefore, not every resource mentioned in this datasheet is available for each CY8C28xxx subgroup. The CY8C28x45 subgroup has a full feature set of all resources described. There are six more segmented subgroups that allow designers to use a device with only the resources and functionality necessary for a specific application. See Table 2 on page 9 to determine the resources available for each CY8C28xxx subgroup. The same information is also presented in more detail in the Ordering Information section.

The architecture for this specific PSoC device family, as shown in the Logic Block Diagram on page 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. The configurable global bus system allows all the device resources to be combined into a complete custom system. PSoC CY8C28xxx family devices have up to six I/O ports that connect to the global digital and analog interconnects, providing access to up to 12 digital blocks and up to 16 analog blocks.

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general Purpose I/O (GPIO). The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microcontroller.

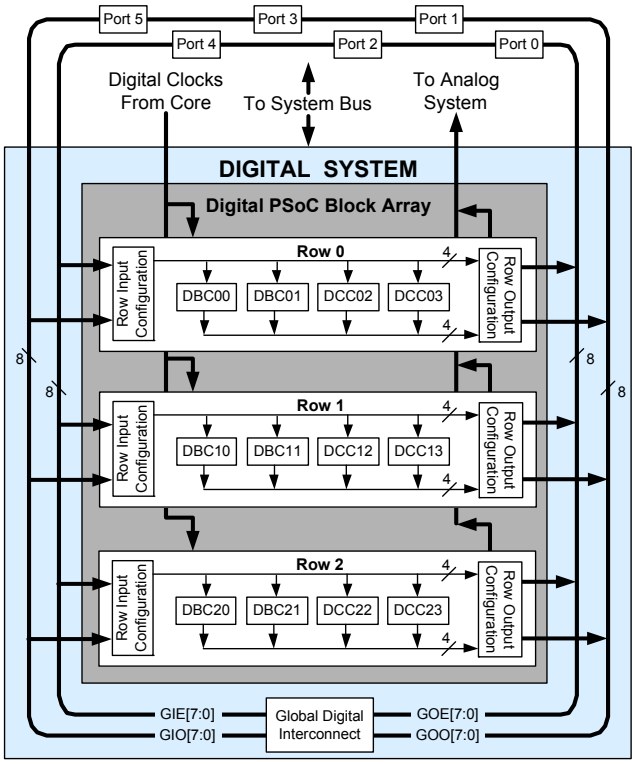
Memory encompasses 16K bytes of Flash for program storage, 1K bytes of SRAM for data storage. The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 2.5% over temperature and voltage. A low power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and watch dog timer (WDT). The 32.768 kHz external crystal oscillator (ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL.

PSoC GPIOs provide connections to the CPU, and digital and analog resources. Each pin's drive mode may be selected from 8 options, which allows great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of up to 12 configurable digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to create 8, 16, 24, and 32-bit peripherals, which are called user modules. The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin.

Figure 2. Digital System Block Diagram[1]



Digital peripheral configurations include:

- PWMs (8- and 16-bit, One-shot and Multi-shot capability)
- PWMs with Dead band/Kill (8- and 16-bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- Full-duplex 8-bit UARTs (up to 3) with selectable parity
- Half-duplex 8-bit UARTs (up to 6) with selectable parity
- Variable length SPI slave and master
  - Up to 6 total slaves and masters (8-bit)
  - Supports 8 to 16 bit operation
- I^2C slave, master, or multi-master (up to 2 available as System Resources)
- IrDA (up to 3)
- Pseudo Random Sequence Generators (8 to 32 bit)
- Cyclical Redundancy Checker/Generator (16 bit)
- Shift Register (2 to 32 bit)

Note
1. CY8C28x52 devices do not have digital block row 2. They have two digital rows with eight total digital blocks.

The devices covered by this datasheet all have the same architecture, specifications, and ratings. However, the amount of some hardware resources varies from device to device within the group. The following table lists resources available for the specific device subgroups covered by this datasheet.

Table 2. CY8C28xxx Device Characteristics

PSoC Part Number	CapSense	Digital Blocks	Regular Analog Blocks	Limited Analog Blocks	HW I^2C	Decimators	Digital I/O	Analog Inputs	Analog Outputs	Analog Mux Buses
CY8C28x03	N	12	0	0	2	0	up to 24	up to 8	0	0
CY8C28x13	Y	12	0	4	1	2	up to 40	up to 40	0	2
CY8C28x23	N	12	6	0	2	2	up to 44	up to 10	2	0
CY8C28x33	Y	12	6	4	1	4	up to 40	up to 40	2	2
CY8C28x43	N	12	12	0	2	4	up to 44	up to 44	4	2
CY8C28x45	Y	12	12	4	2	4	up to 44	up to 44	4	2
CY8C28x52	Y	8	12	4	1	4	up to 24	up to 24	4	2

Table 8. CY8C28x03 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#		80		RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W		81		RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW		82		RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#		83		RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#		84		RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W		85		RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW		86		RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#		87		RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
PRT4GS	12	RW		52			92			D2	
PRT4DM2	13	RW		53			93		IDX_PP	D3	RW
PRT5DR	14	RW		54			94		MVR_PP	D4	RW
PRT5IE	15	RW		55			95		MVW_PP	D5	RW
PRT5GS	16	RW		56			96		I2C0_CFG	D6	RW
PRT5DM2	17	RW		57			97		I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#		60			A0		INT_MSK0	E0	RW
DBC00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBC00DR2	22	RW		62			A2		INT_VC	E2	RC
DBC00CR0	23	#		63			A3		RES_WDT	E3	W
DBC01DR0	24	#		64			A4		I2C1_SCR	E4	#
DBC01DR1	25	W		65			A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW		66			A6			E6	
DBC01CR0	27	#	I2C1_DR	67	RW		A7			E7	
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RDI0RI	B0	RW		F0	
DBC10DR1	31	W		71		RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR0	33	#		73		RDI0LT0	B3	RW		F3	
DBC11DR0	34	#		74		RDI0LT1	B4	RW		F4	
DBC11DR1	35	W		75		RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR0	37	#		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RDI1RI	B8	RW		F8	
DCC12DR1	39	W		79		RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RDI1IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RDI1LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RDI1RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 11. CY8C28x13 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C	RW		CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW		60		GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW		61		GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW		62		GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW		63		GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW		64		RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW		66		RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW		67		RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW		69		SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74	RW	RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 15. CY8C28x33 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDIODSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

Table 20. CY8C28x52 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific. *Address has a dual purpose, see “Mapping Exceptions” on page 251

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 31. 5 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	20	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 0.5 × V_{DD} + 1.3 0.5 × V_{DD} + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 Ω to V_{DD}/2) Power = Low Power = High	 – –	 – –	 0.5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	53	64	–	dB	(0.5 × V_{DD} – 1.0) ≤ V_{OUT} ≤ (0.5 × V_{DD} + 0.9).

Table 32. 3.3 V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	20	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1 kΩ to $V_{DD}/2$) Power = Low Power = High	 – –	 – –	 $0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	 V V	
I_{SOB}	Supply current including bias cell (No Load) Power = Low Power = High	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	47	64	–	dB	$(0.5 \times V_{DD} - 1.0) \le V_{OUT} \le (0.5 \times V_{DD} + 0.9)$.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 34. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.214	$V_{DD}/2$ + 1.279	$V_{DD}/2$ + 1.341	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.018	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.01	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.301	$V_{DD}/2$ – 1.273	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 0.228	$V_{DD}/2$ + 1.284	$V_{DD}/2$ + 1.344	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.015	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.011	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.303	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.287	$V_{DD}/2$ + 1.345	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.275	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.014	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.012	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.328	$V_{DD}/2$ – 1.304	$V_{DD}/2$ – 1.276	V

Note
15. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 34. 5-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b111	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	3.2 × Bandgap	4.056	4.155	4.222	V
		V_{AGND}	AGND	1.6 × Bandgap	2.012	2.083	2.168	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.01	V_{SS} + 0.035	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	3.2 × Bandgap	4.061	4.153	4.223	V
		V_{AGND}	AGND	1.6 × Bandgap	2.023	2.082	2.145	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.022	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	3.2 × Bandgap	4.063	4.154	4.224	V
		V_{AGND}	AGND	1.6 × Bandgap	2.020	2.083	2.152	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	3.2 × Bandgap	4.061	4.154	4.225	V
		V_{AGND}	AGND	1.6 × Bandgap	2.026	2.081	2.140	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V

Table 35. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.223	$V_{DD}/2$ + 1.283	$V_{DD}/2$ + 1.343	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.013	$V_{DD}/2$ – 0.003	$V_{DD}/2$ + 0.005	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.270	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.345	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.008	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.005	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.271	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.232	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.008	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.006	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.272	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.233	$V_{DD}/2$ + 1.291	$V_{DD}/2$ + 1.347	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.006	$V_{DD}/2$	$V_{DD}/2$ + 0.006	V
		V_{REFLO}	Ref low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.322	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.272	V

Table 35. 3.3-V DC Analog Reference Specifications *(continued)*

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.045	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.016	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.019	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.023	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.036	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.013	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.021	P2[4] – P2[6] – 0.001	P2[4] – P2[6] + 0.021	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.034	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.013	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.023	P2[4] – P2[6] – 0.002	P2[4] – P2[6] + 0.016	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.033	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.014	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] – 0.003	P2[4] – P2[6] + 0.020	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.008	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.035	V_{DD}/2 – 0.001	V_{DD}/2 + 0.031	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.0165 V	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.035	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.031	V_{DD}/2 – 0.001	V_{DD}/2 + 0.028	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.012	V
	RefPower = Medium Opamp bias = High	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.044	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.052	V_{DD}/2	V_{DD}/2 + 0.046	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.014	V
	RefPower = Medium Opamp bias = Low	V_{REFHI}	Ref high	V_{DD}	V_{DD} – 0.036	V_{DD} – 0.004	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.032	V_{DD}/2	V_{DD}/2 + 0.029	V
		V_{REFLO}	Ref low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.012	V
0b011	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC IDAC Specifications

Table 39. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_INL	Integral nonlinearity	–5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_Gain	Gain per bit – Range 1 (91 µA)	283	357	447	nA	Measured at full scale
	Gain per bit – Range 2 (318 µA)	985	1250	1532	nA	
	Gain per bit – Range 3 (637 µA)	1959	2500	3056	nA	
IDACOffset	Offset at Code 0 vs LSB Ideal – Range 1 (91 µA)		2.0%	20%	%	Measured as a % of LSB (Current @ Code 0)/(LSB Ideal Current)
	Offset at Code 0 vs LSB Ideal – Range 2 (318 µA)		1.0%	10%	%	
	Offset at Code 0 vs LSB Ideal – Range 3 (637 µA)		1.0%	10%	%	

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices, for more information on the VLT_CR register.

Table 40. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} Value for PPOR Trip (positive ramp)					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0R}	PORLEV[1:0] = 00b	–	2.91	2.985	V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	4.49	V	
V_{PPOR2R}	PORLEV[1:0] = 10b	–	4.55	4.65	V	
	V_{DD} Value for PPOR Trip (negative ramp)					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.82	2.90	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	4.49	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.64	V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.83	2.91	3.00[16]	V	
V_{LVD1}	VM[2:0] = 001b	2.93	3.01	3.10	V	
V_{LVD2}	VM[2:0] = 010b	3.04	3.12	3.21	V	
V_{LVD3}	VM[2:0] = 011b	3.90	3.99	4.09	V	
V_{LVD4}	VM[2:0] = 100b	4.38	4.47	4.58	V	
V_{LVD5}	VM[2:0] = 101b	4.54	4.63	4.74[17]	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.71	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.80	4.92	V	
	V_{DD} Value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.93	3.01	3.10	V	
V_{PUMP1}	VM[2:0] = 001b	3.00	3.08	3.17	V	
V_{PUMP2}	VM[2:0] = 010b	3.16	3.24	3.33	V	
V_{PUMP3}	VM[2:0] = 011b	4.09	4.17	4.28	V	
V_{PUMP4}	VM[2:0] = 100b	4.53	4.62	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.61	4.71	4.82	V	
V_{PUMP6}	VM[2:0] = 110b	4.70	4.80	4.91	V	
V_{PUMP7}	VM[2:0] = 111b	4.88	4.98	5.10	V	

Notes
16. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
17. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 41. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	3	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply Voltage for Flash write operation	3	–	5.25	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.21	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000[18]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[19]	1,800,000	–	–	–	Erase/write cycles. Must be programmed and read at the same voltage to meet this.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Notes

18. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
19. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

Table 43. AC Chip-Level Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
t_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[24,25]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum Frequency of Signal on Row Input or Row Output.	–	–	12.3	MHz	
$SR_{POWERUP}$	Supply Ramp Time	0	–	–	µs	
$t_{POWERUP}$	Time for POR Release to Code Execution	–	16	100	ms	
t_{jit_IMO} [26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1300	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1300	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	200	800	ps	
t_{jit_PLL} [26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1100	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	400	2800	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	200	1400	ps	

Notes
24. 4.75 V < V_{DD} < 5.25 V.
25. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
26. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

AC Type-E Operational Amplifier Specifications

Table 47 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of the Limited Type E Analog PSoC blocks.

Table 47. AC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator Mode Response Time	–	75	100	ns	50 mV overdrive.

AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 48. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC Response Time	–	–	50	µs	≥ 50 mV overdrive.

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 50. 5 V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	2.5	µs	
	Power = High	–	–	2.9	µs	
t_{SOB}	Falling Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	2.3	µs	
	Power = High	–	–	2.3	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1 V Step, 100 pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1 V Step, 100 pF Load					
	Power = Low	0.65	–	–	V/µs	
	Power = High	0.65	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	0.8	–	–	MHz	
	Power = High	0.8	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1 V$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	300	–	–	kHz	
	Power = High	300	–	–	kHz	

Table 51. 3.3 V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	3.8	µs	
	Power = High	–	–	3.8	µs	
t_{SOB}	Falling Settling Time to 0.1%, 1 V Step, 100 pF Load					
	Power = Low	–	–	3.2	µs	
	Power = High	–	–	2.9	µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1 V Step, 100 pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1 V Step, 100 pF Load					
	Power = Low	0.5	–	–	V/µs	
	Power = High	0.5	–	–	V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	0.64	–	–	MHz	
	Power = High	0.64	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1 V$_{pp}$, 3dB BW, 100 pF Load					
	Power = Low	200	–	–	kHz	
	Power = High	200	–	–	kHz	

AC SAR10 ADC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 52. AC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{INSAR10}$	Input clock frequency for SAR10 ADC	–	–	2.0	MHz	
F_{SSAR10}	Sample rate for SAR10 ADC SAR10 ADC Resolution = 10 bits	–	–	142.9	ksps	For 10-bit resolution, the sample rate is the ADC's input clock divided by 14.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 53. 5 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power-up IMO to Switch	150	–	–	µs	

Table 54. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1[28]	0.093	–	12.3	MHz	
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater[29]	0.186	–	24.6	MHz	
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to Switch	150	–	–	µs	

Notes
28. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
29. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

Acronyms

Acronyms Used

Table 61 lists the acronyms that are used in this document.

Table 61. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC®	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SLIMO	slow IMO
IMO	internal main oscillator	SMP	switch mode pump
I/O	input/output	SOIC	small-outline integrated circuit
IrDA	infrared data association	SPI™	serial peripheral interface
ISSP	in-system serial programming	SRAM	static random access memory
LCD	liquid crystal display	SROM	supervisory read only memory
LED	light-emitting diode	SSOP	shrink small-outline package
LPC	low power comparator	UART	universal asynchronous receiver / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 available at http://www.cypress.com.

Document Conventions

Units of Measure

Table 62 lists the unit sof measures.

Table 62. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	µs	microsecond
dB	decibels	ms	millisecond
°C	degree Celsius	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	µV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohm	V	volts
Ω	ohm	µW	microwatts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
mH	millihenry		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	5. A logic signal having its asserted state as the logic 1 state. 6. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.