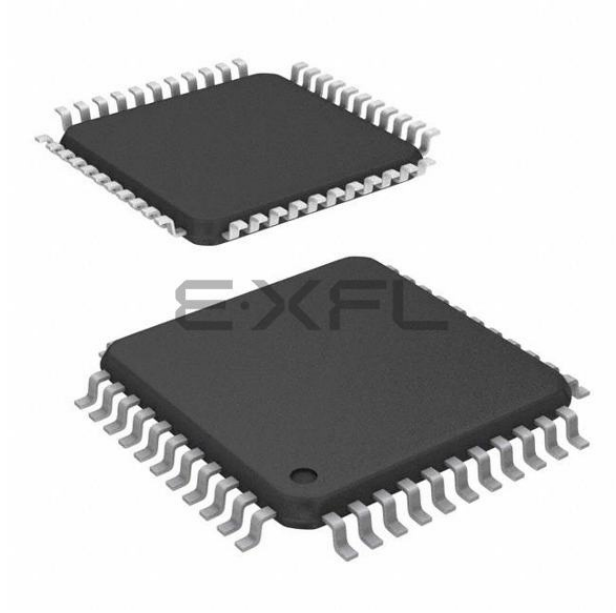
Analog Devices Inc./Maxim Integrated - DS89C440-ENL Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds89c440-enl

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……..-0.3V to +6.0V
Ambient Temperature Range (under bias)……-40°C to +85°C
Storage Temperature Range……-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (Notes 2, 3)	V_{CC}	4.5	5.0	5.5	V
Power-Fail Warning (Notes 2, 4)	V_{PFW}	4.2	4.375	4.6	V
Reset Trip Point (Min Operating Voltage) (Notes 2, 3, 4)	V_{RST}	3.95	4.125	4.35	V
Supply Current, Active Mode (Note 5)	I_{CC}		75	110	mA
Supply Current, Idle Mode at 33MHz (Note 6)	I_{IDLE}		40	50	mA
Supply Current, Stop Mode, Bandgap Disabled (Note 7)	I_{STOP}		1	100	μA
Supply Current, Stop Mode, Bandgap Enabled (Note 7)	I_{SPBG}		150	300	μA
Input Low Level (Note 2)	V_{IL}	-0.3		+0.8	V
Input High Level (Note 2)	V_{IH}	2.0		V_{CC} + 0.3	V
Input High Level XTAL and RST (Note 2)	V_{IH2}	3.5		V_{CC} + 0.3	V
Output Low Voltage, Port 1 and 3 at I_{OL} = 1.6mA (Note 2)	V_{OL1}		0.15	0.45	V
Output Low Voltage, Port 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA (Note 2)	V_{OL2}		0.15	0.45	V
Output High Voltage, Port 1, 2, and 3, at I_{OH} = -50μA (Notes 2, 8)	V_{OH1}	2.4			V
Output High Voltage, Port 1, 2, and 3 at I_{OH} = -1.5mA (Notes 2, 9)	V_{OH2}	2.4			V
Output High Voltage, Port 0, 1, 2, ALE, $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$ in Bus Mode at I_{OH} = -8mA (Notes 2, 10)	V_{OH3}	2.4			V
Output High Voltage, RST at I_{OL} = -0.4mA (Note 2, 11)	V_{OH4}	2.4			V
Input Low Current, Port 1, 2, and 3 at 0.4V	I_{IL}	-50			μA
Transition Current from 1 to 0, Port 1, 2, and 3 at 2V (Note 12)	I_{TL}	-650			μA
Input Leakage Current, Port 0 in I/O Mode and $\overline{EA}$ (Note 13)	I_L	-10		+10	μA
Input Current, Port 0 in Bus Mode (Note 14)	I_L	-300		+300	μA
RST Pulldown Resistance (Note 13)	R_{RST}	50	120	200	kΩ

AC CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (See Figure 1, Figure 2, and Figure 3.)

PARAMETER	SYMBOL	1-CYCLE PAGE MODE 1		2-CYCLE PAGE MODE 1		4-CYCLE PAGE MODE 1		PAGE MODE 2		NONPAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Port 0 Address to Valid Data In (Note 16)	t_{AVDV0}								$3t_{CLCL}$ - 20 + t_{STC1}		$3t_{CLCL}$ - 20 + t_{STC1}	ns
Port 2 Address to Valid Data In (Note 16)	t_{AVDV2}		t_{CLCL} - 20 + t_{STC1}		$1.5t_{CLCL}$ - 20 + t_{STC1}		$3.5t_{CLCL}$ - 20 + t_{STC1}		$3.0t_{CLCL}$ - 20 + t_{STC1}		$3.5t_{CLCL}$ - 20 + t_{STC1}	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{LLRL} (t_{LLWL})	$0.5t_{CLCL}$ - 8 + t_{STC2}	$0.5t_{CLCL}$ + 6 + t_{STC2}	$2t_{CLCL}$ - 8 + t_{STC2}	$2t_{CLCL}$ + 6 + t_{STC2}	$4t_{CLCL}$ - 8 + t_{STC2}	$4t_{CLCL}$ + 6 + t_{STC2}	$0.5t_{CLCL}$ - 8 + t_{STC2}	$0.5t_{CLCL}$ + 4 + t_{STC2}	$0.5t_{CLCL}$ - 8 + t_{STC2}	$0.5t_{CLCL}$ + 5 + t_{STC2}	ns
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{AVRL0} (t_{AVWL0})							$1.5t_{CLCL}$ - 5 + t_{STC2}		t_{CLCL} - 5 + t_{STC2}		ns
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{AVRL2} (t_{AVWL2})	0 + t_{STC5} - 5		$0.5t_{CLCL}$ - 5 + t_{STC5}		$1.5t_{CLCL}$ - 5 + t_{STC5}		t_{CLCL} - 5 + t_{STC5}		$1.5t_{CLCL}$ - 5 + t_{STC5}		ns
Data Out Valid to $\overline{WR}$ Transition (Note 15)	t_{QVWX}	-5		-5		-5		-5		-5		ns
Data Hold After $\overline{WR}$ (Note 15)	t_{WHQX}	t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High (Note 15)	t_{RHLH} (t_{WHLH})	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	ns

Note: Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator and are not 100% tested, but are guaranteed by design.

Note 15: The clock divide and crystal multiplier control bits in the PMR register determine the system clock frequency and the minimum/maximum external clock speed. The term "$1/t_{CLCL}$" used in the *AC Characteristics* variable timing table is determined from the following table. The minimum/maximum external clock speed columns clarify that [(external clock speed) x (multipliers)] cannot exceed the rated speed of the device. In addition, the use of the crystal multiplier feature establishes a minimum external speed.

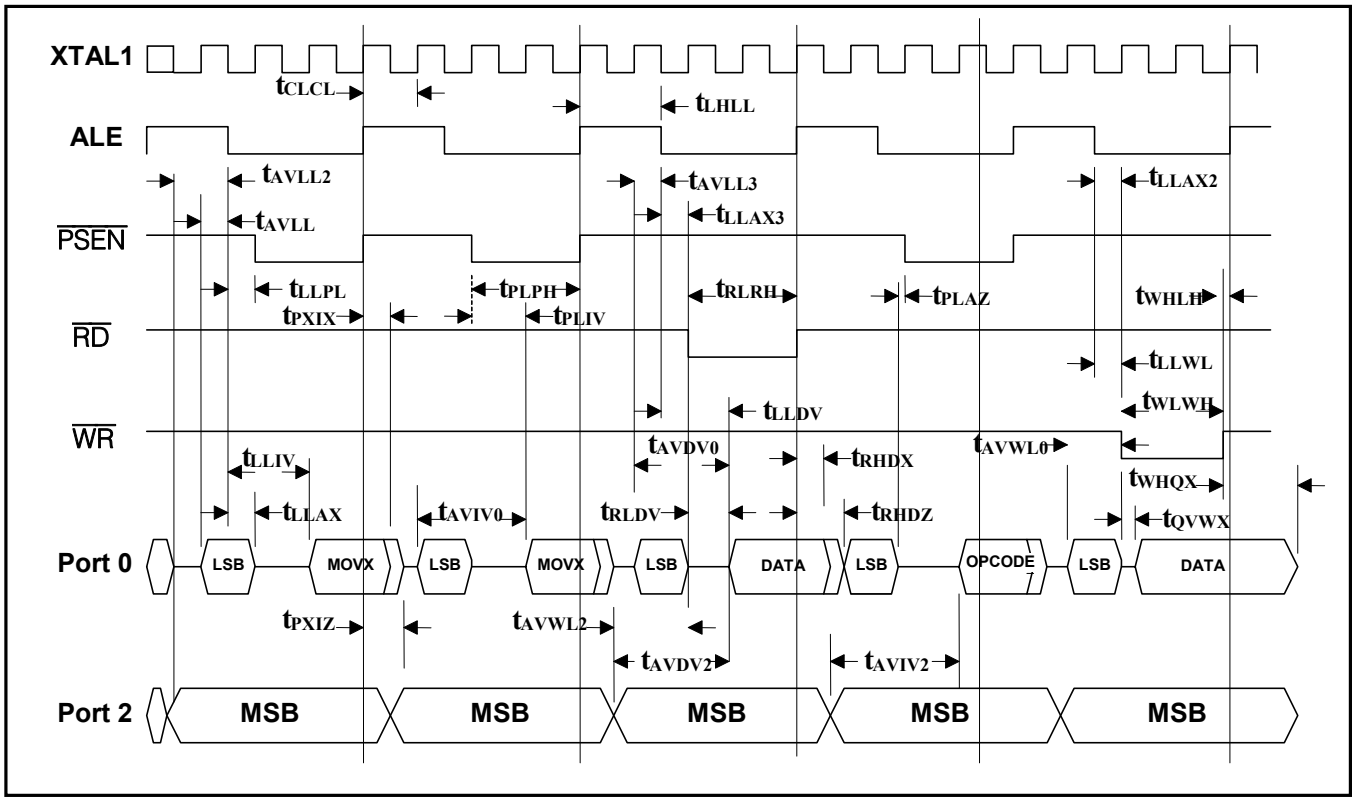
4X/$\overline{2X}$	CD1	CD0	Number of External Clock Cycles per System Clock ($1/t_{CLCL}$)	External Clock Speed	
				Min	Max
1	0	0	1/4	5MHz	8.25MHz
0	0	0	1/2	10MHz	16.5MHz
X	0	1	Reserved	—	—
X	1	0	1	See AC Characteristics	See AC Characteristics
X	1	1	1024	See AC Characteristics	See AC Characteristics

Note 16: External MOVX instruction times are dependent upon the setting of the MD2, MD1, and MD0 bits in the clock control register. The terms "t_{STC1}, t_{STC2}, t_{STC3}" used in the variable timing table above are calculated through the use of the table given below.

MD2	MD1	MD0	MOVX Instruction Time	t_{STC1}	t_{STC2}	t_{STC3}	t_{STC4}	t_{STC5}
0	0	0	2 Machine Cycles	0 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}
0	0	1	3 Machine Cycles	2 t_{CLCL}	1 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	1 t_{CLCL}
0	1	0	4 Machine Cycles	6 t_{CLCL}	1 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	1 t_{CLCL}
0	1	1	5 Machine Cycles	10 t_{CLCL}	1 t_{CLCL}	0 t_{CLCL}	0 t_{CLCL}	1 t_{CLCL}
1	0	0	6 Machine Cycles	14 t_{CLCL}	5 t_{CLCL}	4 t_{CLCL}	1 t_{CLCL}	1 t_{CLCL}
1	0	1	7 Machine Cycles	18 t_{CLCL}	5 t_{CLCL}	4 t_{CLCL}	1 t_{CLCL}	1 t_{CLCL}
1	1	0	8 Machine Cycles	22 t_{CLCL}	5 t_{CLCL}	4 t_{CLCL}	1 t_{CLCL}	1 t_{CLCL}
1	1	1	9 Machine Cycles	26 t_{CLCL}	5 t_{CLCL}	4 t_{CLCL}	1 t_{CLCL}	1 t_{CLCL}

Note 17: Maximum load capacitance (to meet the above timing) for Port 0, ALE, $\overline{PSEN}$, $\overline{WR}$, and $\overline{RD}$ is limited to 60pF. XTAL1 and XTAL2 load capacitance are dependent upon the frequency of the selected crystal.

Figure 1. Nonpage Mode Timing



EXTERNAL CLOCK CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Clock High Time	t_{CHCX}	10		ns
Clock Low Time	t_{CLCX}	10		ns
Clock Rise Time	t_{CLCH}		5	ns
Clock Fall Time	t_{CHCL}		5	ns

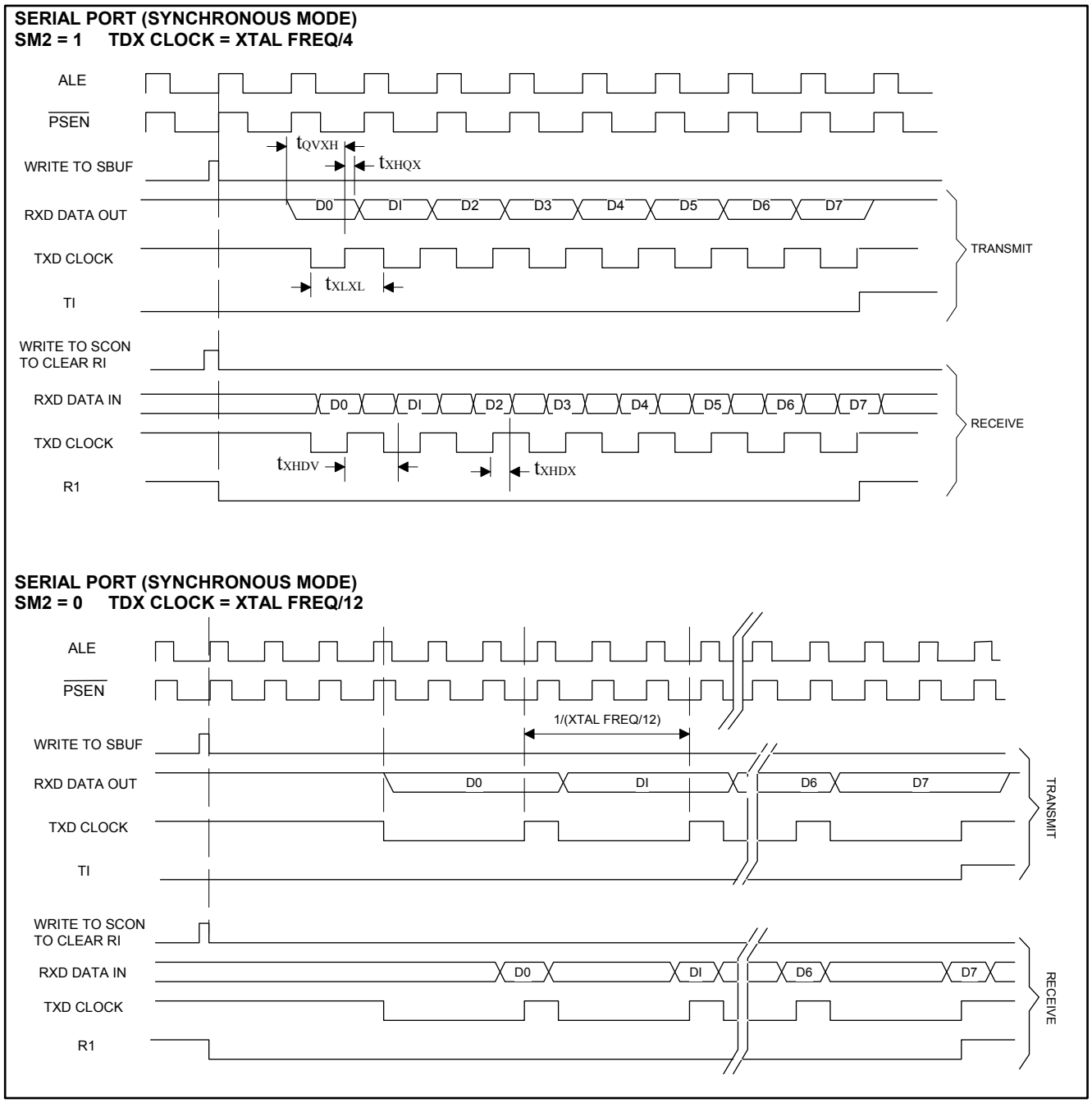
SERIAL PORT MODE 0 TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (Figure 4)

PARAMETER	SYMBOL	CONDITIONS	33MHz		VARIABLE		UNITS
			MIN	MAX	MIN	MAX	
Clock Cycle Time	t_{XLXL}	SM2 = 0	360		$12t_{CLCL}$		ns
		SM2 = 1	120		$4t_{CLCL}$		ns
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0	200		$10t_{CLCL}$ - 100		ns
		SM2 = 1	40		$3t_{CLCL}$ - 10		ns
Output Data Hold to Clock Rising	t_{XHQX}	SM2 = 0	50		$2t_{CLCL}$ - 10		ns
		SM2 = 1	20		t_{CLCL} - 100		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0	0		0		ns
		SM2 = 1	0		0		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0		200		$10t_{CLCL}$ - 100	ns
		SM2 = 1		40		$3t_{CLCL}$ - 50	ns

Note: SM2 is the serial port 0 mode bit 2. When serial port 0 is operating in mode 0 (SM0 = SM1 = 0), SM2 determines the number of crystal clocks in a serial port clock cycle.

Figure 4. Serial Port Timing



POWER-CYCLE TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Startup Time (Note 18)	t_{CSU}		8		ms
Power-On Reset Delay (Note 19)	t_{POR}		65,536		t_{CLCL}

Note 18: Startup time for a crystal varies with load capacitance and manufacturer. The time shown is for an 11.0592MHz crystal manufactured by Fox Electronics.

Note 19: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

FLASH MEMORY PROGRAMMING CHARACTERISTICS

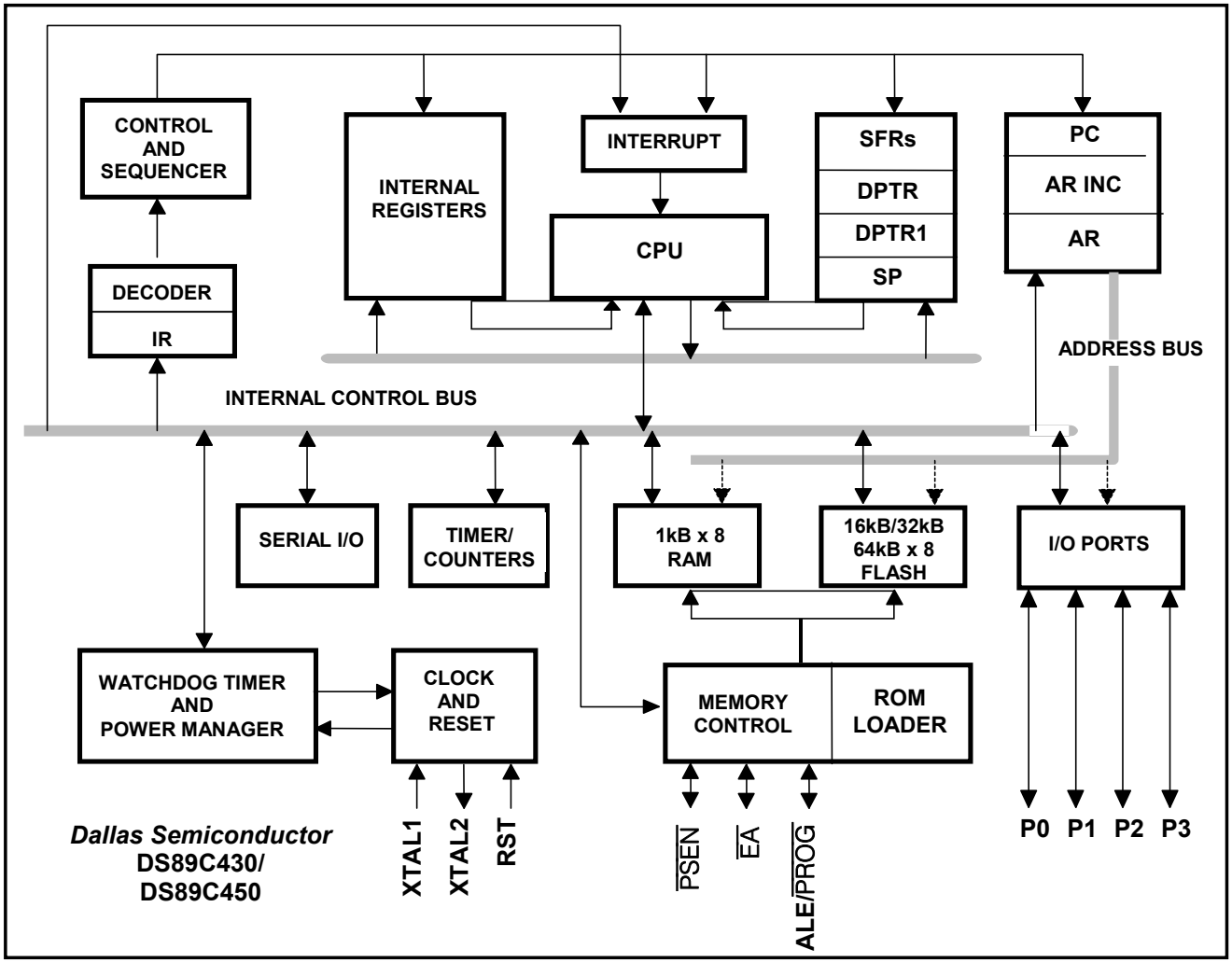
(V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data Retention	t_{DR}	100			years
Write/Erase Endurance	t_{ENDURE}	10,000			cycles
Program/Time	t_{PROG}			40	µs
Erase Time	t_{ERASE}	4			ms

PIN DESCRIPTION

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
40	12, 44	6, 38	V_{CC}	**+5V**
20	1, 22, 23, 34	16, 17, 28, 39	GND	**Logic Ground**
9	10	4	RST	**External Reset.** The RST input pin is bidirectional and contains a Schmitt Trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, as the device provides this function internally.
19	21	15	XTAL1	**Crystal Oscillators.** These pins provide support for fundamental-mode parallel-resonant AT-cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
18	20	14	XTAL2	
29	32	26	$\overline{PSEN}$	**Program Store Enable.** This signal is commonly connected to optional external program memory as a chip enable. $\overline{PSEN}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In one-cycle page mode 1, $\overline{PSEN}$ remains low for consecutive page hits.
30	33	27	ALE/$\overline{PROG}$	**Address Latch Enable.** This signal functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373-family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{PROG}$) is used to execute the parallel program function.
39	43	37	P0.0 (AD0)	**Port 0 (AD0–AD7), I/O.** Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of port 0 is tri-state. Pullup resistors are required only when using port 0 as an I/O port.
38	42	36	P0.1 (AD1)	
37	41	35	P0.2 (AD2)	
36	40	34	P0.3 (AD3)	
35	39	33	P0.4 (AD4)	
34	38	32	P0.5 (AD5)	
33	37	31	P0.6 (AD6)	
32	36	30	P0.7 (AD7)	

Figure 5. Functional Diagram



DETAILED DESCRIPTION

The DS89C430 and DS89C450 are pin compatible with all three packages of the standard 8051 and include standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. The three part numbers vary only by the amount of internal flash memory (DS89C430 = 16kB, DS89C450 = 64kB), which can be in-system/in-application programmed from a serial port using ROM-resident or user-defined loader software. For volume deployments, the flash can also be loaded externally using standard commercially available parallel programmers.

Besides greater speed, the DS89C430/DS89C450 include 1kB of data RAM, a second full hardware serial port, seven additional interrupts, two extra levels of interrupt priority, programmable watchdog timer, brownout monitor, and power-fail reset. Dual data pointers (DPTRs) are included to speed up block data-memory moves with further enhancements coming from selectable automatic increment/decrement and toggle select operation. The speed of MOVX data memory access can be adjusted by adding stretch values up to 10 machine cycles for flexibility in selecting external memory and peripherals.

A power management mode consumes significantly lower power by slowing the CPU execution rate from one clock period per cycle to 1024 clock periods per cycle. A selectable switchback feature can automatically cancel this mode to enable normal speed responses to interrupts.

For EMI-sensitive applications, the microcontroller can disable the ALE signal when the processor is not accessing external memory.

All standard SFR locations from the 8051 are duplicated in the DS89C430, and several SFRs have been added for the unique features of the DS89C430. Most of these features are controlled by bits in SFRs located in unused locations in the 8051 SFR map, allowing for increased functionality while maintaining complete instruction set compatibility. Table 1 shows the SFRs and their locations. Table 2 specifies the default reset condition for all SFR bits.

Data Pointers

The data pointers (DPTR and DPTR1) are used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM location (on-chip or off-chip) or a memory-mapped peripheral. Two pointers are useful when moving data from one memory area to another, or when using a memory-mapped peripheral for both source and destination addresses. The user can select the active pointer through a dedicated SFR bit (SEL = DPS.0), or can activate an automatic toggling feature for altering the pointer selection (TSL = DPS.5). An additional feature, if selected, provides automatic incrementing or decrementing of the current DPTR.

Stack Pointer

The stack pointer denotes the register location at the top of the stack, which is the last used value. The user can place the stack anywhere in the scratchpad RAM by setting the stack pointer to the desired location, although the lower bytes are normally used for working registers.

I/O Ports

The DS89C430 offers four 8-bit I/O ports. Each I/O port is represented by an SFR location and can be written or read. The I/O port has a latch that contains the value written by software.

Counter/Timers

Three 16-bit timer/counters are available in the DS89C430. Each timer is contained in two SFR locations that can be read or written by software. The timers are controlled by other SFRs, described in the *SFR Bit Description* section of the *Ultra-High-Speed Flash Microcontroller User's Guide*.

Serial Ports

The DS89C430 provides two UARTs that are controlled and accessed by SFRs. Each UART has an address that is used to read and write the value contained in the UART. The same address is used for both read and write operations, and the read and write operations are distinguished by the instruction. Its own SFR control register controls each UART.

Table 1. SFR Register Map

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
SP	81h								
DPL	82h								
DPH	83h								
DPL1	84h								
DPH1	85h								
DPS	86h	ID1	ID0	TSL	AID	—	—	—	SEL
PCON	87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TL0	8Ah								
TL1	8Bh								
TH0	8Ch								

Table 2. SFR Reset Value

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	1	1	1	1	1	1	1	1
SP	81h	0	0	0	0	0	1	1	1
DPL	82h	0	0	0	0	0	0	0	0
DPH	83h	0	0	0	0	0	0	0	0
DPL1	84h	0	0	0	0	0	0	0	0
DPH1	85h	0	0	0	0	0	0	0	0
DPS	86h	0	0	0	0	0	1	0	0
PCON	87h	0	0	Special	Special	0	0	0	0
TCON	88h	0	0	0	0	0	0	0	0
TMOD	89h	0	0	0	0	0	0	0	0
TL0	8Ah	0	0	0	0	0	0	0	0
TL1	8Bh	0	0	0	0	0	0	0	0
TH0	8Ch	0	0	0	0	0	0	0	0
TH1	8Dh	0	0	0	0	0	0	0	0
CKCON	8Eh	0	0	0	0	0	0	0	1
P1	90h	1	1	1	1	1	1	1	1
EXIF	91h	0	0	0	0	Special	Special	Special	0
CKMOD	96h	1	1	0	0	0	1	1	1
SCON0	98h	0	0	0	0	0	0	0	0
SBUF0	99h	0	0	0	0	0	0	0	0
ACON	9Dh	0	0	0	1	1	1	1	1
P2	A0h	1	1	1	1	1	1	1	1
IE	A8h	0	0	0	0	0	0	0	0
SADDR0	A9h	0	0	0	0	0	0	0	0
SADDR1	AAh	0	0	0	0	0	0	0	0
P3	B0h	1	1	1	1	1	1	1	1
IP1	B1h	1	0	0	0	0	0	0	0
IP0	B8h	1	0	0	0	0	0	0	0
SADEN0	B9h	0	0	0	0	0	0	0	0
SADEN1	BAh	0	0	0	0	0	0	0	0
SCON1	C0h	0	0	0	0	0	0	0	0
SBUF1	C1h	0	0	0	0	0	0	0	0
ROMSIZE	C2h	1	1	1	1	0	1	0	1
PMR	C4h	1	0	0	0	0	0	0	0
STATUS	C5h	0	0	0	1	0	0	0	0
TA	C7h	1	1	1	1	1	1	1	1
T2CON	C8h	0	0	0	0	0	0	0	0
T2MOD	C9h	1	1	1	1	1	1	0	0
RCAP2L	CAh	0	0	0	0	0	0	0	0
RCAP2H	CBh	0	0	0	0	0	0	0	0

Table 2. SFR Reset Value (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TL2	CCh	0	0	0	0	0	0	0	0
TH2	CDh	0	0	0	0	0	0	0	0
PSW	D0h	0	0	0	0	0	0	0	0
FCNTL	D5h	1	0	1	1	0	0	0	0
FDATA	D6h	0	0	0	0	0	0	0	0
WDCON	D8h	0	Special	0	Special	0	Special	Special	0
ACC	E0h	0	0	0	0	0	0	0	0
EIE	E8h	1	1	1	0	0	0	0	0
B	F0h	0	0	0	0	0	0	0	0
EIP1	F1h	1	1	1	0	0	0	0	0
EIP0	F8h	1	1	1	0	0	0	0	0

Note: Consult the *Ultra-High-Speed Flash Microcontroller User's Guide* for more information about the bits marked "Special."

Memory Organization

There are three distinct memory areas in the DS89C430: scratchpad registers, program memory, and data memory. The registers are located on-chip but the program and data memory spaces can be on-chip, off-chip, or both. The DS89C430/DS89C450 have 16kB/64kB of on-chip program memory, respectively, implemented in flash memory and also have 1kB of on-chip data memory space that can be configured as program space using the PRAME bit in the ROMSIZE feature. The DS89C430 uses a memory-addressing scheme that separates program memory from data memory. The program and data segments can be overlapped since they are accessed in different manners. If the maximum address of on-chip program or data memory is exceeded, the DS89C430 performs an external memory access using the expanded memory bus. The $\overline{PSEN}$ signal goes active low to serve as a chip enable or output enable when performing a code fetch from external program memory. MOVX instructions activate the $\overline{RD}$ or $\overline{WR}$ signal for external MOVX data memory access. The program memory ROMSIZE feature allows software to dynamically configure the maximum address of on-chip program memory. This allows the DS89C430 to act as a bootloader for an external memory. It also enables the use of the overlapping external program spaces. The lower 128 bytes of on-chip flash memory—if ROMSIZE is greater than 0—are used to store reset and interrupt vectors. 256 bytes of on-chip RAM serve as a register area and program stack, which are separated from the data memory.

Register Space

Registers are located in the 256 bytes of on-chip RAM labeled "internal registers" (Figure 6), which can be divided into two sub areas of 128 bytes each. Separate classes of instructions are used to access the registers and the program/data memory. The upper 128 bytes are overlapped with the 128 bytes of SFRs in the memory map. Indirect addressing is used to access the upper 128 bytes of scratchpad RAM, while the SFR area is accessed using direct addressing. The lower 128 bytes can be accessed using direct or indirect addressing.

There are four banks of eight working registers in the lower 128 bytes of scratchpad RAM. The working registers are general-purpose RAM locations that can be addressed within the selected bank by any instructions that use R0–R7. The register bank selection is controlled through the program status register in the SFR area. The contents of the working registers can be used for indirect addressing of the upper 128 bytes of scratchpad RAM.

Individually addressable bits in the RAM and SFR areas support Boolean operations. In the scratchpad RAM area, registers 20h–2Fh are bit addressable by software using Boolean operation instructions.

Another use of the scratchpad RAM area is for the stack. The stack pointer, contained in the SFRs, is used to select storage locations for program variables and for return addresses of control operations.

fetch that takes four clocks. Page mode 1 is the only external addressing mode where the CPU does not require stalls for external memory access, but page misses result in reduced external access performance.

On-Chip Program Memory

The processor can fetch the entire on-chip program memory range automatically. By default, the reset routines and all interrupt vectors are located in the lower 128 bytes of the on-chip program memory.

On-chip program memory is logically divided into pairs of 8kB, 16kB, or 32kB flash memory banks to support in-application programming. The upper block of the on-chip program memory is designed to be programmed in-application with the standard 5V V_{CC} supply under the control of the user software or by using a built-in program memory loader. It can also be programmed in standard flash or EPROM programmers. The DS89C430 incorporates a memory management unit (MMU) and other hardware to support any of the three programming methods. The MMU controls program and data memory access, and provides sequencing and timing controls for programming of the on-chip program memory. A separate security flash block supports a three-level lock, a 64-byte encryption array, and other flash options.

Security Features

The DS89C430 incorporates a 64-byte encryption array, allowing the user to verify program codes while viewing the data in encrypted form. The encryption array is implemented in a security flash memory block that has the same electrical and timing characteristics as the on-chip program memory. Once the encryption array is programmed to non-FFh, the data presented in the verify mode is encrypted. Each byte of data is XNORed with a byte in the encryption array during verification.

A three-level lock restricts viewing of the internal program and data memory contents. By programming the three lock bits, the user can select a level of security as specified in Table 3. The protection levels function differently than those in a traditional 8051 microcontroller, and should not be used while executing external code.

Once a security level is selected and programmed, the setting of the lock bits remains. Only a mass erase can erase these bits and allow reprogramming the security level to a less restricted protection.

Table 3. Flash Memory Lock Bits

LEVEL	LB1	LB2	LB3	PROTECTION
1	1	1	1	No program lock. Encrypted verify if encryption array is programmed. Do not execute external program code while operating at this security level.
2	0	1	1	Prevent MOVC in external memory from reading program code in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further parallel or program memory loader programming. Do not execute external program code while operating at this security level.
3	X	0	1	Level 2 plus no verify operation. Also prevent MOVX in external memory from reading internal SRAM. Do not execute external program code while operating at this security level.
4	X	X	0	Level 3 plus no external execution.

The DS89C430 provides user-selectable options that must be set before beginning software execution. The option control register uses flash bits rather than SFRs, and is individually erasable and programmable as a byte-wide register. Bit 3 of this register is defined as the watchdog POR. Setting this bit to 1 disables the watchdog reset function on power-up. Clearing this bit to 0 enables the watchdog reset function automatically. Other bits of this register are undefined and are at logic 1 when read. The value of this register can be read at address FCh in parallel programming mode or executing a verify-option-control register instruction in ROM loader mode or in-application programming mode.

Table 4. In-Application Programming Commands

FC3:FC0	COMMAND	OPERATION
0000	Read Mode	Default state. All flash blocks are in read mode. **Note:** The upper bank of flash memory is inaccessible for execution unless the FC3:0 bits are in the read mode (0000b) state.
0001	Verify Option Control Register	Read data from the option control register. Data is available in the FDATA at the end of the following machine cycle. FDATA.3 is the logic value of the watchdog POR default setting.
0010	Verify Security Block	Read a byte of data from the security block. After the address byte is written to the FDATA, data is available in the FDATA at the end of the following machine cycle. (Lock bits are addressed at 40h and FDATA.5:3 are the logic value of LB1, LB2 and LB3, respectively.)
0011	Verify Upper Program Memory Bank	Read a byte of data from upper flash memory bank (address range from 2000h to 3FFFh). The first and second byte writes to the FDATA are the upper and lower byte of the address. Data is available in the FDATA at the end of the following machine cycle after the second address byte is written.
0100	Reserved for Future Use	This command should not be modified by user programs.
1000	Reserved for Future Use	This command should not be modified by user programs.
1001	Write Option Control Register	Write to the option control register as data is written to FDATA. Bit 3 of the data byte represents the watchdog POR default setting.
1010	Write Security Block	Write a byte of data to the security block at a selected locations addressed by the first byte write to the FDATA. The second write to the FDATA is the data byte. (Lock bits are addressed at 40h and the FDATA 5:3 represents lock bits LB3, LB2, and LB1, respectively.)
1011	Write Upper Program Memory Bank	Write a byte of code to the upper flash memory bank (address range from 2000h to 3FFFh). The first and second byte writes to the FDATA are the upper byte and the lower byte of the address. The third write to the FDATA is the data byte.
1100	Erase Option Control Register	Erase the option control register. The contents of this register are returned to FFh. This operation disables the watchdog reset function on power-up.
1101	Erase Security Block	Erase the security flash block that contains the 64-byte encryption array and the lock bits. The content of every memory location is turned into FFh.
1110	Erase Upper Program Memory Bank	Erase the upper bank of flash memory bank. The contents of every memory location are returned to FFh.
1111	System Reset	This command is used to cause a system reset.

The flash command bits are cleared to 0 on all forms of reset, and it is important for the user software to clear these bits to 0 to return the flash memory to read mode from erase/program operation. This setting is a “no operation” condition for the MMU, which allows the processor to return to its normal execution. Note that the busy and error flags have no function in normal flash-read mode.

The FCNTL SFR can only be written using timed access. This procedure provides protection against inadvertent erase/program operation on the flash memory. Any command written to the FCNTL during a flash operation is ignored (FBUSY = 0). To ensure data integrity, an erase command sequence should be reinitiated if an erase or program operation is interrupted by a reset.

ROM Loader

The full on-chip flash program memory space, security flash block, and external SRAM can be programmed in-system from an external source through serial port 0 under the control of a built-in ROM loader. The ROM loader also has an auto-baud feature that determines which baud-rate frequencies are being used for communication and sets the baud-rate generator for that speed.

When the DS89C430 is powered up and has entered its user operating mode, the ROM loader mode can be invoked at any time by forcing RST = 1, $\overline{EA}$ = 0, and $\overline{PSEN}$ = 0. It remains in effect until power-down or when the condition (RST = 1 and $\overline{PSEN}$ = $\overline{EA}$ = 0) is removed. Entering the ROM loader mode forces the processor to start fetching from the 2kB internal ROM for program memory initialization and other loader functions.

The read/write accessibility is determined by the state of the lock bits, which can be verified directly by the ROM loader.

The flash memory can be programmed (by the built-in ROM loader) using commands that are received over the serial interface from a host PC. Full details of the ROM loader commands are given in the *Ultra-High-Speed Flash Microcontroller User's Guide*. Host software to communicate with the ROM loader is available in Windows® format as well as other platforms. Contact our technical support department at www.maxim-ic.com/support for more information.

Parallel Programming Mode

The microcontroller also supports a programming mode such as that used by commercial device programmers. This mode is of little utility in normal applications and is only used by commercial device programmers. For information on this mode, contact our technical support department.

Data Pointer Increment/Decrement and Options

The DS89C430 incorporates a hardware feature to assist applications that require data pointer increment/decrement. Data pointer increment/decrement bits ID0 and ID1 (DPS.6 and DPS.7) define how the INC DPTR instruction functions in relation to the active DPTR (selected by the SEL bit). Setting ID0 = 1 and SEL = 0 enables the decrement operation for DPTR, and execution of the INC DPTR instruction decrements the DPTR contents by 1. Similarly, setting ID1 = 1 and SEL = 1 enables the decrement operation for DPTR1, and execution of the INC DPTR instruction decrements the DPTR1 contents by 1. With this feature, the user can configure the data pointers to operate in four ways for the INC DPTR instruction:

ID1	ID0	SEL = 0	SEL = 1
0	0	INC DPTR	INC DPTR1
0	1	DEC DPTR	INC DPTR1
1	0	INC DPTR	DEC DPTR1
1	1	DEC DPTR	DEC DPTR1

SEL (DPS.0) bit always selects the active data pointer. The DS89C430 offers a programmable option that allows any instructions related to data pointer to toggle the SEL bit automatically. This option is enabled by setting the toggle-select-enable bit (TSL–DPS.5) to a logic 1. Once enabled, the SEL bit is automatically toggled *after* the execution of one of the following five DPTR-related instructions:

```
INC DPTR
MOV DPTR #data16
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

The DS89C430 also offers a programmable option that automatically increases (or decreases) the contents of the selected data pointer by 1 *after* the execution of a DPTR-related instruction. The actual function (increment or decrement) is dependent on the setting of the ID1 and ID0 bits. This option is enabled by setting the automatic increment/decrement enable (AID–DPS.4) to a logic 1 and is affected by the following three instructions:

```
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

Windows is a registered trademark of Microsoft Corporation.

Figure 8. Nonpage Mode, External Data Memory Access (Stretch = 0, CD1:CD2 = 10)

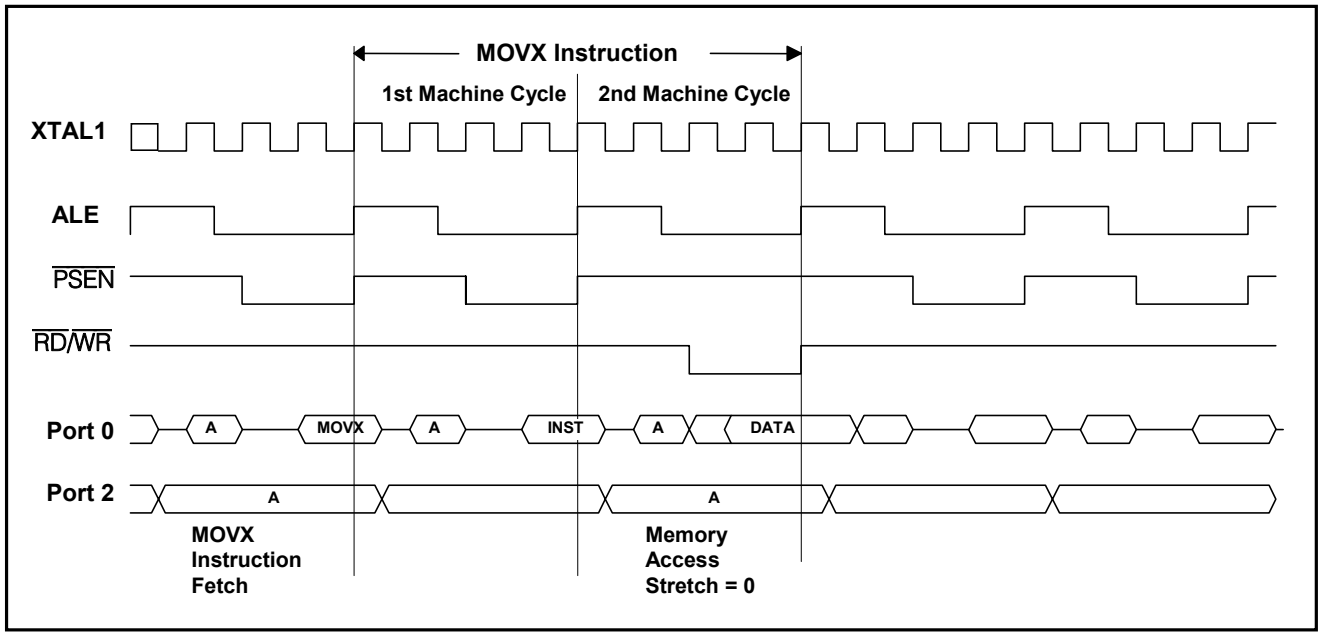


Figure 9. Nonpage Mode, External Data Memory Access (Stretch = 1, CD1:CD2 = 10)

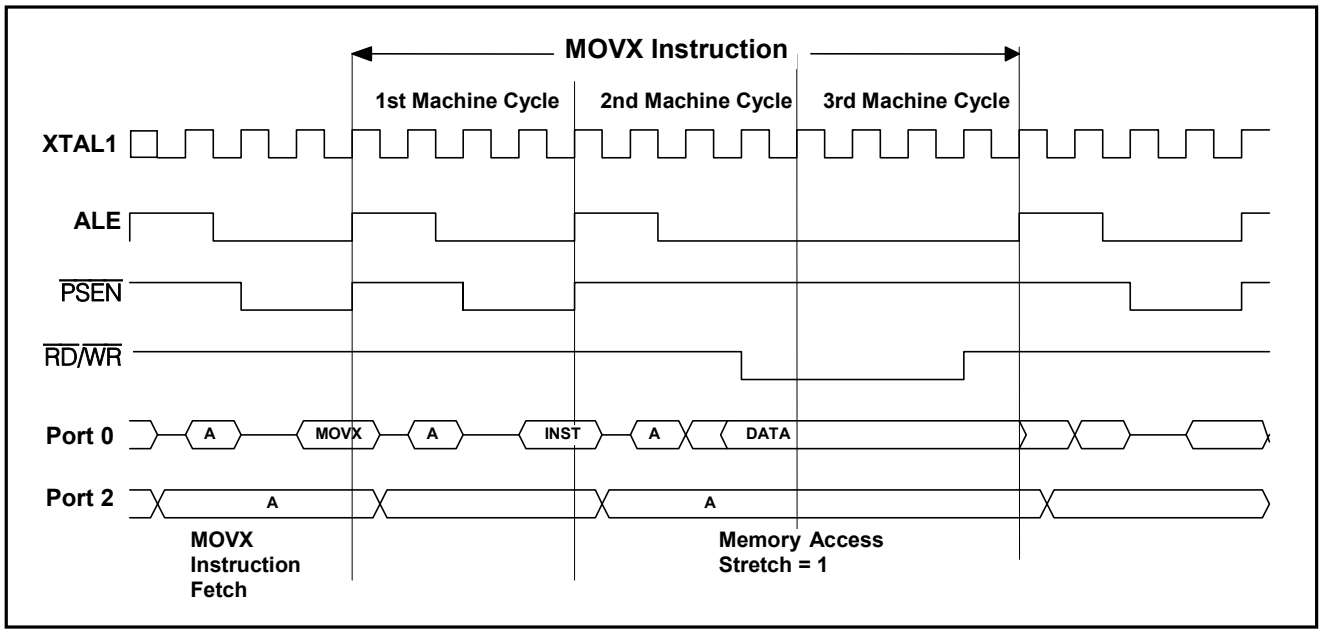


Table 10. Page Mode 2, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 11)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

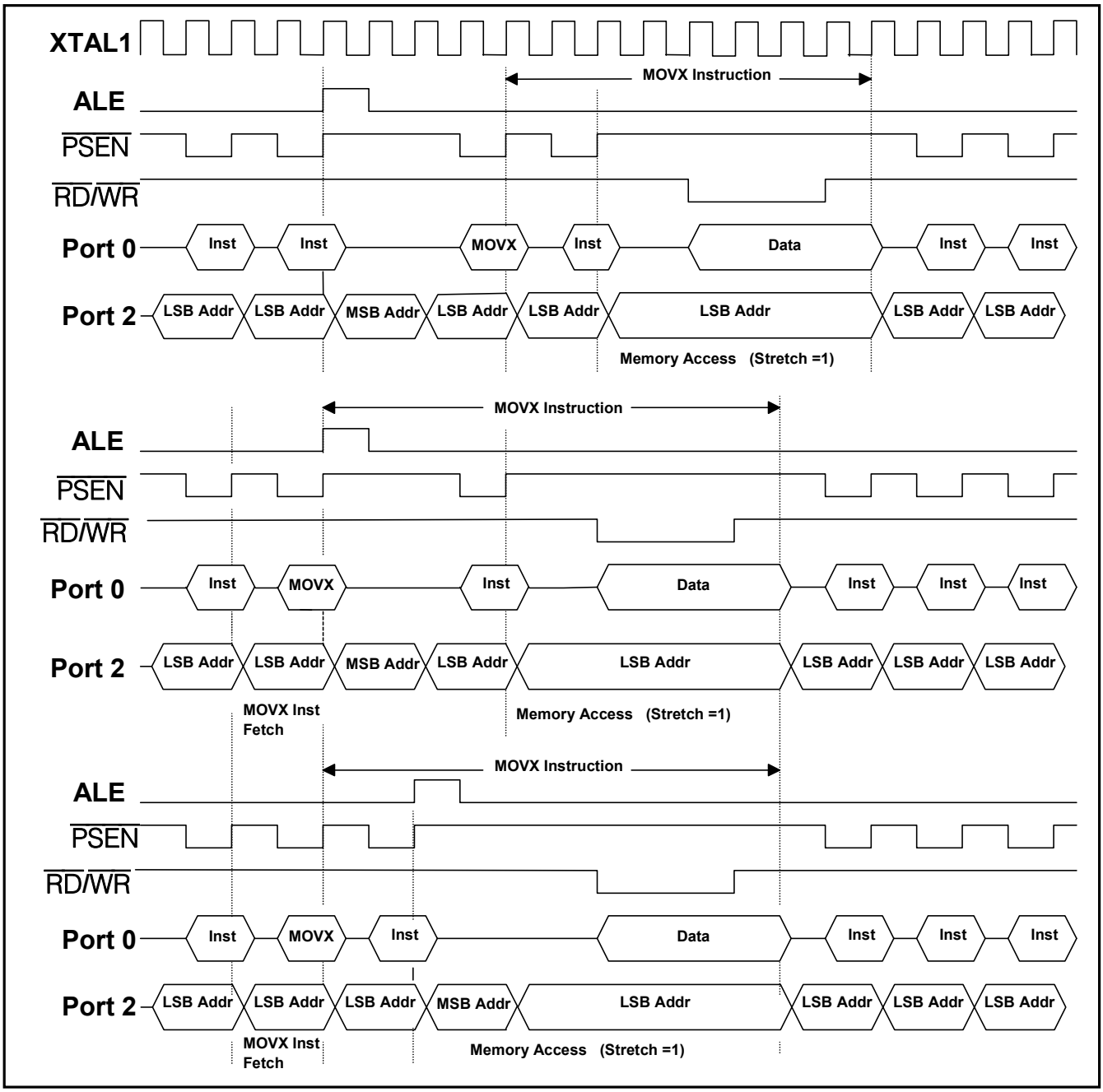
As shown in the previous tables, the stretch feature supports eight stretched external data-memory access options, which can be categorized into three timing groups. When the stretch value is cleared to 000b, there is no stretch on external data memory access, and a MOVX instruction is completed in two basic memory cycles. When the stretch value is set to 1, 2, or 3, the external data memory access is extended by 1, 2, or 3 stretch memory cycles, respectively. Note that the first stretch value does not result in adding four system clocks to the control signals. This is because the first stretch uses one system clock to create additional address setup and data bus float time and one system clock to create additional address and data hold time. When using very slow RAM and peripherals, a larger stretch value (4–7) can be selected. In this stretch category, two stretch cycles are used to create additional setup (the ALE pulse width is also stretched by one stretch cycle for page miss) and one stretch cycle is used to create additional hold time. The following timing diagrams illustrate the external data memory access at divide-by-1 system clock mode (CD1:CD0 = 10b).

Figure 12 illustrates the external data-memory stretch-cycle timing relationship when PAGEE = 1 and PAGES1:PAGES0 = 01. The stretch cycle shown is for a stretch value of 1 and is coincident with a page miss. Note that the first stretch value does not result in adding four system clocks to the $\overline{RD}/\overline{WR}$ control signals. This is because the first stretch uses one system clock to create additional setup and one system clock to create additional hold time.

Figure 13 shows the timing relationship for a slow peripheral interface (stretch value = 4). Note that a page hit data memory cycle is shorter than a page miss data memory cycle. The ALE pulse width is also stretched by a stretch cycle in the case of a page miss.

The stretched data memory bus cycle timing relationship for PAGES = 11 is identical to nonpage mode operation since the basic data memory cycle always contains four system clocks in this page mode operation.

Figure 12. Page Mode 1, External Data Memory Access (PAGES = 01, STRETCH = 1, CD = 10)



Interrupt Priority

There are five levels of interrupt priority: Level 4 to 0. The highest interrupt priority is level 4, which is reserved for the power-fail interrupt. All other interrupts have individual priority bits in the interrupt priority registers to allow each interrupt to be assigned a priority level from 3 to 0. The power-fail interrupt always has the highest priority if it is enabled. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in Table 11.

The processor indicates that an interrupt condition occurred by setting the respective flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Unless marked in Table 11, all these flags must be cleared by software.

Table 11. Interrupt Summary

INTERRUPT	VECTOR	NATURAL ORDER	FLAG	ENABLE	PRIORITY CONTROL
Power Fail	33h	0 (Highest)	PFI (WDCON.4)	EPFI(WDCON.5)	N/A
External Interrupt 0	03h	1	IE0 (TCON.1) (Note 1)	EX0 (IE.0)	LPX0 (IP0.0); MPX0 (IP1.0)
Timer 0 Overflow	0Bh	2	TF0 (TCON.5) (Note 2)	ET0 (IE.1)	LPT0 (IP0.1); MPT0 (IP1.1)
External Interrupt 1	13h	3	IE1 (TCON.3) (Note 1)	EX1 (IE.2)	LPX1 (IP0.2); MPX1 (IP1.2)
Timer 1 Overflow	1Bh	4	TF1 (TCON.7) (Note 2)	ET1 (IE.3)	LPT1 (IP0.3); MPT1 (IP1.3)
Serial Port 0	23h	5	RI_0 (SCON0.0); TI_0 (SCON0.1)	ES0 (IE.4)	LPS0 (IP0.4); MPS0 (IP1.4)
Timer 2 Overflow	2Bh	6	TF2 (T2CON.7); EXF2 (T2CON.6)	ET2 (IE.5)	LPT2 (IP0.5); MPT2 (IP1.5)
Serial Port 1	3Bh	7	RI_1 (SCON1.0); TI_1 (SCON1.1)	ES1 (IE.6)	LPS1 (IP0.6); MPS1 (IP1.6)
External Interrupt 2	43h	8	IE2 (EXIF.4)	EX2 (EIE.0)	LPX2 (EIP0.0); MPX2 (EIP1.0)
External Interrupt 3	4Bh	9	IE3 (EXIF.5)	EX3 (EIE.1)	LPX3 (EIP0.1); MPX3 (EIP1.1)
External Interrupt 4	53h	10	IE4 (EXIF.6)	EX4 (EIE.2)	LPX4 (EIP0.2); MPX4 (EIP1.2)
External Interrupt 5	5Bh	11	IE5 (EXIF.7)	EX5 (EIE.3)	LPX5 (EIP0.3); MPX5 (EIP1.3)
Watchdog	63h	12 (Lowest)	WDIF (WDCON.3)	EWDI (EIE.4)	LPWDI (EIP0.4); MPWDI (EIP1.4)

Note 1: If the interrupt is edge triggered, the flag is cleared automatically by hardware when the service routine is vectored to. If the interrupt is level triggered, the flag follows the state of the pin.
Note 2: The flag is cleared automatically by hardware when the service routine is vectored to.

Watchdog Timer

The watchdog timer functions as the source of both the watchdog interrupt and the watchdog reset. When the clock divider is set to 10b, the interrupt timeout has a default divide ratio of 2^{17} of the crystal oscillator clock, with the watchdog reset set to time out 512 system clock cycles later. This results in a 33MHz crystal oscillator producing an interrupt timeout every 3.9718ms, followed 15.5µs later by a watchdog reset. The watchdog timer is reset to the default divide ratio following any reset. Using the WD0 and WD1 bits in the clock control (CKCON.6 and 7) register, other divide ratios can be selected for longer watchdog interrupt periods. Table 13 summarizes the watchdog bits settings and the timeout values. **Note:** All watchdog timer reset timeouts follow the programmed interrupt timeouts by 512 system clock cycles, which equates to varying numbers of oscillator cycles depending on the clock divide (CD1:0) and crystal multiplier settings.

Table 13. Watchdog Timeout Value (In Number of Oscillator Clocks)

4X/$\overline{2X}$	CD1:0	WATCHDOG INTERRUPT TIMEOUT				WATCHDOG RESET TIMEOUT			
		WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11	WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11
1	00	2^{15}	2^{18}	2^{21}	2^{24}	2^{15} + 128	2^{18} + 128	2^{21} + 128	2^{24} + 128
0	00	2^{16}	2^{19}	2^{22}	2^{25}	2^{16} + 256	2^{19} + 256	2^{22} + 256	2^{25} + 256
x	01	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	10	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	11	2^{27}	2^{30}	2^{33}	2^{36}	2^{27} + 524,288	2^{30} + 524,288	2^{33} + 524,288	2^{36} + 524,288

A watchdog control (WDCON) SFR is used for programming the functions. EWT (WDCON.1) is the enable for the watchdog timer-reset function and RWT (WDCON.0) is the bit used to restart the watchdog timer. Setting the RWT bit restarts the timer for another full interval. If the watchdog timer-reset function is masked by the EWT bit and no resets are issued to the timer through the RWT bit, the watchdog timer generates interrupt timeouts at a rate determined by the programmed divide ratio. WDIF (WDCON.3) is the interrupt flag set at timer termination and WTRF (WDCON.2) is the reset flag set following a watchdog reset timeout. Setting the EWDI bit (EIE.4) enables the watchdog interrupt. The watchdog timer reset and interrupt timeouts are measured by counting system clock cycles.

An independent watchdog timer functions as the crystal startup counter to count 65,536 crystal clock cycles before allowing the crystal oscillator to function as the system clock. This warmup time is verified by the watchdog timer following each power-up as well as each time the crystal is restarted following a stop mode. The watchdog is also used to establish a startup time whenever the CTM in the PMR register is set to enable the crystal multiplier (4X/$\overline{2X}$).

One of the watchdog timer applications is for the watchdog to wake up the system from idle mode. The watchdog interrupt can be programmed to allow a system to wake up periodically to sample the external world.

Internal System Reset

A software reset can be initiated by writing a system reset command to the flash control SFR. The reset state is maintained for approximately 90 external clock cycles. During this time, the RST pin is driven to a logic high. Once the reset is removed, the RST pin is driven low, and operation begins from address 0000h.

REVISION HISTORY

DATE	DESCRIPTION
111003	New product release.
032204	*DC Electrical Characteristics* table: Corrected typo—Under Supply Current for Active and Idle Mode, changed Units from "µA" to "mA." Note 15: Changed number of external clock cyles per system clock and minimum external clock speeds. *Flash Memory Programming Characteristics* table: Removed Note 20 (room temperature only) from the Data Retention parameter.
060204	Changed Write/Erase Endurance parameter from 20,000 cycles to 10,000 cycles. Removed original *Table 5. Parallel Programming Instruction Set*, and replaced it with a paragraph introducing the subject and advising interested parties to contact the factory for more information. Clarified IAP programming sequence.
060805	Added lead-free devices to *Ordering Information* table.
091906	Removed references to DS89C440 and/or added "Contact factory or replace with DS89C430 or DS89C450."
040507	Added clarification to the *Security Features* section and *Table 3* that flash security levels 1, 2, and 3 should not be used when executing external code (page 22); corrected Figure 8 to show PSEN high through the second machine cycle (page 28).