Analog Devices Inc./Maxim Integrated - DS89C440-MNG Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds89c440-mng

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

Note 2: All voltages are referenced to ground.

Note 3: The user should note that this part is tested and guaranteed to operate down to 4.5V (10%) and that V_{RST} (min) is specified below that point. This indicates that there is a range of voltages [(V_{MIN} to V_{RST} (min)] where the processor's operation is not guaranteed, but the reset trip point has not been reached. This should not be an issue in most applications, but should be considered when proper operation must be maintained at all times. For these applications, it may be desirable to use a more accurate external reset.

Note 4: While the specifications for V_{PFW} and V_{RST} overlap, the design of the hardware makes it so this is not possible. Within the ranges given, there is guaranteed separation between these two voltages.

Note 5: Active current is measured with a 33MHz clock source driving XTAL1, V_{CC} = RST = 5.5V. All other pins are disconnected.

Note 6: Idle mode current is measured with a 33MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground. All other pins are disconnected.

Note 7: Stop mode is measured with XTAL and RST grounded, V_{CC} = 5.5V. All other pins are disconnected.

Note 8: RST = 5.5V. This condition mimics the operation of pins in I/O mode.

Note 9: During a 0-to-1 transition, a one shot drives the ports hard for two clock cycles. This measurement reflects a port pin in transition mode.

Note 10: When addressing external memory.

Note 11: Guaranteed by design.

Note 12: Ports 1, 2, and 3 source transition current when pulled down externally. The current reaches its maximum at approximately 2V.

Note 13: RST = 5.5V. Port 0 is floating during reset and when in the logic-high state during I/O mode.

Note 14: This port is a weak address holding latch in bus mode. Peak current occurs near the input transition point of the holding latch at approximately 2V.

AC CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (See Figure 1, Figure 2, and Figure 3.)

PARAMETER	SYMBOL	1-CYCLE PAGE MODE 1		2-CYCLE PAGE MODE 1		4-CYCLE PAGE MODE 1		PAGE MODE 2		NONPAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}		t_{CLCL} - 20		t_{CLCL} - 20		$2t_{CLCL}$ - 20		t_{CLCL} - 20		$2t_{CLCL}$ - 20	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}	0		0		0		0		0		ns
Input Instruction Float After $\overline{PSEN}$	t_{PXIZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
Port 0 Address to Valid Instruction In	t_{AVIV0}								$1.5t_{CLCL}$ - 22		$3t_{CLCL}$ - 22	ns
Port 2 Address to Valid Instruction In	t_{AVIV2}		t_{CLCL} - 20		$1.5t_{CLCL}$ - 20		$2.5t_{CLCL}$ - 20		$3t_{CLCL}$ - 20		$3.5t_{CLCL}$ - 20	ns
$\overline{PSEN}$ Low to Port 0 Address Float	t_{PLAZ}								0		0	ns
$\overline{RD}$ Pulse Width (P3.7) (Note 16)	t_{RLRH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{WR}$ Pulse Width (P3.6) (Note 16)	t_{WLWH}	t_{CLCL} - 5 + t_{STC1}		t_{CLCL} - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}		ns
$\overline{RD}$ (P3.7) Low to Valid Data In (Note 16)	t_{RLDV}		t_{CLCL} - 18 + t_{STC1}		t_{CLCL} - 18 + t_{STC1}		$2t_{CLCL}$ - 18 + t_{STC1}		$2t_{CLCL}$ - 18 + t_{STC1}		$2t_{CLCL}$ - 18 + t_{STC1}	ns
Data Hold After $\overline{RD}$ (P3.7)	t_{RHDX}	0		0		0		0		0		ns
Data Float After $\overline{RD}$ (P3.7)	t_{RHDZ}								t_{CLCL} - 5		t_{CLCL} - 5	ns
MOVX ALE Low to Input Data Valid (Note 16)	t_{LLDV}								$2t_{CLCL}$ - 8 + t_{STC1}		$2t_{CLCL}$ - 5 + t_{STC1}	ns

AC CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (See Figure 1, Figure 2, and Figure 3.)

PARAMETER	SYMBOL	1-CYCLE PAGE MODE 1		2-CYCLE PAGE MODE 1		4-CYCLE PAGE MODE 1		PAGE MODE 2		NONPAGE MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Port 0 Address to Valid Data In (Note 16)	t_{AVDV0}								$3t_{CLCL}$ - 20 + t_{STC1}		$3t_{CLCL}$ - 20 + t_{STC1}	ns
Port 2 Address to Valid Data In (Note 16)	t_{AVDV2}		t_{CLCL} - 20 + t_{STC1}		$1.5t_{CLCL}$ - 20 + t_{STC1}		$3.5t_{CLCL}$ - 20 + t_{STC1}		$3.0t_{CLCL}$ - 20 + t_{STC1}		$3.5t_{CLCL}$ - 20 + t_{STC1}	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{LLRL} (t_{LLWL})	$0.5t_{CLCL}$ - 8 + t_{STC2}	$0.5t_{CLCL}$ + 6 + t_{STC2}	$2t_{CLCL}$ - 8 + t_{STC2}	$2t_{CLCL}$ + 6 + t_{STC2}	$4t_{CLCL}$ - 8 + t_{STC2}	$4t_{CLCL}$ + 6 + t_{STC2}	$0.5t_{CLCL}$ - 8 + t_{STC2}	$0.5t_{CLCL}$ + 4 + t_{STC2}	$0.5t_{CLCL}$ - 8 + t_{STC2}	$0.5t_{CLCL}$ + 5 + t_{STC2}	ns
Port 0 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{AVRL0} (t_{AVWL0})							$1.5t_{CLCL}$ - 5 + t_{STC2}		t_{CLCL} - 5 + t_{STC2}		ns
Port 2 Address Valid to $\overline{RD}$ or $\overline{WR}$ Low (Note 16)	t_{AVRL2} (t_{AVWL2})	0 + t_{STC5} - 5		$0.5t_{CLCL}$ - 5 + t_{STC5}		$1.5t_{CLCL}$ - 5 + t_{STC5}		t_{CLCL} - 5 + t_{STC5}		$1.5t_{CLCL}$ - 5 + t_{STC5}		ns
Data Out Valid to $\overline{WR}$ Transition (Note 15)	t_{QVWX}	-5		-5		-5		-5		-5		ns
Data Hold After $\overline{WR}$ (Note 15)	t_{WHQX}	t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		t_{CLCL} + t_{STC2} - 10		ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High (Note 15)	t_{RHLH} (t_{WHLH})	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	t_{STC2} - 2	t_{STC2} + 4	ns

Note: Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics assume 50% duty cycle for the oscillator and are not 100% tested, but are guaranteed by design.

POWER-CYCLE TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Startup Time (Note 18)	t_{CSU}		8		ms
Power-On Reset Delay (Note 19)	t_{POR}		65,536		t_{CLCL}

Note 18: Startup time for a crystal varies with load capacitance and manufacturer. The time shown is for an 11.0592MHz crystal manufactured by Fox Electronics.

Note 19: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

FLASH MEMORY PROGRAMMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data Retention	t_{DR}	100			years
Write/Erase Endurance	t_{ENDURE}	10,000			cycles
Program/Time	t_{PROG}			40	µs
Erase Time	t_{ERASE}	4			ms

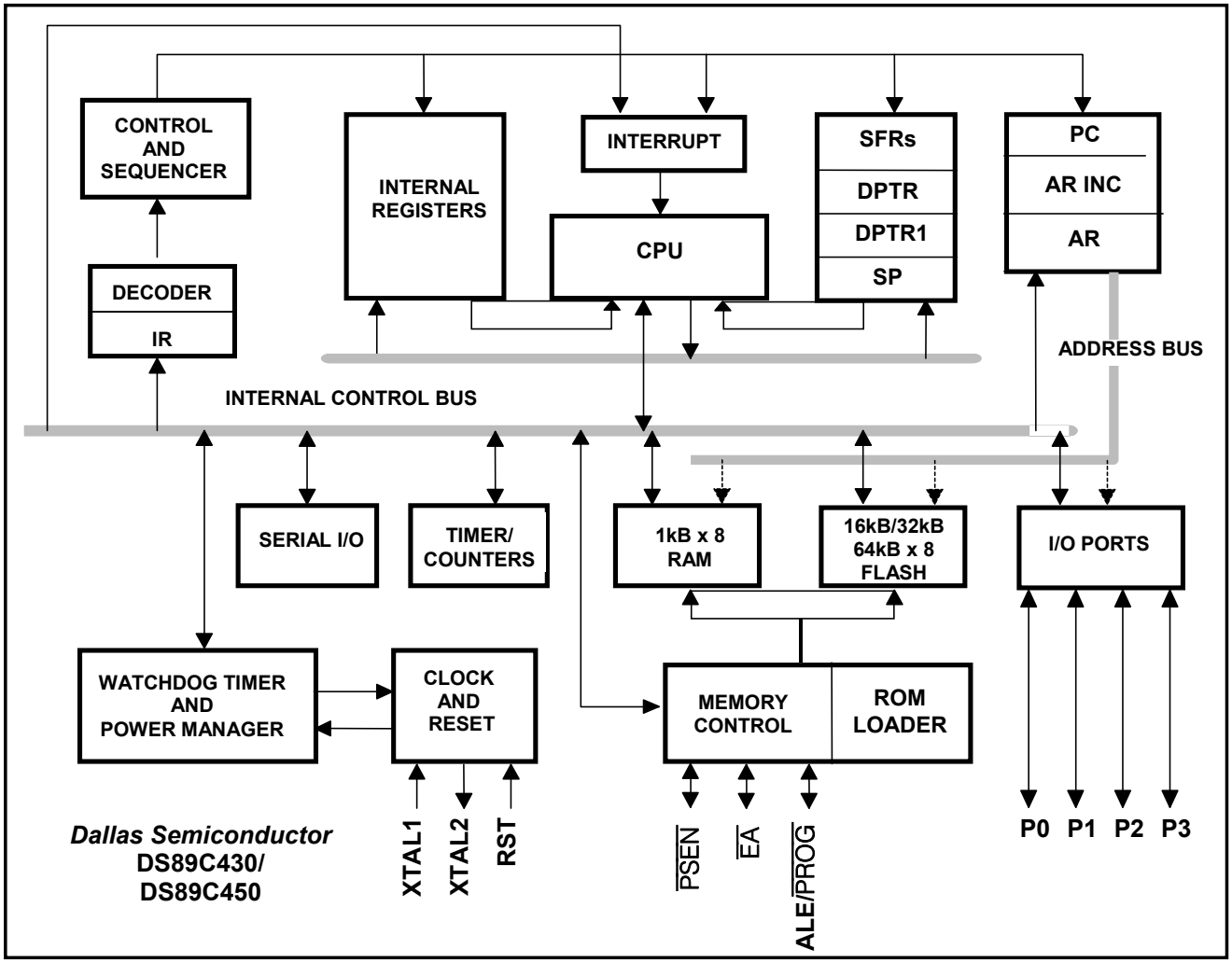
PIN DESCRIPTION

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
40	12, 44	6, 38	V_{CC}	**+5V**
20	1, 22, 23, 34	16, 17, 28, 39	GND	**Logic Ground**
9	10	4	RST	**External Reset.** The RST input pin is bidirectional and contains a Schmitt Trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, as the device provides this function internally.
19	21	15	XTAL1	**Crystal Oscillators.** These pins provide support for fundamental-mode parallel-resonant AT-cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
18	20	14	XTAL2	
29	32	26	$\overline{PSEN}$	**Program Store Enable.** This signal is commonly connected to optional external program memory as a chip enable. $\overline{PSEN}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In one-cycle page mode 1, $\overline{PSEN}$ remains low for consecutive page hits.
30	33	27	ALE/$\overline{PROG}$	**Address Latch Enable.** This signal functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373-family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{PROG}$) is used to execute the parallel program function.
39	43	37	P0.0 (AD0)	**Port 0 (AD0–AD7), I/O.** Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of port 0 is tri-state. Pullup resistors are required only when using port 0 as an I/O port.
38	42	36	P0.1 (AD1)	
37	41	35	P0.2 (AD2)	
36	40	34	P0.3 (AD3)	
35	39	33	P0.4 (AD4)	
34	38	32	P0.5 (AD5)	
33	37	31	P0.6 (AD6)	
32	36	30	P0.7 (AD7)	

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>PDIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>1</td><td>2</td><td>40</td><td>P1.0</td><td rowspan="8">Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for timer 2 I/O, new external interrupts, and new serial port 1. The reset condition of port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate functions of port 1 are as follows:
PORT — ALTERNATE — FUNCTION
P1.0 — T2 — External I/O for Timer/Counter2
P1.1 — T2EX — Timer 2 Capture/Reload Trigger
P1.2 — RXD1 — Serial Port 1 Receive
P1.3 — TXD1 — Serial Port 1 Transmit
P1.4 — INT2 — External Interrupt 2 (Positive Edge Detect)
P1.5 — $\overline{INT3}$ — External Interrupt 3 (Negative Edge Detect)
P1.6 — INT4 — External Interrupt 4 (Positive Edge Detect)
P1.7 — $\overline{INT5}$ — External Interrupt 5 (Negative Edge Detect)</td></tr>
<tr><td>2</td><td>3</td><td>41</td><td>P1.1</td></tr>
<tr><td>3</td><td>4</td><td>42</td><td>P1.2</td></tr>
<tr><td>4</td><td>5</td><td>43</td><td>P1.3</td></tr>
<tr><td>5</td><td>6</td><td>44</td><td>P1.4</td></tr>
<tr><td>6</td><td>7</td><td>1</td><td>P1.5</td></tr>
<tr><td>7</td><td>8</td><td>2</td><td>P1.6</td></tr>
<tr><td>8</td><td>9</td><td>3</td><td>P1.7</td></tr>
<tr><td>21</td><td>24</td><td>18</td><td>P2.0 (A8)</td><td rowspan="8">Port 2 (A8–A15), I/O. Port 2 is an 8-bit, bidirectional I/O port. The reset condition of port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function, port 2 can function as the MSB of the external address bus when reading external program memory and read/write external RAM or peripherals. In page mode 1, port 2 provides both the MSB and LSB of the external address bus. In page mode 2, it provides the MSB and data.</td></tr>
<tr><td>22</td><td>25</td><td>19</td><td>P2.1 (A9)</td></tr>
<tr><td>23</td><td>26</td><td>20</td><td>P2.2 (A10)</td></tr>
<tr><td>24</td><td>27</td><td>21</td><td>P2.3 (A11)</td></tr>
<tr><td>25</td><td>28</td><td>22</td><td>P2.4 (A12)</td></tr>
<tr><td>26</td><td>29</td><td>23</td><td>P2.5 (A13)</td></tr>
<tr><td>27</td><td>30</td><td>24</td><td>P2.6 (A14)</td></tr>
<tr><td>28</td><td>31</td><td>25</td><td>P2.7 (A15)</td></tr>
<tr><td>10</td><td>11</td><td>5</td><td>P3.0</td><td rowspan="8">Port 3, I/O. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for external interrupts, serial port 0, timer 0 and 1 inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of port 3 are as follows:
PORT — ALTERNATE — FUNCTION
P3.0 — RXD0 — Serial Port 0 Receive
P3.1 — TXD0 — Serial Port 0 Transmit
P3.2 — $\overline{INT0}$ — External Interrupt 0
P3.3 — $\overline{INT1}$ — External Interrupt 1
P3.4 — T0 — Timer 0 External Input
P3.5 — T1 — Timer 1 External Input
P3.6 — $\overline{WR}$ — External Data Memory Write Strobe
P3.7 — $\overline{RD}$ — External Data Memory Read Strobe</td></tr>
<tr><td>11</td><td>13</td><td>7</td><td>P3.1</td></tr>
<tr><td>12</td><td>14</td><td>8</td><td>P3.2</td></tr>
<tr><td>13</td><td>15</td><td>9</td><td>P3.3</td></tr>
<tr><td>14</td><td>16</td><td>10</td><td>P3.4</td></tr>
<tr><td>15</td><td>17</td><td>11</td><td>P3.5</td></tr>
<tr><td>16</td><td>18</td><td>12</td><td>P3.6</td></tr>
<tr><td>17</td><td>19</td><td>13</td><td>P3.7</td></tr>
<tr><td>31</td><td>35</td><td>29</td><td>$\overline{EA}$</td><td>External Access. Allows selection of internal or external program memory. Connect to ground to force the DS89C430/DS89C450 to use an external memory program memory. The internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal flash memory.</td></tr>
</table>

Figure 5. Functional Diagram



DETAILED DESCRIPTION

The DS89C430 and DS89C450 are pin compatible with all three packages of the standard 8051 and include standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. The three part numbers vary only by the amount of internal flash memory (DS89C430 = 16kB, DS89C450 = 64kB), which can be in-system/in-application programmed from a serial port using ROM-resident or user-defined loader software. For volume deployments, the flash can also be loaded externally using standard commercially available parallel programmers.

Besides greater speed, the DS89C430/DS89C450 include 1kB of data RAM, a second full hardware serial port, seven additional interrupts, two extra levels of interrupt priority, programmable watchdog timer, brownout monitor, and power-fail reset. Dual data pointers (DPTRs) are included to speed up block data-memory moves with further enhancements coming from selectable automatic increment/decrement and toggle select operation. The speed of MOVX data memory access can be adjusted by adding stretch values up to 10 machine cycles for flexibility in selecting external memory and peripherals.

A power management mode consumes significantly lower power by slowing the CPU execution rate from one clock period per cycle to 1024 clock periods per cycle. A selectable switchback feature can automatically cancel this mode to enable normal speed responses to interrupts.

For EMI-sensitive applications, the microcontroller can disable the ALE signal when the processor is not accessing external memory.

Terminology

The term *DS89C430* is used in the remainder of the document to refer to the DS89C430 and DS89C450, unless otherwise specified.

Compatibility

The DS89C430 is a fully static CMOS 8051-compatible microcontroller similar in functional features to the DS87C520, but it offers much higher performance. In most cases, the DS89C430 can drop into an existing socket for the 8xC51 family, immediately improving the operation. While remaining familiar to 8051 family users, the DS89C430 has many new features. In general, software written for existing 8051-based systems works without modification on the DS89C430, with the exception of critical timing routines, as the DS89C430 performs its instructions much faster for any given crystal selection.

The DS89C430 provides three 16-bit timer/counters, two full-duplex serial ports, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports can operate as in standard 8051 products. Timers default to 12 clocks-per-cycle operation to keep their timing compatible with a legacy 8051 family systems. However, timers are individually programmable to run at the new one clock per cycle if desired. The DS89C430 provides several new hardware features, described in subsequent sections, implemented by new special-function registers (SFRs).

Performance Overview

Featuring a completely redesigned high-speed 8051-compatible core, the DS89C430 allows operation at a higher clock frequency. This updated core does not have the wasted memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. The same machine cycle takes one clock in the DS89C430. Thus, the fastest instructions execute 12 times faster for the same crystal frequency (and actually 24 times faster for the INC data pointer instruction). It should be noted that this speed improvement is reduced when using external memory access modes that require more than one clock per cycle.

Individual program improvement depends on the instructions used. Speed-sensitive applications would make the most use of instructions that are 12 times faster. However, the sheer number of 12-to-1 improved op codes makes dramatic speed improvements likely for any code. These architectural improvements produce instruction cycle times as low as 30ns. The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory. The new page modes allow for increased efficiency in external memory accesses.

Instruction Set Summary

All instructions have the same functionality as their 8051 counterparts, including their affect on bits, flags, and other status functions. However, the timing of each instruction is different, in both absolute and relative number of clocks.

For absolute timing of real-time events, the duration of software loops can be calculated using information given in the *Instruction Set* table in the *Ultra-High-Speed Flash Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at a reduced number of clocks per increment to take advantage of faster processor operation.

The relative time of some instructions may be different in the new architecture. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS89C430, the MOVX instruction takes as little as two machine cycles or two oscillator cycles, but the "MOV direct, direct" uses three machine cycles or three oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS89C430 usually uses one machine cycle for each instruction byte and requires one cycle for execution. *The user concerned with precise program timing should examine the timing of each instruction to become familiar with the changes*.

Special-Function Registers (SFRs)

All peripherals and operations that are not explicit instructions in the DS89C430 are controlled through SFRs. The most common features basic to the architecture are mapped to the SFRs. These include the CPU registers (ACC, B, and PSW), data pointers, stack pointer, I/O ports, timer/counters, and serial ports. In many cases, an SFR controls an individual function or reports the function's status. The SFRs reside in register locations 80h–FFh and are only accessible by direct addressing. SFRs with addresses ending in 0h or 8h are bit addressable.

Table 1. SFR Register Map (continued)

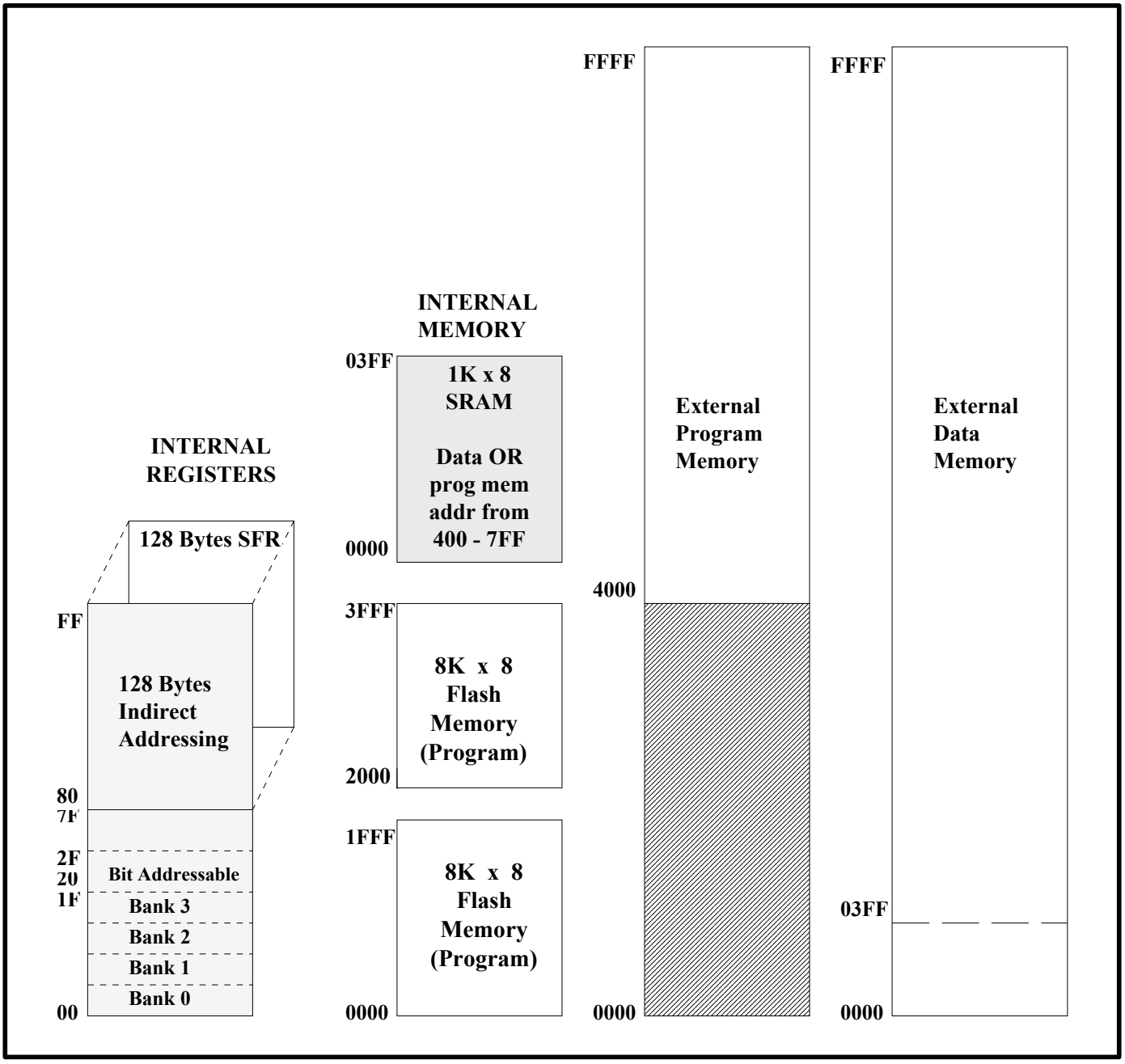
REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TH1	8Dh								
CKCON	8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
P1	90h	P1.7/$\overline{INT5}$	P1.6/INT4	P1.5/$\overline{INT3}$	P1.4/INT2	P1.3/TXD1	P1.2/RXD1	P1.1/T2EX	P1.0/T2
EXIF	91h	IE5	IE4	IE3	IE2	CKRY	RGMD	RGSL	BGS
CKMOD	96h			T2MH	T1MH	T0MH	—	—	—
SCON0	98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
SBUF0	99h								
ACON	9Dh	PAGEE	PAGES1	PAGES0	—	—	—	—	—
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
SADDR0	A9h								
SADDR1	AAh								
P3	B0h	P3.7/$\overline{RD}$	P3.6/$\overline{WR}$	P3.5/T1	P3.4/T0	P3.3/$\overline{INT1}$	P3.2/$\overline{INT0}$	P3.1/TXD0	P3.0/RXD0
IP1	B1h	—	MPS1	MPT2	MPS0	MPT1	MPX1	MPT0	MPX0
IP0	B8h	—	LPS1	LPT2	LPS0	LPT1	LPX1	LPT0	LPX0
SADEN0	B9h								
SADEN1	BAh								
SCON1	C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
SBUF1	C1h								
ROMSIZE	C2h					PRAME	RMS2	RMS1	RMS0
PMR	C4h	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEON	DME1	DME0
STATUS	C5h	PIS2	PIS1	PIS0	—	SPTA1	SPRA1	SPTA0	SPRA0
TA	C7h								
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9h							T2OE	DCEN
RCAP2L	CAh								
RCAP2H	CBh								
TL2	CCh								
TH2	CDh								
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P
FCNTL	D5h	$\overline{FBUSY}$	FERR			FC3	FC2	FC1	FC0
FDATA	D6h								
WDCON	D8h	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
ACC	E0h								
EIE	E8h	—	—	—	EWDI	EX5	EX4	EX3	EX2
B	F0h								
EIP1	F1h	—	—	—	MPWDI	MPX5	MPX4	MPX3	MPX2
EIP0	F8h	—	—	—	LPWDI	LPX5	LPX4	LPX3	LPX2

Note: Shaded bits are timed-access protected.

Table 2. SFR Reset Value

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	1	1	1	1	1	1	1	1
SP	81h	0	0	0	0	0	1	1	1
DPL	82h	0	0	0	0	0	0	0	0
DPH	83h	0	0	0	0	0	0	0	0
DPL1	84h	0	0	0	0	0	0	0	0
DPH1	85h	0	0	0	0	0	0	0	0
DPS	86h	0	0	0	0	0	1	0	0
PCON	87h	0	0	Special	Special	0	0	0	0
TCON	88h	0	0	0	0	0	0	0	0
TMOD	89h	0	0	0	0	0	0	0	0
TL0	8Ah	0	0	0	0	0	0	0	0
TL1	8Bh	0	0	0	0	0	0	0	0
TH0	8Ch	0	0	0	0	0	0	0	0
TH1	8Dh	0	0	0	0	0	0	0	0
CKCON	8Eh	0	0	0	0	0	0	0	1
P1	90h	1	1	1	1	1	1	1	1
EXIF	91h	0	0	0	0	Special	Special	Special	0
CKMOD	96h	1	1	0	0	0	1	1	1
SCON0	98h	0	0	0	0	0	0	0	0
SBUF0	99h	0	0	0	0	0	0	0	0
ACON	9Dh	0	0	0	1	1	1	1	1
P2	A0h	1	1	1	1	1	1	1	1
IE	A8h	0	0	0	0	0	0	0	0
SADDR0	A9h	0	0	0	0	0	0	0	0
SADDR1	AAh	0	0	0	0	0	0	0	0
P3	B0h	1	1	1	1	1	1	1	1
IP1	B1h	1	0	0	0	0	0	0	0
IP0	B8h	1	0	0	0	0	0	0	0
SADEN0	B9h	0	0	0	0	0	0	0	0
SADEN1	BAh	0	0	0	0	0	0	0	0
SCON1	C0h	0	0	0	0	0	0	0	0
SBUF1	C1h	0	0	0	0	0	0	0	0
ROMSIZE	C2h	1	1	1	1	0	1	0	1
PMR	C4h	1	0	0	0	0	0	0	0
STATUS	C5h	0	0	0	1	0	0	0	0
TA	C7h	1	1	1	1	1	1	1	1
T2CON	C8h	0	0	0	0	0	0	0	0
T2MOD	C9h	1	1	1	1	1	1	0	0
RCAP2L	CAh	0	0	0	0	0	0	0	0
RCAP2H	CBh	0	0	0	0	0	0	0	0

Figure 6. Memory Map (as shown for the DS89C430)



Memory Configuration

As illustrated in Figure 6, the DS89C430 incorporates two 8kB flash areas for on-chip program memory and 1kB of SRAM for on-chip data memory or a particular range (400–7FF) of “alternate” program memory space. The DS89C450 incorporates two 32kB flash memories. The DS89C430 uses an address scheme that separates program memory from data memory such that the 16-bit address bus can address each memory area up to maximum of 64kB.

The signature bytes can be read in ROM loader mode or in parallel programming mode. Reading data from addresses 30h, 31h, and 60h provides signature information on manufacturer, part, and extension as follows:

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer ID
31h	43h	DS89C430 Device ID
31h	44h	DS89C440 Device ID (Contact factory or replace with DS89C430 or DS89C450.)
31h	45h	DS89C450 Device ID
60h	01h	Device Extension

Note: *The read/write accessibility of the flash memory during in-application programming is not affected by the state of the lock bits. However, the lock bits do affect the read/write accessibility in ROM loader and parallel programming modes.*

In-Application Programming by User Software

The DS89C430 supports in-application programming of on-chip flash memory by user software. In-application programming is initiated by writing a flash command into the flash control (FCNTL:D5h) register to enable the flash memory for erase/program/verify operations. Address and data are input into the MMU through the flash data (FDATA:D6h) register. The flash command also enables read/write accesses to the FDATA. The MMU's sequencer provides the operation sequences and control functions to the flash memory. The MMU is designed to operate independently from the processor, except for read/write access to the SFRs.

Only the upper bank of the on-chip program memory can be in-application programmed by the user software. The lower bank of the on-chip program memory contains system hardware-dependent codes that are crucial to system operation and should not be altered during in-application programming.

All flash operations are self-timed. The user software can monitor the progress of an erase or programming operation through the flash busy (FBUSY;FCNTL.7) bit with a reset value at logic 1. A selected operation automatically starts when required data is written to the FDATA SFR. The MMU clears the FBUSY bit to indicate the start of a write/erase operation. The FBUSY bit may not change state for up to 1μs after the operation is requested. During this time, the application should poll the status of the FBUSY bit waiting for it to change state. This bit is held low until either the end of the operation or until an error indicator is returned. A flash operating failure terminates the current operation and sets the flash error flag (FERR;FCNTL.6) to logic 1. Both the busy and error flags are read-only bits.

Read/write access during in-application programming is not affected by the state of the lock bits.

A sample programming sequence for a "write upper program memory bank" is shown below. The command must be reentered each time an operation is requested, i.e., it is not permissible to issue the "write upper program memory bank" command once and then repeatedly load address and data values to program a block of memory.

1. Make sure the $\overline{\text{FBUSY}}$ bit is 1 to indicate flash MMU is idle.
2. Write 0Bh to the FCNTL register using the timed access sequence.
3. Write address_MSB to the FDATA register.
4. Write address_LSB to the FDATA register.
5. Write data_value to the FDATA register.
6. Make sure the $\overline{\text{FBUSY}}$ bit is 0 to indicate programming has started.
7. Wait for $\overline{\text{FBUSY}}$ bit to return to 1 to indicate end of programming operation.
8. Make sure FERR is 0 to indicate no programming error.

The flash command (FC3–FC0;FCNTL.3:0) bits provide flash commands as listed in Table 4.

Page Mode, External Memory Cycle

Page mode retains the basic circuitry requirement for an original 8051 external memory interface, but alters the configuration of P0 and P2 for the purposes of address output and data I/O during external memory cycles. Additionally, the functions of ALE and $\overline{PSEN}$ are altered to support this mode of operation.

Setting the PAGEE (ACON.7) bit to logic 1 enables page mode. Clearing the PAGEE bit to logic 0 disables the page mode and the external bus structure defaults to the original 8051 expanded bus configuration (nonpage mode). The DS89C430 supports page mode in two external bus structures. The logic value of the page-mode-select bits in the ACON register determines the external bus structure and the basic memory cycle in number of system clocks. Table 6 summarizes this option. The first three selections use the same bus structure but with different memory cycle time. Setting the select bits to 11b selects another bus structure. Write access to the ACON register requires a timed access.

Table 6. Page Mode Select

PAGES1:PAGES0	CLOCKS PER MEMORY CYCLE		EXTERNAL BUS STRUCTURE
	PAGE-HIT	PAGE-MISS	
00	1	2	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of address.
01	2	4	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of address.
10	4	8	P0: Primary data bus. P2: Primary address bus, multiplexing both the upper byte and lower byte of address.
11	2	4	P0: Lower address byte. P2: The upper address byte is multiplexed with the data byte. Note: This setting affects external code fetches only; accessing the external data memory requires four clock cycles, regardless of page hit or miss.

The first page mode's (page mode 1) external bus structure uses P2 as the primary address bus, (multiplexing both the most significant byte and least significant byte of the address for each external memory cycle) and P0 is used as the primary data bus. During external code fetches, P0 is held in a high-impedance state by the processor. Op codes are driven by the external memory onto P0 and latched at the end of the external fetch cycle at the rising edge of $\overline{PSEN}$. During external data read/write operations, P0 functions as the data I/O bus. It is held in a high-impedance state for external reads from data memory and driven with data during external writes to data memory.

- A page miss occurs when the most significant byte of the subsequent address is different from the last address. The external memory machine cycle can be 2, 4, or 8 system clocks in length for a page miss.

- A page hit occurs when the most significant byte of the subsequent address does not change from the last address. The external memory machine cycle can be 1, 2, or 4 system clocks in length for a page hit.

During a page hit, P2 drives Addr [0–7] of the 16-bit address, while the most significant address byte is held in the external address latches. $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ strobes accordingly for the appropriate operation on the P0 data bus. There is no ALE assertion for page hits.

Table 7. Page Mode 1, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 00)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.25	0.5	1	1024
001	1	0.75	1.5	3	3072
010	2	1.75	3.5	7	7168
011	3	2.75	5.5	11	11,264
100	7	3.75	7.5	15	15,360
101	8	4.75	9.5	19	19,456
110	9	5.75	11.5	23	23,552
111	10	6.75	13.5	27	27,648

Table 8. Page Mode 1, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 01)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.25	0.5	1	1024
001	1	0.75	1.5	3	3072
010	2	1.75	3.5	7	7168
011	3	2.75	5.5	11	11,264
100	7	3.75	7.5	15	15,360
101	8	4.75	9.5	19	19,456
110	9	5.75	11.5	23	23,552
111	10	6.75	13.5	27	27,648

Table 9. Page Mode 1, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 10)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

Table 10. Page Mode 2, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 11)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

As shown in the previous tables, the stretch feature supports eight stretched external data-memory access options, which can be categorized into three timing groups. When the stretch value is cleared to 000b, there is no stretch on external data memory access, and a MOVX instruction is completed in two basic memory cycles. When the stretch value is set to 1, 2, or 3, the external data memory access is extended by 1, 2, or 3 stretch memory cycles, respectively. Note that the first stretch value does not result in adding four system clocks to the control signals. This is because the first stretch uses one system clock to create additional address setup and data bus float time and one system clock to create additional address and data hold time. When using very slow RAM and peripherals, a larger stretch value (4–7) can be selected. In this stretch category, two stretch cycles are used to create additional setup (the ALE pulse width is also stretched by one stretch cycle for page miss) and one stretch cycle is used to create additional hold time. The following timing diagrams illustrate the external data memory access at divide-by-1 system clock mode (CD1:CD0 = 10b).

Figure 12 illustrates the external data-memory stretch-cycle timing relationship when PAGEE = 1 and PAGES1:PAGES0 = 01. The stretch cycle shown is for a stretch value of 1 and is coincident with a page miss. Note that the first stretch value does not result in adding four system clocks to the $\overline{RD}/\overline{WR}$ control signals. This is because the first stretch uses one system clock to create additional setup and one system clock to create additional hold time.

Figure 13 shows the timing relationship for a slow peripheral interface (stretch value = 4). Note that a page hit data memory cycle is shorter than a page miss data memory cycle. The ALE pulse width is also stretched by a stretch cycle in the case of a page miss.

The stretched data memory bus cycle timing relationship for PAGES = 11 is identical to nonpage mode operation since the basic data memory cycle always contains four system clocks in this page mode operation.

Interrupt Priority

There are five levels of interrupt priority: Level 4 to 0. The highest interrupt priority is level 4, which is reserved for the power-fail interrupt. All other interrupts have individual priority bits in the interrupt priority registers to allow each interrupt to be assigned a priority level from 3 to 0. The power-fail interrupt always has the highest priority if it is enabled. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in Table 11.

The processor indicates that an interrupt condition occurred by setting the respective flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Unless marked in Table 11, all these flags must be cleared by software.

Table 11. Interrupt Summary

INTERRUPT	VECTOR	NATURAL ORDER	FLAG	ENABLE	PRIORITY CONTROL
Power Fail	33h	0 (Highest)	PFI (WDCON.4)	EPFI(WDCON.5)	N/A
External Interrupt 0	03h	1	IE0 (TCON.1) (Note 1)	EX0 (IE.0)	LPX0 (IP0.0); MPX0 (IP1.0)
Timer 0 Overflow	0Bh	2	TF0 (TCON.5) (Note 2)	ET0 (IE.1)	LPT0 (IP0.1); MPT0 (IP1.1)
External Interrupt 1	13h	3	IE1 (TCON.3) (Note 1)	EX1 (IE.2)	LPX1 (IP0.2); MPX1 (IP1.2)
Timer 1 Overflow	1Bh	4	TF1 (TCON.7) (Note 2)	ET1 (IE.3)	LPT1 (IP0.3); MPT1 (IP1.3)
Serial Port 0	23h	5	RI_0 (SCON0.0); TI_0 (SCON0.1)	ES0 (IE.4)	LPS0 (IP0.4); MPS0 (IP1.4)
Timer 2 Overflow	2Bh	6	TF2 (T2CON.7); EXF2 (T2CON.6)	ET2 (IE.5)	LPT2 (IP0.5); MPT2 (IP1.5)
Serial Port 1	3Bh	7	RI_1 (SCON1.0); TI_1 (SCON1.1)	ES1 (IE.6)	LPS1 (IP0.6); MPS1 (IP1.6)
External Interrupt 2	43h	8	IE2 (EXIF.4)	EX2 (EIE.0)	LPX2 (EIP0.0); MPX2 (EIP1.0)
External Interrupt 3	4Bh	9	IE3 (EXIF.5)	EX3 (EIE.1)	LPX3 (EIP0.1); MPX3 (EIP1.1)
External Interrupt 4	53h	10	IE4 (EXIF.6)	EX4 (EIE.2)	LPX4 (EIP0.2); MPX4 (EIP1.2)
External Interrupt 5	5Bh	11	IE5 (EXIF.7)	EX5 (EIE.3)	LPX5 (EIP0.3); MPX5 (EIP1.3)
Watchdog	63h	12 (Lowest)	WDIF (WDCON.3)	EWDI (EIE.4)	LPWDI (EIP0.4); MPWDI (EIP1.4)

Note 1: If the interrupt is edge triggered, the flag is cleared automatically by hardware when the service routine is vectored to. If the interrupt is level triggered, the flag follows the state of the pin.
Note 2: The flag is cleared automatically by hardware when the service routine is vectored to.

during the three machine cycles following the writing of the 55h. Writing to a timed-access-protected bit outside of these three machine cycles has no effect on the bit.

The timed-access process is address, data, and time dependent. A processor running out of control and not executing system software statistically is not able to perform this timed sequence of steps, and as such, does not accidentally alter the protected bits. It should be noted that this method should be used in the main body of the system software and *never* used in an interrupt routine in conjunction with the watchdog reset. Interrupt routines using the timed-access watchdog-reset bit (RWT) can recover a lost system and allow the resetting of the watchdog, but the system returns to a lost condition once the RETI is executed, unless the stack is modified. Also, it is advisable that interrupts be disabled (EA = 0) when executing the timed-access sequence, since an interrupt during the sequence adds time, making the timed-access attempt fail.

Power Management and Clock-Divide Control

Power-management features are available that monitor the power-supply voltage levels and support low-power operation with three power-saving modes. Such features include a bandgap voltage monitor, watchdog timer, selectable internal ring oscillator, and programmable system clock speed. The SFRs that provide control and application software access are the watchdog control (WDCON, D8h), extended interrupt enable (EIE, E8h), extended interrupt flag (EXIF, 91h) and power control (PCON, 87h) registers.

System Clock-Divide Control

The programmable clock-divide control bits (CD1 and CD0) provide the processor with the ability to adapt to different crystals and to slow the system clocks, providing lower power operation when required. An on-chip crystal multiplier allows the DS89C430 to operate at two or four times the crystal frequency by setting the 4X/$\overline{2X}$ bit, and is enabled by setting the CTM bit to a logic 1. An additional circuit provides a clock source at divide by 1024. When used with a 7.372MHz crystal, for example, the processor executes the machine cycle in times ranging from 33.9ns (mulitply-by-4 mode) to 138.9µs (divide-by-1024 mode) and maintains a highly accurate serial port baud rate, while allowing the use of more cost-effective lower frequency crystals. Although the clock-divide control bits can be written at any time, certain hardware features enhance the use of these clock controls to guarantee proper serial port operation and to allow for a high-speed response to an external interrupt. The 01b setting of CD1 and CD0 is reserved. It has the same effect as the setting of 10b, which forces the system clock into a divide-by-1 mode. The DS89C430 defaults to divide-by-1 clock mode on all forms of reset.

When in divide-by-1024 mode, in order to allow a quick response to incoming data on a serial port, the system uses the switchback mode to automatically revert to divide-by-1 mode whenever a start bit is detected. This automatic switchback is only enabled in divide-by-1024 mode when the switchback bit (PMR.5:SWB) is set. All other clock modes are unaffected by interrupts and serial port activity.

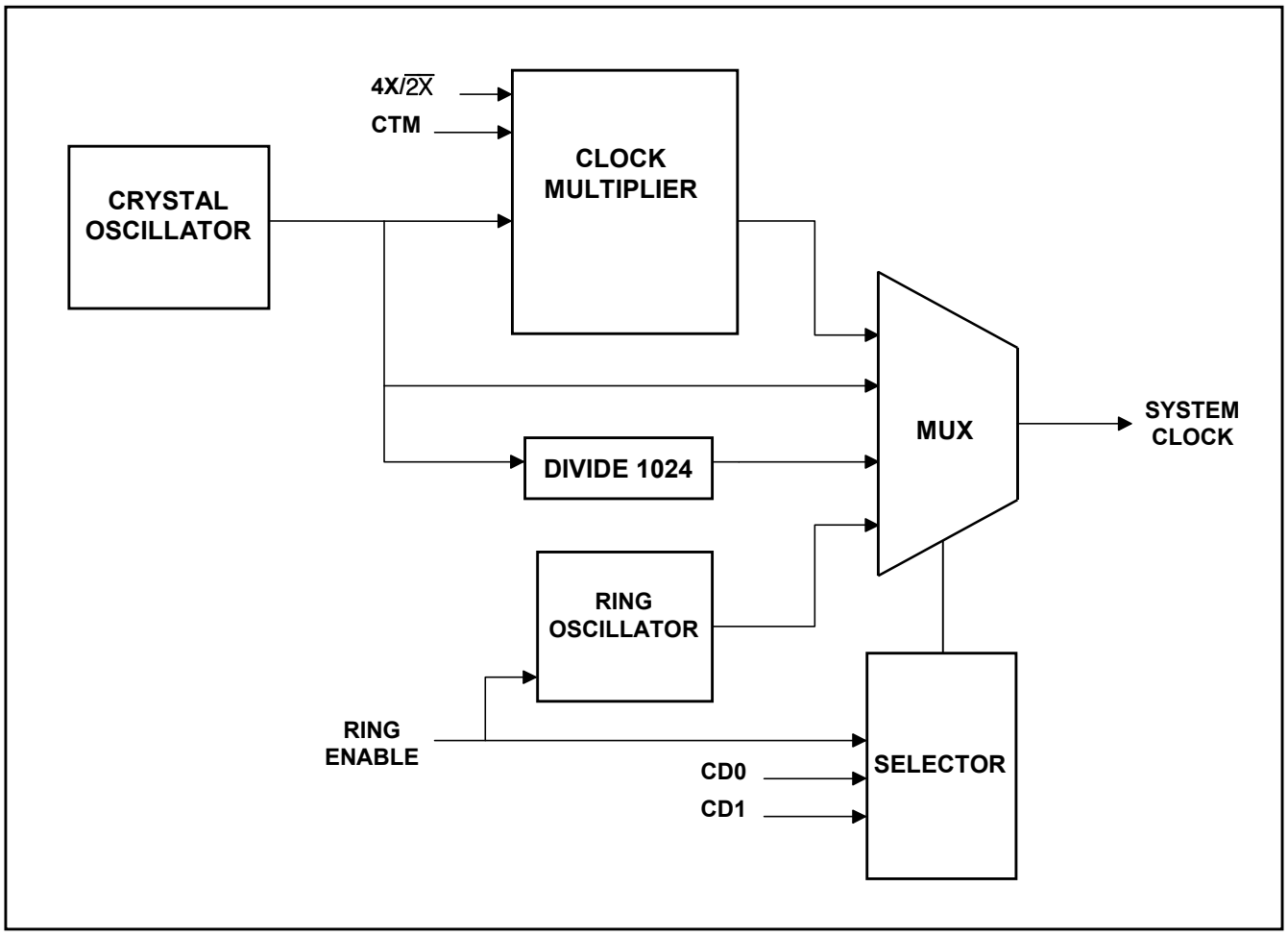
The oscillator multiply ratios of 4, 2, and 1 are also used to provide standard baud-rate generation for the serial ports through a forced divide-by-12 input clock (TxMH,TxM = 00b, x = 1, 2, or 3) to the timers.

Use of the multiply-by-4 or multiply-by-2 options through the clock-divide control bits requires that the crystal multiplier be enabled and the specific system-clock-multiply value be established by the 4X/$\overline{2X}$ bit in the PMR register. The multiplier is enabled through the CTM (PMR.4) bit but cannot be automatically selected until a startup delay has been established through the CKRY bit in the status register. The 4X/$\overline{2X}$ bit can only be altered when the CTM bit is cleared to a logic 0. This prevents the system from changing the multiplier until the system has moved back to the divide-by-1 mode and the multiplier has been disabled by the CTM bit. The CTM bit can only be altered when the CD1 and CD0 bits are set to divide-by-1 mode and the RGMD bit is cleared to 0. Setting the CTM to a logic 1 from a previous logic 0 automatically clears the CKRY bit in the status register and starts the multiplier startup timeout in the multiplier startup counter. During the multiplier startup period, the CKRY bit remains cleared and the CD1 and CD0 clock controls cannot be set to 00b. The CTM bit is cleared to a logic 0 on all resets.

Note that the rated maximum speed of operation applies to the speed of the microcontroller core, not the external clock source. When using the clock multiplier feature, the external clock source frequency, multiplied by the clock multiplier (2X or 4X) can never be faster than the maximum rated speed of the device. Thus, if a designer wished to use the 4X clock multiplier on a device rated at 33MHz, the maximum external clock speed would be 8.25MHz.

Figure 14 gives a simplified description of the generation of the system clocks. Specifics of hardware restrictions associated with the use of the 4X/$\overline{2X}$ CTM, CKRY, CD1, and CD0 bits are outlined in the *SFR* section.

Figure 14. System Clock Sources



Bandgap-Monitored Interrupt and Reset Generation

The power monitor in the DS89C430 monitors the V_{CC} pin in relation to the on-chip bandgap voltage reference. Whenever V_{CC} falls below V_{PFW}, an interrupt is generated if the corresponding power-fail interrupt-enable bit EPFI (WDCON.5) is set, causing the device to vector to address 33h. The power-fail interrupt status bit PFI (WDCON.4) is set any time V_{CC} transitions below V_{PFW}, and can only be cleared by software once set. Similarly, as V_{CC} falls below V_{RST}, a reset is issued internally to halt program execution. Following power-up, a power-on reset initiates a power-on reset timeout before starting program execution. When V_{CC} is first applied to the DS89C430, the processor is held in reset until $V_{CC} > V_{RST}$ and a delay of 65,536 oscillator cycles has elapsed, to ensure that power is within tolerance and the clock source has had time to stabilize. Once the reset timeout period has elapsed, the reset condition is removed automatically and software execution begins at the reset vector location of 0000h. The power-on reset flag POR (WDCON.6) is set to logic 1 to indicate a power-on reset has occurred, and can only be cleared by software.

When the DS89C430 enters stop mode, the bandgap, reset comparator, and power-fail interrupt comparator are automatically disabled to conserve power if the BGS (EXIF.0) bit is set to logic 0. This is the lowest power mode. If BGS is set to logic 1, the bandgap reference, reset comparator, and the power-fail comparator are powered up, although in a mode that reduces their power consumption.

Serial ports and timers track the oscillator cycles per machine cycle when the higher divide ratio of 1024 is selected, and require the switchback function to automatically return to the divide-by-1 mode for proper operation when a qualified event occurs. Table 14 summarizes the effect of clock mode on timer operation.

It is possible to enable a receive function on a serial port when incoming data is not present and then change to the higher divide ratio. An inactive serial port receive/transmission mode requires the receive input pin to remain high and all outgoing transmissions to be completed. During this inactive receive mode it is possible to change the clock-divide control bits from a divide by 1 to a 1024 divide ratio. In the case when the serial port is being used to receive or transmit data, it is very important to validate an attempted change in the clock-divide control bits (read CD1 and CD0 to verify write was allowed) before proceeding with low-power program functions.

Table 14. Effect of Clock Mode on Timer Operation (In Number of Oscillator Clocks)

4X/$\overline{2X}$, CD1, CD0	OSC CYCLES PER MACHINE CYCLE	OSC CYCLES PER TIMERS 0, 1, 2 CLOCK TxMH,TxM =			OSC CYCLES PER TIMER 2 CLOCK BAUD RATE GENERATION	OSC CYCLES PER SERIAL PORT CLOCK MODE 0		OSC CYCLES PER SERIAL PORT CLOCK MODE 2	
		00	01	1x	T2MH,T2M = xx	SM2 = 0	SM2 = 1	SMOD = 0	SMOD = 1
100	0.25	12	1	0.25	2	3	1	64	32
000	0.5	12	2	0.5	2	6	2	64	32
x01	1 (reserved)								
x10	1 (default)	12	4	1	2	12	4	64	32
x11	1024	12,288	4096	1024	2048	12,288	4096	65,536	32,768

x = Don't care.

Ring Oscillator

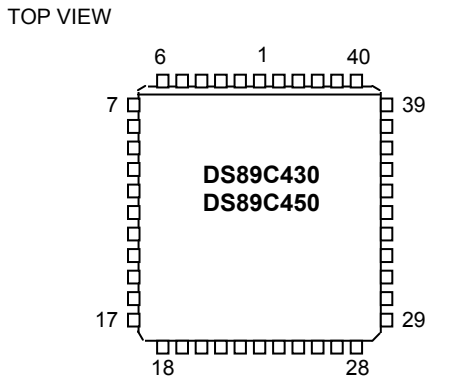
When the system is in stop mode the crystal is disabled. When stop mode is removed, the crystal requires a period of time to start up and stabilize. To allow the system to begin immediate execution of software following the removal of the stop mode, the ring oscillator is used to supply a system clock until the crystal startup time is satisfied. Once this time has passed, the ring oscillator is switched off and the system clock is switched to the crystal oscillator. This function is programmable and is enabled by setting the RGSL bit (EXIF.1) to logic 1. When it is logic 0, the processor delays software execution until after the 65,536 crystal clock periods. To allow the processor to know whether it is being clocked by the ring or by the crystal oscillator, an additional bit—RGMD—indicates which clock source is being used. When the processor is running from the ring, the clock-divide control bits (CD1 and CD0 in the PMR register) are locked into the divide-by-1 mode (CD1:CD0 = 10b). The clock-divide control bits cannot be changed from this state until after the system clock transitions to the crystal oscillator (RGMD = 0).

Note: The watchdog is connected to the crystal oscillator and continues to run at the external clock rate. The ring oscillator does not drive it.

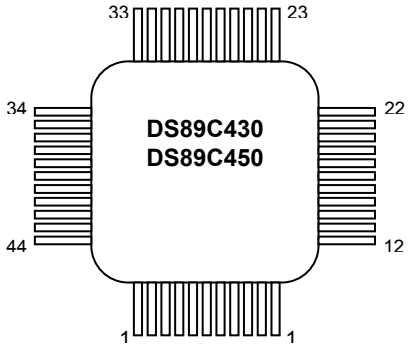
Idle Mode

Idle mode suspends the processor by holding the program counter in a static state. No instructions are fetched and no processing occurs. Setting the IDLE bit (PCON.0) to logic 1 invokes idle mode. The instruction that executes this step is the last instruction prior to freezing the program counter. Once in idle mode, all resources are preserved, but all peripheral clocks remain active and the timers, watchdog, serial ports, and power monitor functions continue to operate, so that the processor can exit the idle mode using any interrupt sources that are enabled. The oscillator-detect circuit also continues to function when enabled. The IDLE bit is cleared automatically once the idle mode is exited. On returning from the interrupt vector using the RETI instruction, the next address is the one that immediately follows the instruction that invoked the idle mode. Any reset of the processor also removes the idle mode.

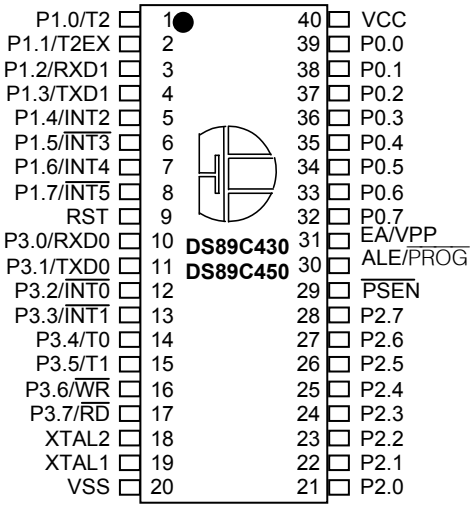
PIN CONFIGURATIONS



PLCC



TQFP



PDIP

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
44 TQFP	C44+2	**21-0293**
40 PDIP	P40+3	**21-0044**
40 PLCC	Q44+7	**21-0049**