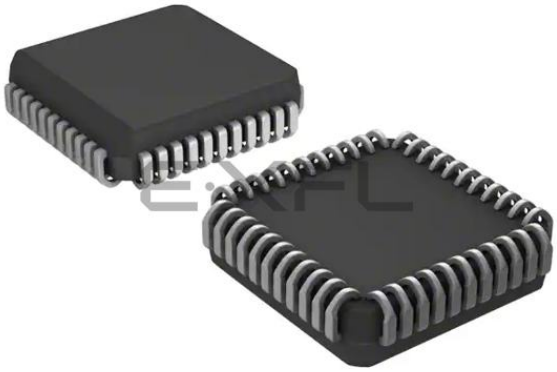

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds89c440-qng

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……..-0.3V to +6.0V
Ambient Temperature Range (under bias)……-40°C to +85°C
Storage Temperature Range……-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (Notes 2, 3)	V_{CC}	4.5	5.0	5.5	V
Power-Fail Warning (Notes 2, 4)	V_{PFW}	4.2	4.375	4.6	V
Reset Trip Point (Min Operating Voltage) (Notes 2, 3, 4)	V_{RST}	3.95	4.125	4.35	V
Supply Current, Active Mode (Note 5)	I_{CC}		75	110	mA
Supply Current, Idle Mode at 33MHz (Note 6)	I_{IDLE}		40	50	mA
Supply Current, Stop Mode, Bandgap Disabled (Note 7)	I_{STOP}		1	100	μA
Supply Current, Stop Mode, Bandgap Enabled (Note 7)	I_{SPBG}		150	300	μA
Input Low Level (Note 2)	V_{IL}	-0.3		+0.8	V
Input High Level (Note 2)	V_{IH}	2.0		V_{CC} + 0.3	V
Input High Level XTAL and RST (Note 2)	V_{IH2}	3.5		V_{CC} + 0.3	V
Output Low Voltage, Port 1 and 3 at I_{OL} = 1.6mA (Note 2)	V_{OL1}		0.15	0.45	V
Output Low Voltage, Port 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA (Note 2)	V_{OL2}		0.15	0.45	V
Output High Voltage, Port 1, 2, and 3, at I_{OH} = -50μA (Notes 2, 8)	V_{OH1}	2.4			V
Output High Voltage, Port 1, 2, and 3 at I_{OH} = -1.5mA (Notes 2, 9)	V_{OH2}	2.4			V
Output High Voltage, Port 0, 1, 2, ALE, $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$ in Bus Mode at I_{OH} = -8mA (Notes 2, 10)	V_{OH3}	2.4			V
Output High Voltage, RST at I_{OL} = -0.4mA (Note 2, 11)	V_{OH4}	2.4			V
Input Low Current, Port 1, 2, and 3 at 0.4V	I_{IL}	-50			μA
Transition Current from 1 to 0, Port 1, 2, and 3 at 2V (Note 12)	I_{TL}	-650			μA
Input Leakage Current, Port 0 in I/O Mode and $\overline{EA}$ (Note 13)	I_L	-10		+10	μA
Input Current, Port 0 in Bus Mode (Note 14)	I_L	-300		+300	μA
RST Pulldown Resistance (Note 13)	R_{RST}	50	120	200	kΩ

Figure 2. Page Mode 1 Timing

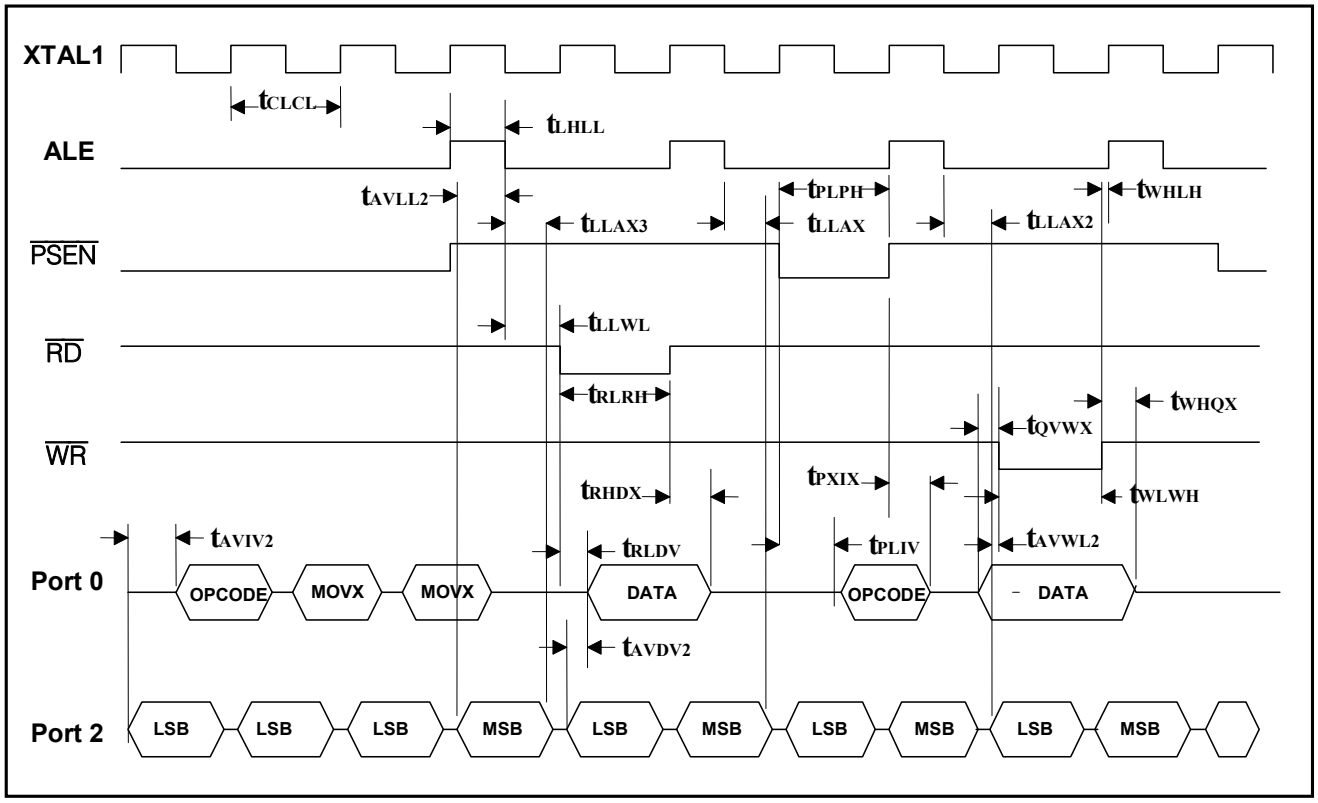
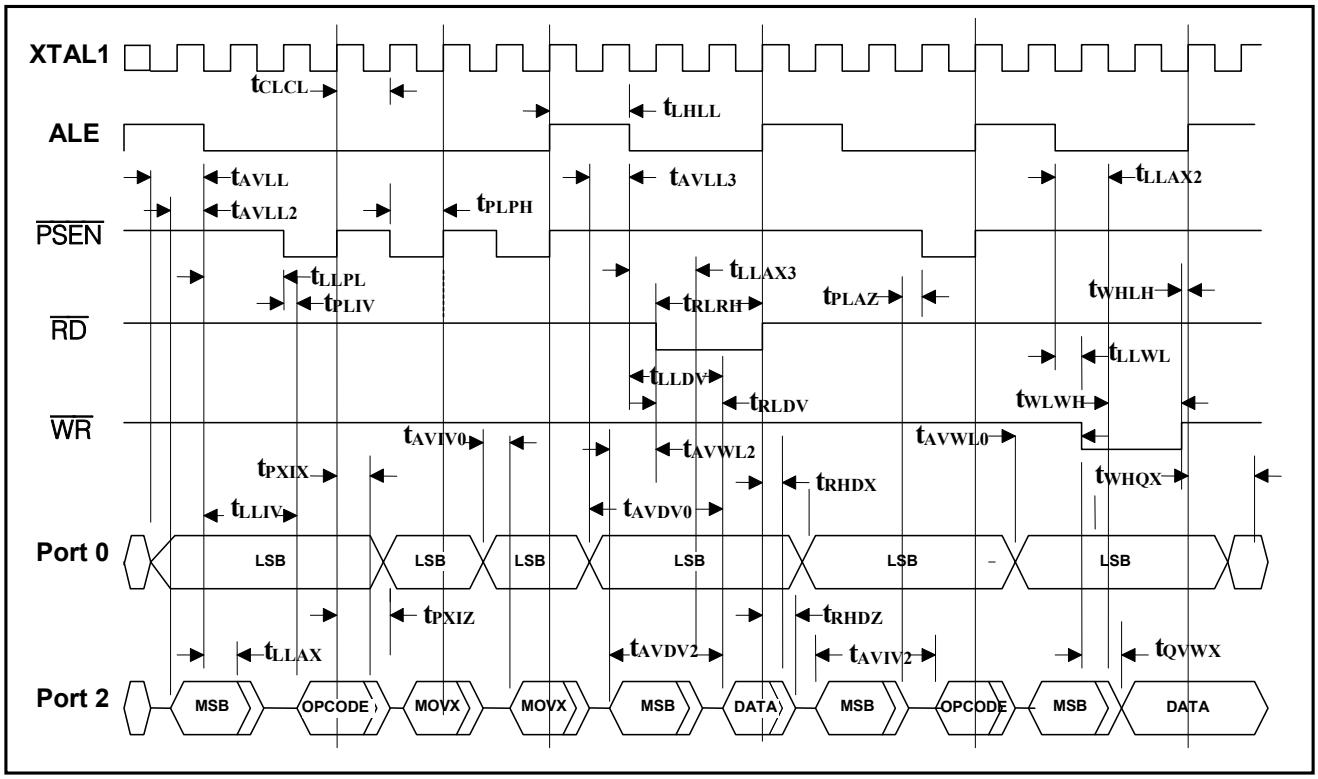


Figure 3. Page Mode 2 Timing



PIN DESCRIPTION

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
40	12, 44	6, 38	V_{CC}	**+5V**
20	1, 22, 23, 34	16, 17, 28, 39	GND	**Logic Ground**
9	10	4	RST	**External Reset.** The RST input pin is bidirectional and contains a Schmitt Trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, as the device provides this function internally.
19	21	15	XTAL1	**Crystal Oscillators.** These pins provide support for fundamental-mode parallel-resonant AT-cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
18	20	14	XTAL2	
29	32	26	$\overline{PSEN}$	**Program Store Enable.** This signal is commonly connected to optional external program memory as a chip enable. $\overline{PSEN}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In one-cycle page mode 1, $\overline{PSEN}$ remains low for consecutive page hits.
30	33	27	ALE/$\overline{PROG}$	**Address Latch Enable.** This signal functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373-family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{PROG}$) is used to execute the parallel program function.
39	43	37	P0.0 (AD0)	**Port 0 (AD0–AD7), I/O.** Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of port 0 is tri-state. Pullup resistors are required only when using port 0 as an I/O port.
38	42	36	P0.1 (AD1)	
37	41	35	P0.2 (AD2)	
36	40	34	P0.3 (AD3)	
35	39	33	P0.4 (AD4)	
34	38	32	P0.5 (AD5)	
33	37	31	P0.6 (AD6)	
32	36	30	P0.7 (AD7)	

Terminology

The term *DS89C430* is used in the remainder of the document to refer to the DS89C430 and DS89C450, unless otherwise specified.

Compatibility

The DS89C430 is a fully static CMOS 8051-compatible microcontroller similar in functional features to the DS87C520, but it offers much higher performance. In most cases, the DS89C430 can drop into an existing socket for the 8xC51 family, immediately improving the operation. While remaining familiar to 8051 family users, the DS89C430 has many new features. In general, software written for existing 8051-based systems works without modification on the DS89C430, with the exception of critical timing routines, as the DS89C430 performs its instructions much faster for any given crystal selection.

The DS89C430 provides three 16-bit timer/counters, two full-duplex serial ports, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports can operate as in standard 8051 products. Timers default to 12 clocks-per-cycle operation to keep their timing compatible with a legacy 8051 family systems. However, timers are individually programmable to run at the new one clock per cycle if desired. The DS89C430 provides several new hardware features, described in subsequent sections, implemented by new special-function registers (SFRs).

Performance Overview

Featuring a completely redesigned high-speed 8051-compatible core, the DS89C430 allows operation at a higher clock frequency. This updated core does not have the wasted memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. The same machine cycle takes one clock in the DS89C430. Thus, the fastest instructions execute 12 times faster for the same crystal frequency (and actually 24 times faster for the INC data pointer instruction). It should be noted that this speed improvement is reduced when using external memory access modes that require more than one clock per cycle.

Individual program improvement depends on the instructions used. Speed-sensitive applications would make the most use of instructions that are 12 times faster. However, the sheer number of 12-to-1 improved op codes makes dramatic speed improvements likely for any code. These architectural improvements produce instruction cycle times as low as 30ns. The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory. The new page modes allow for increased efficiency in external memory accesses.

Instruction Set Summary

All instructions have the same functionality as their 8051 counterparts, including their affect on bits, flags, and other status functions. However, the timing of each instruction is different, in both absolute and relative number of clocks.

For absolute timing of real-time events, the duration of software loops can be calculated using information given in the *Instruction Set* table in the *Ultra-High-Speed Flash Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at a reduced number of clocks per increment to take advantage of faster processor operation.

The relative time of some instructions may be different in the new architecture. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS89C430, the MOVX instruction takes as little as two machine cycles or two oscillator cycles, but the "MOV direct, direct" uses three machine cycles or three oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS89C430 usually uses one machine cycle for each instruction byte and requires one cycle for execution. *The user concerned with precise program timing should examine the timing of each instruction to become familiar with the changes*.

Special-Function Registers (SFRs)

All peripherals and operations that are not explicit instructions in the DS89C430 are controlled through SFRs. The most common features basic to the architecture are mapped to the SFRs. These include the CPU registers (ACC, B, and PSW), data pointers, stack pointer, I/O ports, timer/counters, and serial ports. In many cases, an SFR controls an individual function or reports the function's status. The SFRs reside in register locations 80h–FFh and are only accessible by direct addressing. SFRs with addresses ending in 0h or 8h are bit addressable.

All standard SFR locations from the 8051 are duplicated in the DS89C430, and several SFRs have been added for the unique features of the DS89C430. Most of these features are controlled by bits in SFRs located in unused locations in the 8051 SFR map, allowing for increased functionality while maintaining complete instruction set compatibility. Table 1 shows the SFRs and their locations. Table 2 specifies the default reset condition for all SFR bits.

Data Pointers

The data pointers (DPTR and DPTR1) are used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM location (on-chip or off-chip) or a memory-mapped peripheral. Two pointers are useful when moving data from one memory area to another, or when using a memory-mapped peripheral for both source and destination addresses. The user can select the active pointer through a dedicated SFR bit (SEL = DPS.0), or can activate an automatic toggling feature for altering the pointer selection (TSL = DPS.5). An additional feature, if selected, provides automatic incrementing or decrementing of the current DPTR.

Stack Pointer

The stack pointer denotes the register location at the top of the stack, which is the last used value. The user can place the stack anywhere in the scratchpad RAM by setting the stack pointer to the desired location, although the lower bytes are normally used for working registers.

I/O Ports

The DS89C430 offers four 8-bit I/O ports. Each I/O port is represented by an SFR location and can be written or read. The I/O port has a latch that contains the value written by software.

Counter/Timers

Three 16-bit timer/counters are available in the DS89C430. Each timer is contained in two SFR locations that can be read or written by software. The timers are controlled by other SFRs, described in the *SFR Bit Description* section of the *Ultra-High-Speed Flash Microcontroller User's Guide*.

Serial Ports

The DS89C430 provides two UARTs that are controlled and accessed by SFRs. Each UART has an address that is used to read and write the value contained in the UART. The same address is used for both read and write operations, and the read and write operations are distinguished by the instruction. Its own SFR control register controls each UART.

Table 1. SFR Register Map

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
SP	81h								
DPL	82h								
DPH	83h								
DPL1	84h								
DPH1	85h								
DPS	86h	ID1	ID0	TSL	AID	—	—	—	SEL
PCON	87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TL0	8Ah								
TL1	8Bh								
TH0	8Ch								

Table 1. SFR Register Map (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TH1	8Dh								
CKCON	8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
P1	90h	P1.7/$\overline{INT5}$	P1.6/INT4	P1.5/$\overline{INT3}$	P1.4/INT2	P1.3/TXD1	P1.2/RXD1	P1.1/T2EX	P1.0/T2
EXIF	91h	IE5	IE4	IE3	IE2	CKRY	RGMD	RGSL	BGS
CKMOD	96h			T2MH	T1MH	T0MH	—	—	—
SCON0	98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
SBUF0	99h								
ACON	9Dh	PAGEE	PAGES1	PAGES0	—	—	—	—	—
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
SADDR0	A9h								
SADDR1	AAh								
P3	B0h	P3.7/$\overline{RD}$	P3.6/$\overline{WR}$	P3.5/T1	P3.4/T0	P3.3/$\overline{INT1}$	P3.2/$\overline{INT0}$	P3.1/TXD0	P3.0/RXD0
IP1	B1h	—	MPS1	MPT2	MPS0	MPT1	MPX1	MPT0	MPX0
IP0	B8h	—	LPS1	LPT2	LPS0	LPT1	LPX1	LPT0	LPX0
SADEN0	B9h								
SADEN1	BAh								
SCON1	C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
SBUF1	C1h								
ROMSIZE	C2h					PRAME	RMS2	RMS1	RMS0
PMR	C4h	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEON	DME1	DME0
STATUS	C5h	PIS2	PIS1	PIS0	—	SPTA1	SPRA1	SPTA0	SPRA0
TA	C7h								
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9h							T2OE	DCEN
RCAP2L	CAh								
RCAP2H	CBh								
TL2	CCh								
TH2	CDh								
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P
FCNTL	D5h	$\overline{FBUSY}$	FERR			FC3	FC2	FC1	FC0
FDATA	D6h								
WDCON	D8h	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
ACC	E0h								
EIE	E8h	—	—	—	EWDI	EX5	EX4	EX3	EX2
B	F0h								
EIP1	F1h	—	—	—	MPWDI	MPX5	MPX4	MPX3	MPX2
EIP0	F8h	—	—	—	LPWDI	LPX5	LPX4	LPX3	LPX2

Note: Shaded bits are timed-access protected.

The signature bytes can be read in ROM loader mode or in parallel programming mode. Reading data from addresses 30h, 31h, and 60h provides signature information on manufacturer, part, and extension as follows:

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer ID
31h	43h	DS89C430 Device ID
31h	44h	DS89C440 Device ID (Contact factory or replace with DS89C430 or DS89C450.)
31h	45h	DS89C450 Device ID
60h	01h	Device Extension

Note: *The read/write accessibility of the flash memory during in-application programming is not affected by the state of the lock bits. However, the lock bits do affect the read/write accessibility in ROM loader and parallel programming modes.*

In-Application Programming by User Software

The DS89C430 supports in-application programming of on-chip flash memory by user software. In-application programming is initiated by writing a flash command into the flash control (FCNTL:D5h) register to enable the flash memory for erase/program/verify operations. Address and data are input into the MMU through the flash data (FDATA:D6h) register. The flash command also enables read/write accesses to the FDATA. The MMU's sequencer provides the operation sequences and control functions to the flash memory. The MMU is designed to operate independently from the processor, except for read/write access to the SFRs.

Only the upper bank of the on-chip program memory can be in-application programmed by the user software. The lower bank of the on-chip program memory contains system hardware-dependent codes that are crucial to system operation and should not be altered during in-application programming.

All flash operations are self-timed. The user software can monitor the progress of an erase or programming operation through the flash busy (FBUSY;FCNTL.7) bit with a reset value at logic 1. A selected operation automatically starts when required data is written to the FDATA SFR. The MMU clears the FBUSY bit to indicate the start of a write/erase operation. The FBUSY bit may not change state for up to 1μs after the operation is requested. During this time, the application should poll the status of the FBUSY bit waiting for it to change state. This bit is held low until either the end of the operation or until an error indicator is returned. A flash operating failure terminates the current operation and sets the flash error flag (FERR;FCNTL.6) to logic 1. Both the busy and error flags are read-only bits.

Read/write access during in-application programming is not affected by the state of the lock bits.

A sample programming sequence for a "write upper program memory bank" is shown below. The command must be reentered each time an operation is requested, i.e., it is not permissible to issue the "write upper program memory bank" command once and then repeatedly load address and data values to program a block of memory.

1. Make sure the $\overline{\text{FBUSY}}$ bit is 1 to indicate flash MMU is idle.
2. Write 0Bh to the FCNTL register using the timed access sequence.
3. Write address_MSB to the FDATA register.
4. Write address_LSB to the FDATA register.
5. Write data_value to the FDATA register.
6. Make sure the $\overline{\text{FBUSY}}$ bit is 0 to indicate programming has started.
7. Wait for $\overline{\text{FBUSY}}$ bit to return to 1 to indicate end of programming operation.
8. Make sure FERR is 0 to indicate no programming error.

The flash command (FC3–FC0;FCNTL.3:0) bits provide flash commands as listed in Table 4.

External Memory

The DS89C430 executes external memory cycles for code fetches and read/writes of external program and data memory. A nonpage external memory cycle is four times slower than the internal memory cycles (i.e., an external memory cycle contains four system clocks). However, a page mode external memory cycle can be completed in one, two, or four system clocks for a page hit and two, four, or eight system clocks for a page miss, depending on user selection. The DS89C430 also supports a second page mode operation with a different external bus structure that provides for fast external code fetches but uses four system clock cycles for data memory access.

External Program Memory Interface (Nonpage Mode)

Figure 7 shows the timing relationship for internal and external code fetches when CD1 and CD0 are set to 10b, assuming the microcontroller is in nonpage mode for external fetches. Note that an external program fetch takes four system clocks, and an internal program fetch requires only one system clock.

As illustrated in Figure 7, ALE is deasserted when executing an internal memory fetch. The DS89C430 provides a programmable user option to turn on ALE during internal program memory operation. ALE is automatically enabled for code fetch externally, independent of the setting of this option.

$\overline{\text{PSEN}}$ is only asserted for external code fetches, and is inactive during internal execution.

Figure 7. External Program Memory Access (Nonpage Mode, CD1:CD0 = 10)

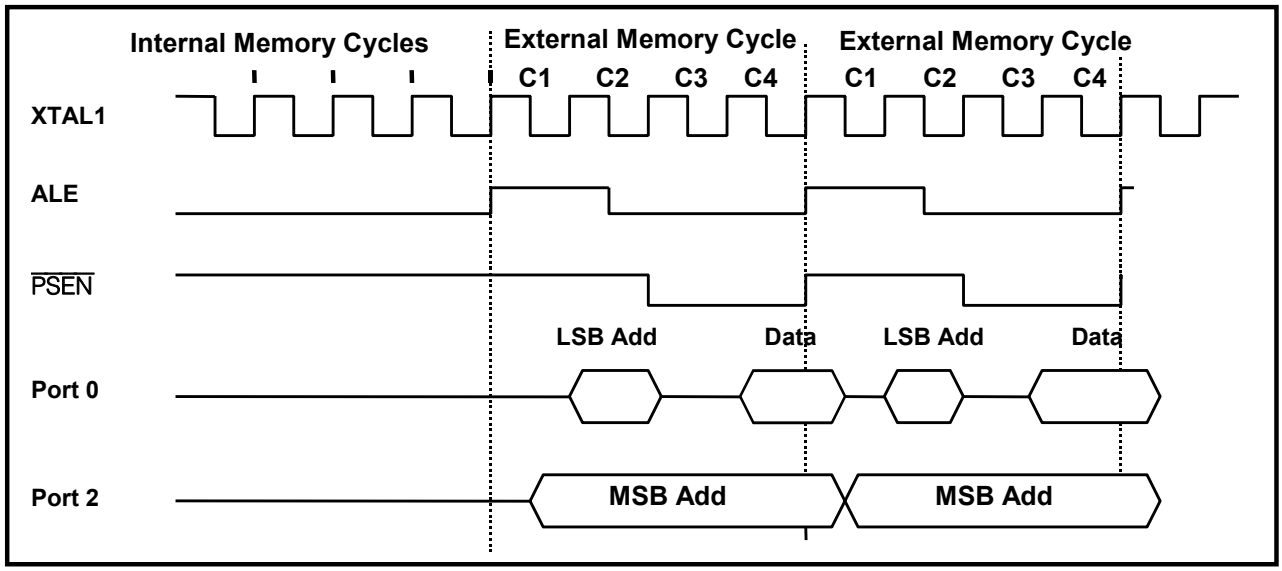
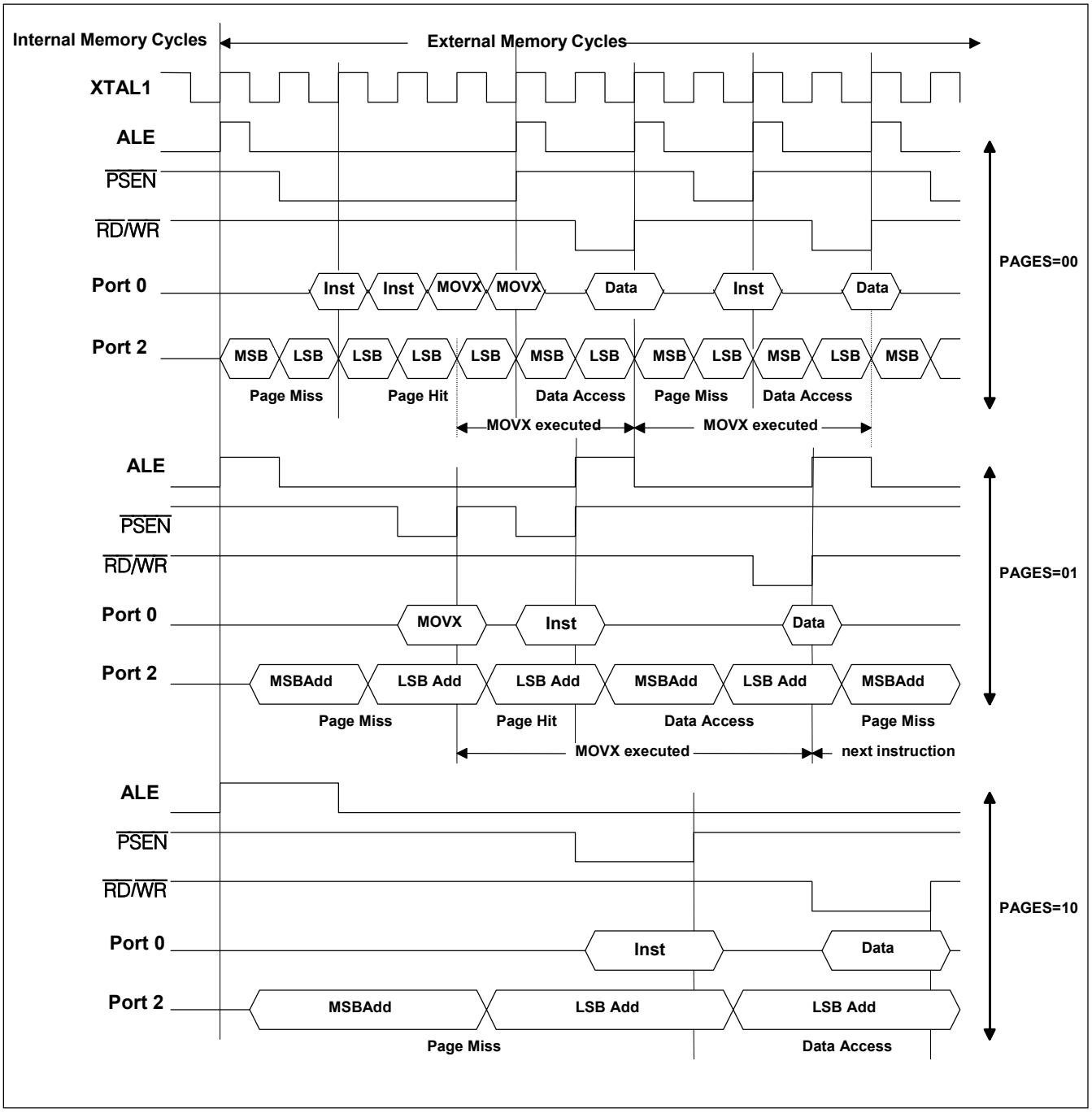


Figure 10. Page Mode 1, External Memory Cycle (CD1:CD0 = 10)



During a page miss, P2 drives the Addr [8:15] of the 16-bit address and holds it for the duration of the first half of the memory cycle to allow the external address latches to latch the new most significant address byte. ALE is asserted to strobe the external address latches. During this operation, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ are held in inactive states and P0 is in a high-impedance state. The following half-memory cycle is executed as a page hit cycle and the appropriate operation takes place.

A page miss can occur at set intervals or during external operations that require a memory access into a page of memory that has not been accessed during the last external cycle. Generally, the first external memory access causes a page miss. The new page address is stored internally and is used to detect a page miss for the current external memory cycle.

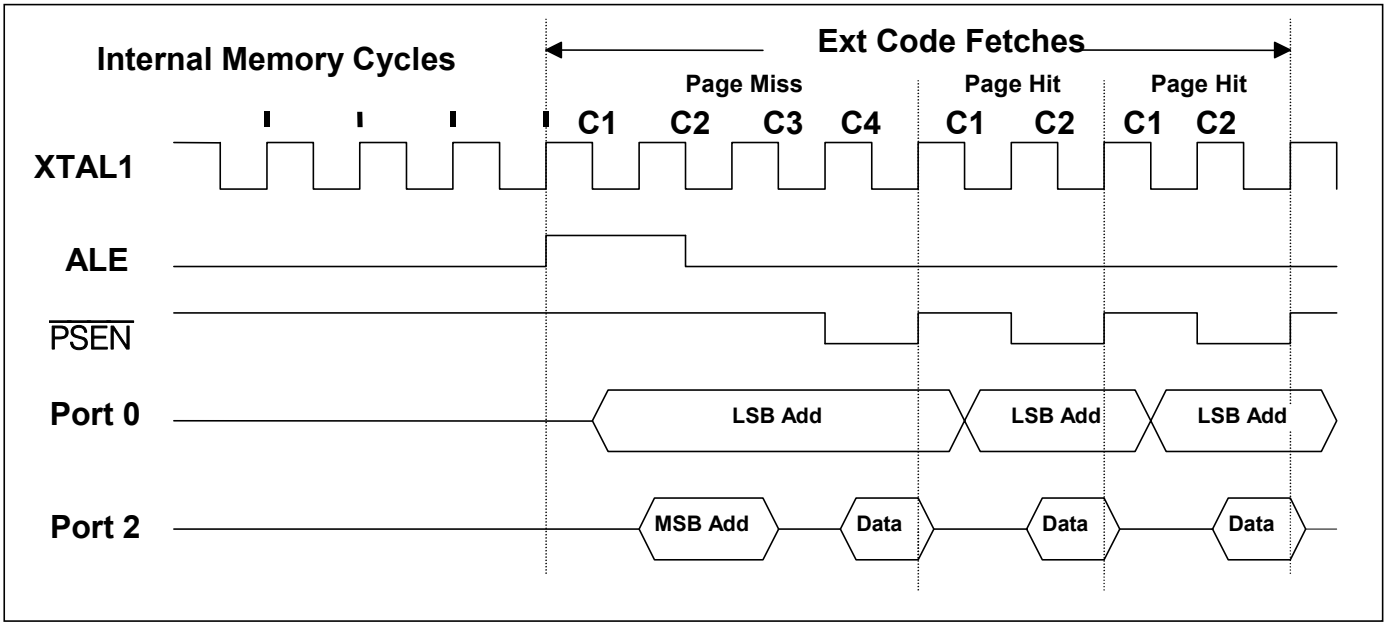
Note that there are a few exceptions for this mode of operation when PAGES1 and PAGES2 are set to 00b:

- $\overline{\text{PSEN}}$ is asserted for both a page hit and a page miss for a full clock cycle.
- The execution of external MOVX instruction causes a page miss.
- A page miss occurs when fetching the next external instruction following the execution of an external MOVX instruction.

Figure 10 shows the external memory cycle for this bus structure. The first case illustrates a back-to-back execution sequence for the one-cycle page mode (PAGES1 = PAGES0 = 0b). $\overline{\text{PSEN}}$ remains active during page hit cycles, and page misses are forced during and after MOVX executions, independent of the most significant byte of the subsequent addresses. The second case illustrates a MOVX execution sequence for two-cycle page mode (PAGES1 = 0 and PAGES0 = 1). $\overline{\text{PSEN}}$ is active for a full clock cycle in code fetches. Note that changing the most significant byte of the data address causes the page misses in this sequence. The third case illustrates a MOVX execution sequence for four-cycle page mode (PAGES1 = 1 and PAGES0 = 0). There is no page miss in this execution cycle as the most significant byte of the data address is assumed to match the last program address.

The second page mode (page mode 2) external bus structure multiplexes the most significant address byte with data on P2 and uses P0 for the least significant address byte. This bus structure is used to speed up external code fetches only. External data memory access cycles are identical to the nonpage mode except for the different signals on P0 and P2. Figure 11 illustrates the memory cycle for external code fetches.

Figure 11. Page Mode 2, External Code Fetch Cycle (CD1:CD0 = 10)



Stretch External Data Memory Cycle in Page Mode

The DS89C430 allows software to adjust the speed of external data memory access by stretching the memory bus cycle in page mode operation just like nonpage mode operation. The following tables summarize the stretch values and their effect on the external MOVX memory bus cycle and the control signals' pulse width in terms of the number of oscillator clocks. A stretch machine cycle always contains four system clocks, independent of the logic value of the page mode select bits.

Table 10. Page Mode 2, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 11)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

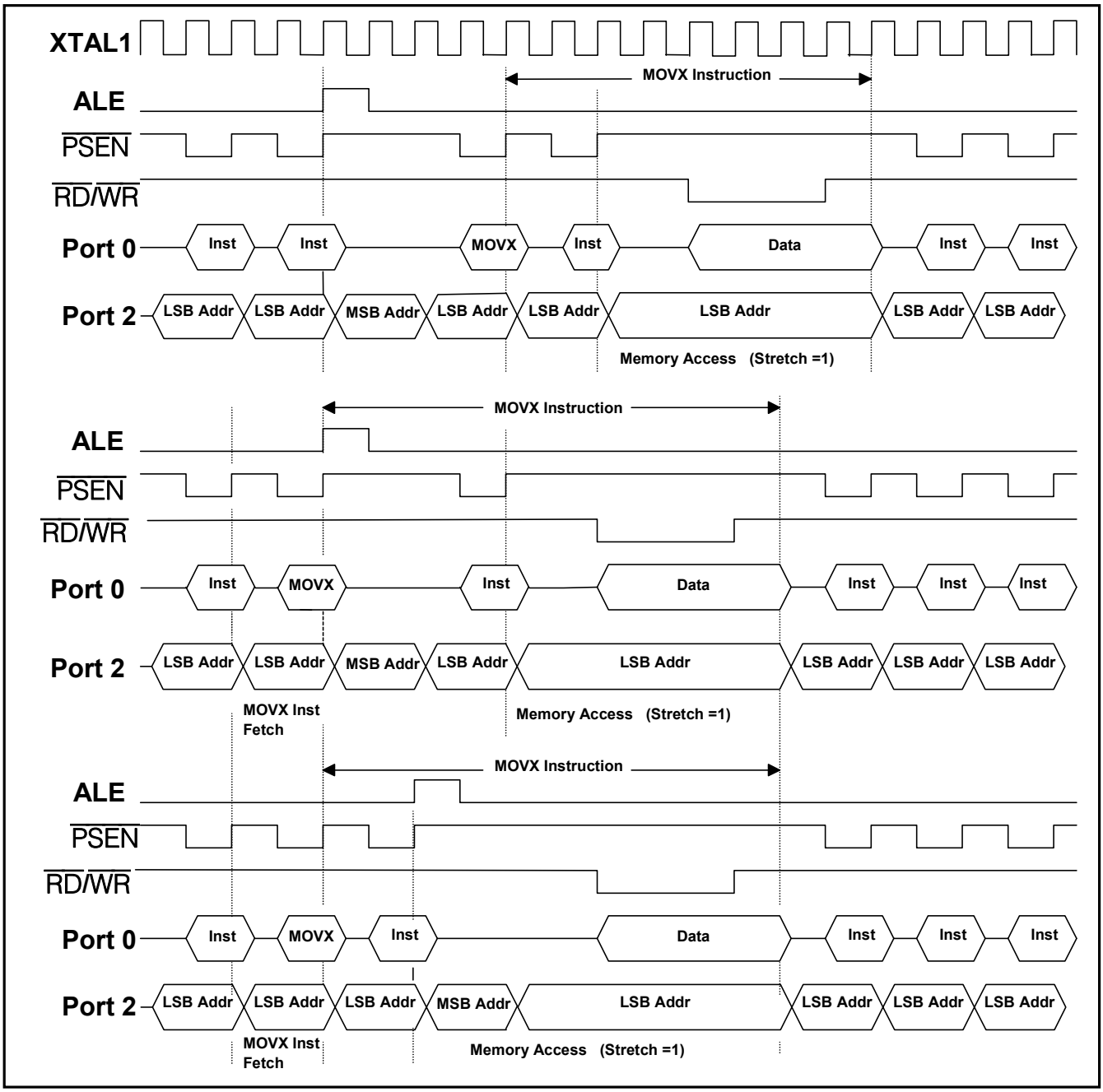
As shown in the previous tables, the stretch feature supports eight stretched external data-memory access options, which can be categorized into three timing groups. When the stretch value is cleared to 000b, there is no stretch on external data memory access, and a MOVX instruction is completed in two basic memory cycles. When the stretch value is set to 1, 2, or 3, the external data memory access is extended by 1, 2, or 3 stretch memory cycles, respectively. Note that the first stretch value does not result in adding four system clocks to the control signals. This is because the first stretch uses one system clock to create additional address setup and data bus float time and one system clock to create additional address and data hold time. When using very slow RAM and peripherals, a larger stretch value (4–7) can be selected. In this stretch category, two stretch cycles are used to create additional setup (the ALE pulse width is also stretched by one stretch cycle for page miss) and one stretch cycle is used to create additional hold time. The following timing diagrams illustrate the external data memory access at divide-by-1 system clock mode (CD1:CD0 = 10b).

Figure 12 illustrates the external data-memory stretch-cycle timing relationship when PAGEE = 1 and PAGES1:PAGES0 = 01. The stretch cycle shown is for a stretch value of 1 and is coincident with a page miss. Note that the first stretch value does not result in adding four system clocks to the $\overline{RD}/\overline{WR}$ control signals. This is because the first stretch uses one system clock to create additional setup and one system clock to create additional hold time.

Figure 13 shows the timing relationship for a slow peripheral interface (stretch value = 4). Note that a page hit data memory cycle is shorter than a page miss data memory cycle. The ALE pulse width is also stretched by a stretch cycle in the case of a page miss.

The stretched data memory bus cycle timing relationship for PAGES = 11 is identical to nonpage mode operation since the basic data memory cycle always contains four system clocks in this page mode operation.

Figure 12. Page Mode 1, External Data Memory Access (PAGES = 01, STRETCH = 1, CD = 10)



Interrupt Priority

There are five levels of interrupt priority: Level 4 to 0. The highest interrupt priority is level 4, which is reserved for the power-fail interrupt. All other interrupts have individual priority bits in the interrupt priority registers to allow each interrupt to be assigned a priority level from 3 to 0. The power-fail interrupt always has the highest priority if it is enabled. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in Table 11.

The processor indicates that an interrupt condition occurred by setting the respective flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Unless marked in Table 11, all these flags must be cleared by software.

Table 11. Interrupt Summary

INTERRUPT	VECTOR	NATURAL ORDER	FLAG	ENABLE	PRIORITY CONTROL
Power Fail	33h	0 (Highest)	PFI (WDCON.4)	EPFI(WDCON.5)	N/A
External Interrupt 0	03h	1	IE0 (TCON.1) (Note 1)	EX0 (IE.0)	LPX0 (IP0.0); MPX0 (IP1.0)
Timer 0 Overflow	0Bh	2	TF0 (TCON.5) (Note 2)	ET0 (IE.1)	LPT0 (IP0.1); MPT0 (IP1.1)
External Interrupt 1	13h	3	IE1 (TCON.3) (Note 1)	EX1 (IE.2)	LPX1 (IP0.2); MPX1 (IP1.2)
Timer 1 Overflow	1Bh	4	TF1 (TCON.7) (Note 2)	ET1 (IE.3)	LPT1 (IP0.3); MPT1 (IP1.3)
Serial Port 0	23h	5	RI_0 (SCON0.0); TI_0 (SCON0.1)	ES0 (IE.4)	LPS0 (IP0.4); MPS0 (IP1.4)
Timer 2 Overflow	2Bh	6	TF2 (T2CON.7); EXF2 (T2CON.6)	ET2 (IE.5)	LPT2 (IP0.5); MPT2 (IP1.5)
Serial Port 1	3Bh	7	RI_1 (SCON1.0); TI_1 (SCON1.1)	ES1 (IE.6)	LPS1 (IP0.6); MPS1 (IP1.6)
External Interrupt 2	43h	8	IE2 (EXIF.4)	EX2 (EIE.0)	LPX2 (EIP0.0); MPX2 (EIP1.0)
External Interrupt 3	4Bh	9	IE3 (EXIF.5)	EX3 (EIE.1)	LPX3 (EIP0.1); MPX3 (EIP1.1)
External Interrupt 4	53h	10	IE4 (EXIF.6)	EX4 (EIE.2)	LPX4 (EIP0.2); MPX4 (EIP1.2)
External Interrupt 5	5Bh	11	IE5 (EXIF.7)	EX5 (EIE.3)	LPX5 (EIP0.3); MPX5 (EIP1.3)
Watchdog	63h	12 (Lowest)	WDIF (WDCON.3)	EWDI (EIE.4)	LPWDI (EIP0.4); MPWDI (EIP1.4)

Note 1: If the interrupt is edge triggered, the flag is cleared automatically by hardware when the service routine is vectored to. If the interrupt is level triggered, the flag follows the state of the pin.
Note 2: The flag is cleared automatically by hardware when the service routine is vectored to.

Timer/Counters

The DS89C430 incorporates three 16-bit timers. All three timers can be used as either counters of external events, where 1-to-0 transitions on a port pin are monitored and counted, or timers that count oscillator cycles. Table 12 summarizes the timer functions.

Timers 0 and 1 both have three modes of operations. They can each be used as a 13-bit timer/counter, a 16-bit timer/counter, or an 8-bit timer/counter with autoreload. Timer 0 has a fourth operating mode as two 8-bit timer/counters without autoreload. Each timer can also be used as a counter of external pulses on the corresponding T0/T1 pin for 1-to-0 transitions. The timer mode (TMOD) register controls the mode of operation. Each timer consists of a 16-bit register in 2 bytes, which can be found in the SFR map as TL0, TH0, TL1, and TH1. The timer control (TCON) register enables timers 0 and 1.

Table 12. Timer Functions

FUNCTIONS	TIMER 0	TIMER 1	TIMER 2
Timer/Counter	13/16/8*/2x8 bit	13/16/8* bit	16 bit
Timer with Capture	No	No	Yes
External Control Pulse Counter	Yes	Yes	No
Up/Down Autoreload Timer/Counter	No	No	Yes
Baud Rate Generator	No	Yes	Yes
Timer Output Clock Generator	No	No	Yes

**8-bit timer/counter includes autoreload feature. 2x8-bit mode does not.*

Each timer has a selectable time base (Table 14). Following a reset, the timers default to divide by 12 to maintain drop-in compatibility with the 8051. If timer 2 is used as a baud rate generator or clock output, its time base is fixed at divide by 2, regardless of the setting of its timer mode bits.

Timer 2 is a true 16-bit timer/counter that, with a 16-bit capture (RCAP2L and RCAP2H) register, is able to provide some unique functions like up/down autoreload timer/counter and timer output-clock generation. Timer 2 (registers TL2 and TH2) is enabled by the T2CON register. Its mode of operation is selected by the T2MOD register.

For operation details, refer to *Section 11: Programmable Timers* in the *Ultra-High-Speed Flash Microcontroller User's Guide.*

Timed Access

The timed-access function prevents an errant CPU from making accidental changes to certain SFR bits that are considered vital to proper system operation. This is achieved by using software control when accessing the following SFR control bits:

SFR	BIT	FUNCTION
WDCON.0	RWT	Reset Watchdog Timer
WDCON.1	EWT	Watchdog Reset Enable
WDCON.3	WDIF	Watchdog Interrupt Flag
WDCON.6	POR	Power-On Reset Flag
EXIF.0	BGS	Bandgap Select
ACON.5	PAGES0	Page Mode Select Bit 0
ACON.6	PAGES1	Page Mode Select Bit 1
ACON.7	PAGEE	Page Mode Enable
ROMSIZE.0	RMS0	Program Memory Size Select Bit 0
ROMSIZE.1	RMS1	Program Memory Size Select Bit 1
ROMSIZE.2	RMS2	Program Memory Size Select Bit 2
ROMSIZE.3	PRAME	Program RAM Enable
FCNTL.0	FC0	Flash Command Bit 0
FCNTL.1	FC1	Flash Command Bit 1
FCNTL.2	FC2	Flash Command Bit 2
FCNTL.3	FC3	Flash Command Bit 3

Before these bits can be altered, the processor must execute the timed-access sequence. This sequence consists of writing an AAh to the timed access (TA, C7h) register, followed by writing a 55h to the same register within three machine cycles. This timed sequence of steps allows any of the timed access-protected SFR bits to be altered

during the three machine cycles following the writing of the 55h. Writing to a timed-access-protected bit outside of these three machine cycles has no effect on the bit.

The timed-access process is address, data, and time dependent. A processor running out of control and not executing system software statistically is not able to perform this timed sequence of steps, and as such, does not accidentally alter the protected bits. It should be noted that this method should be used in the main body of the system software and *never* used in an interrupt routine in conjunction with the watchdog reset. Interrupt routines using the timed-access watchdog-reset bit (RWT) can recover a lost system and allow the resetting of the watchdog, but the system returns to a lost condition once the RETI is executed, unless the stack is modified. Also, it is advisable that interrupts be disabled (EA = 0) when executing the timed-access sequence, since an interrupt during the sequence adds time, making the timed-access attempt fail.

Power Management and Clock-Divide Control

Power-management features are available that monitor the power-supply voltage levels and support low-power operation with three power-saving modes. Such features include a bandgap voltage monitor, watchdog timer, selectable internal ring oscillator, and programmable system clock speed. The SFRs that provide control and application software access are the watchdog control (WDCON, D8h), extended interrupt enable (EIE, E8h), extended interrupt flag (EXIF, 91h) and power control (PCON, 87h) registers.

System Clock-Divide Control

The programmable clock-divide control bits (CD1 and CD0) provide the processor with the ability to adapt to different crystals and to slow the system clocks, providing lower power operation when required. An on-chip crystal multiplier allows the DS89C430 to operate at two or four times the crystal frequency by setting the 4X/$\overline{2X}$ bit, and is enabled by setting the CTM bit to a logic 1. An additional circuit provides a clock source at divide by 1024. When used with a 7.372MHz crystal, for example, the processor executes the machine cycle in times ranging from 33.9ns (mulitply-by-4 mode) to 138.9µs (divide-by-1024 mode) and maintains a highly accurate serial port baud rate, while allowing the use of more cost-effective lower frequency crystals. Although the clock-divide control bits can be written at any time, certain hardware features enhance the use of these clock controls to guarantee proper serial port operation and to allow for a high-speed response to an external interrupt. The 01b setting of CD1 and CD0 is reserved. It has the same effect as the setting of 10b, which forces the system clock into a divide-by-1 mode. The DS89C430 defaults to divide-by-1 clock mode on all forms of reset.

When in divide-by-1024 mode, in order to allow a quick response to incoming data on a serial port, the system uses the switchback mode to automatically revert to divide-by-1 mode whenever a start bit is detected. This automatic switchback is only enabled in divide-by-1024 mode when the switchback bit (PMR.5:SWB) is set. All other clock modes are unaffected by interrupts and serial port activity.

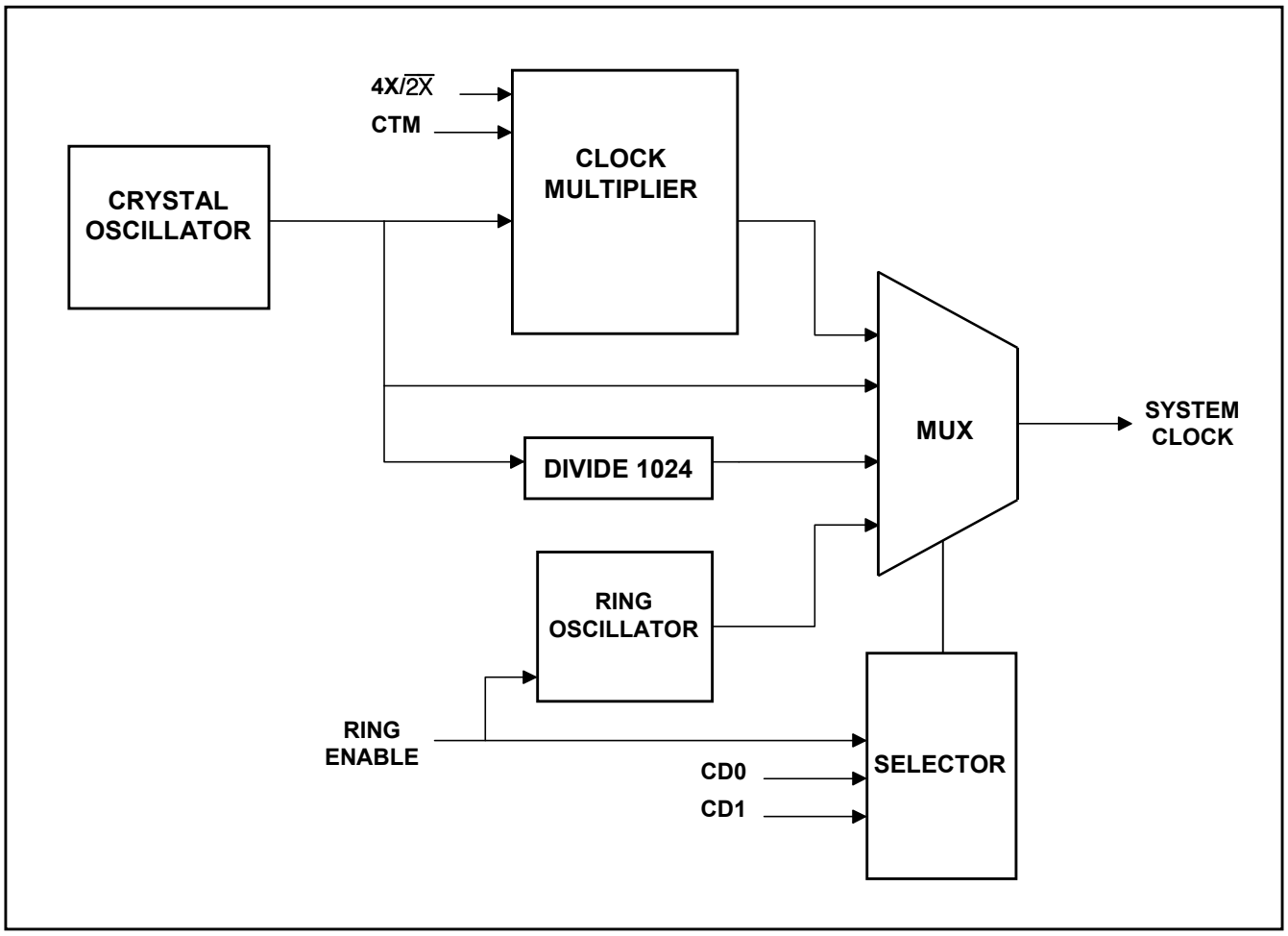
The oscillator multiply ratios of 4, 2, and 1 are also used to provide standard baud-rate generation for the serial ports through a forced divide-by-12 input clock (TxMH,TxM = 00b, x = 1, 2, or 3) to the timers.

Use of the multiply-by-4 or multiply-by-2 options through the clock-divide control bits requires that the crystal multiplier be enabled and the specific system-clock-multiply value be established by the 4X/$\overline{2X}$ bit in the PMR register. The multiplier is enabled through the CTM (PMR.4) bit but cannot be automatically selected until a startup delay has been established through the CKRY bit in the status register. The 4X/$\overline{2X}$ bit can only be altered when the CTM bit is cleared to a logic 0. This prevents the system from changing the multiplier until the system has moved back to the divide-by-1 mode and the multiplier has been disabled by the CTM bit. The CTM bit can only be altered when the CD1 and CD0 bits are set to divide-by-1 mode and the RGMD bit is cleared to 0. Setting the CTM to a logic 1 from a previous logic 0 automatically clears the CKRY bit in the status register and starts the multiplier startup timeout in the multiplier startup counter. During the multiplier startup period, the CKRY bit remains cleared and the CD1 and CD0 clock controls cannot be set to 00b. The CTM bit is cleared to a logic 0 on all resets.

Note that the rated maximum speed of operation applies to the speed of the microcontroller core, not the external clock source. When using the clock multiplier feature, the external clock source frequency, multiplied by the clock multiplier (2X or 4X) can never be faster than the maximum rated speed of the device. Thus, if a designer wished to use the 4X clock multiplier on a device rated at 33MHz, the maximum external clock speed would be 8.25MHz.

Figure 14 gives a simplified description of the generation of the system clocks. Specifics of hardware restrictions associated with the use of the 4X/$\overline{2X}$ CTM, CKRY, CD1, and CD0 bits are outlined in the *SFR* section.

Figure 14. System Clock Sources



Bandgap-Monitored Interrupt and Reset Generation

The power monitor in the DS89C430 monitors the V_{CC} pin in relation to the on-chip bandgap voltage reference. Whenever V_{CC} falls below V_{PFW}, an interrupt is generated if the corresponding power-fail interrupt-enable bit EPFI (WDCON.5) is set, causing the device to vector to address 33h. The power-fail interrupt status bit PFI (WDCON.4) is set any time V_{CC} transitions below V_{PFW}, and can only be cleared by software once set. Similarly, as V_{CC} falls below V_{RST}, a reset is issued internally to halt program execution. Following power-up, a power-on reset initiates a power-on reset timeout before starting program execution. When V_{CC} is first applied to the DS89C430, the processor is held in reset until $V_{CC} > V_{RST}$ and a delay of 65,536 oscillator cycles has elapsed, to ensure that power is within tolerance and the clock source has had time to stabilize. Once the reset timeout period has elapsed, the reset condition is removed automatically and software execution begins at the reset vector location of 0000h. The power-on reset flag POR (WDCON.6) is set to logic 1 to indicate a power-on reset has occurred, and can only be cleared by software.

When the DS89C430 enters stop mode, the bandgap, reset comparator, and power-fail interrupt comparator are automatically disabled to conserve power if the BGS (EXIF.0) bit is set to logic 0. This is the lowest power mode. If BGS is set to logic 1, the bandgap reference, reset comparator, and the power-fail comparator are powered up, although in a mode that reduces their power consumption.

Watchdog Timer

The watchdog timer functions as the source of both the watchdog interrupt and the watchdog reset. When the clock divider is set to 10b, the interrupt timeout has a default divide ratio of 2^{17} of the crystal oscillator clock, with the watchdog reset set to time out 512 system clock cycles later. This results in a 33MHz crystal oscillator producing an interrupt timeout every 3.9718ms, followed 15.5µs later by a watchdog reset. The watchdog timer is reset to the default divide ratio following any reset. Using the WD0 and WD1 bits in the clock control (CKCON.6 and 7) register, other divide ratios can be selected for longer watchdog interrupt periods. Table 13 summarizes the watchdog bits settings and the timeout values. **Note:** All watchdog timer reset timeouts follow the programmed interrupt timeouts by 512 system clock cycles, which equates to varying numbers of oscillator cycles depending on the clock divide (CD1:0) and crystal multiplier settings.

Table 13. Watchdog Timeout Value (In Number of Oscillator Clocks)

4X/$\overline{2X}$	CD1:0	WATCHDOG INTERRUPT TIMEOUT				WATCHDOG RESET TIMEOUT			
		WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11	WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11
1	00	2^{15}	2^{18}	2^{21}	2^{24}	2^{15} + 128	2^{18} + 128	2^{21} + 128	2^{24} + 128
0	00	2^{16}	2^{19}	2^{22}	2^{25}	2^{16} + 256	2^{19} + 256	2^{22} + 256	2^{25} + 256
x	01	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	10	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	11	2^{27}	2^{30}	2^{33}	2^{36}	2^{27} + 524,288	2^{30} + 524,288	2^{33} + 524,288	2^{36} + 524,288

A watchdog control (WDCON) SFR is used for programming the functions. EWT (WDCON.1) is the enable for the watchdog timer-reset function and RWT (WDCON.0) is the bit used to restart the watchdog timer. Setting the RWT bit restarts the timer for another full interval. If the watchdog timer-reset function is masked by the EWT bit and no resets are issued to the timer through the RWT bit, the watchdog timer generates interrupt timeouts at a rate determined by the programmed divide ratio. WDIF (WDCON.3) is the interrupt flag set at timer termination and WTRF (WDCON.2) is the reset flag set following a watchdog reset timeout. Setting the EWDI bit (EIE.4) enables the watchdog interrupt. The watchdog timer reset and interrupt timeouts are measured by counting system clock cycles.

An independent watchdog timer functions as the crystal startup counter to count 65,536 crystal clock cycles before allowing the crystal oscillator to function as the system clock. This warmup time is verified by the watchdog timer following each power-up as well as each time the crystal is restarted following a stop mode. The watchdog is also used to establish a startup time whenever the CTM in the PMR register is set to enable the crystal multiplier (4X/$\overline{2X}$).

One of the watchdog timer applications is for the watchdog to wake up the system from idle mode. The watchdog interrupt can be programmed to allow a system to wake up periodically to sample the external world.

Internal System Reset

A software reset can be initiated by writing a system reset command to the flash control SFR. The reset state is maintained for approximately 90 external clock cycles. During this time, the RST pin is driven to a logic high. Once the reset is removed, the RST pin is driven low, and operation begins from address 0000h.

External/Hardware Reset

A hardware reset can be initiated by asserting the RST pin high for at least three external clock cycles while the external clock is running. The reset is asserted immediately.

When the RST pin is taken to a logic low, the microcontroller exits the reset state within a delay that depends on the state of the flash memory at the time the reset was asserted. If a flash write or erase operation was in progress, the reset state is a 4ms maximum. If no flash write or erase operations were in progress, there is a delay of 90 external clock cycles. Operation resumes at address 0000h. If taking RST to a logic low causes the device to exit stop mode, an additional delay of 65,536 clock cycles is experienced before operation begins.

Reset Output

If a reset is caused by a power-fail reset, a watchdog timer reset, or an internal system reset, a logic high output-reset pulse is also generated at the bidirectional RST pin. This reset pulse is asserted as long as an internal reset is asserted. Although the microcontroller generates its own power-on delay for crystal warmup, legacy designs may employ an external RC circuit. Large values of “C” may load the pin enough that the RST output may not achieve a logic high, but the state of the external RST pin does not affect the internal reset condition.

Oscillator-Fail Detect and Reset

The DS89C430 incorporates an oscillator-fail-detect circuit that, when enabled, causes a reset if the crystal oscillator frequency falls below 20kHz and holds the chip in reset with the ring oscillator operating. Setting the OFDE (PCON.4) bit to logic 1 enables the circuit. The OFDE bit is only cleared from logic 1 to logic 0 by a power-fail reset or by software. A reset caused by an oscillator failure also sets the OFDF (PCON.5) to logic 1. This flag is cleared by software or power-on reset. This circuit does not force a reset when the oscillator is stopped by the software-enabled stop mode.

Power-Management Mode

The power-management mode offers a software-controllable power-saving scheme by providing a reduced instruction cycle speed, which allows the microcontroller to continue operating while using an internally divided version of the clock source to save power. Power-management mode is invoked by software setting the clock-divide control bits CD1 and CD0 (PMR.7–6) bits to 11b, which sets an operating rate of 1024 oscillator cycles for one machine cycle. On all forms of reset, the clock-divide control bits default to 10b, which selects one oscillator cycle per machine cycle.

Since the clock speed choice affects all functional logic, including timers, several hardware switchback features allow the clock speed to automatically return to the divide-by-1 mode from a reduced cycle rate. Setting the SWB (PMR.5) bit to 1 in software enables this switchback function.

When CD1 and CD0 are programmed to the divide-by-1024 mode and the SWB bit is also enabled, the system forces the clock-divide control bits to automatically reset to the divide-by-1 mode whenever the system detects an externally enabled (and allowed by nesting priorities) interrupt. The switchback occurs whenever one of the two following conditions occurs. The first switchback condition is initiated by the detection of a low on either $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$, or $\overline{\text{INT5}}$ or a high on INT2 or INT4 when the respective pin has been programmed and allowed (by nesting priorities) to issue an interrupt. The second switchback condition occurs when either serial port is enabled to receive data and is found to have an active-low transition on the respective receive-input pin. Serial port transmit activity also forces a switchback if the SWB is set. Note that the serial port activity, as related to the switchback, is independent of the serial port interrupt relationship. Any attempt to change the clock divider to the divide-by-1024 mode while the serial port is either transmitting or receiving has no effect, leaving the clock control in the divide-by-1 mode. Note also that the switchback interrupt relationship requires that the respective external interrupt source is allowed to actually generate an interrupt, as defined by the priority of the interrupt and the state of the nested interrupts, before the switchback can actually occur. An interrupt by the serial port is not required, nor is the setting of serial port enable. Disabling external interrupts and serial port receive/transmission mode disables the automatic switchback mode. Clearing the SWB bit also disables the switchback, and all interrupt and serial port controls of the clock divider are disabled. All other clock modes ignore the switchback relationship and are unaffected by interrupts and serial port activity.

The basic divide-by-12 mode for the timers (TxMH, TxM = 00b) as well as the divide by 32 and 64 for mode 2 on the serial ports has been maintained when running the processor with the oscillator divide ratio of 0.25, 0.5, and 1.

SELECTOR GUIDE

PART	TEMP RANGE	FLASH MEMORY SIZE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS89C430-MNL	-40°C to +85°C	16kB x 8	33	40 PDIP
DS89C430-MNL+	-40°C to +85°C	16kB x 8	33	40 PDIP
DS89C430-QNL	-40°C to +85°C	16kB x 8	33	44 PLCC
DS89C430-QNL+	-40°C to +85°C	16kB x 8	33	44 PLCC
DS89C430-ENL	-40°C to +85°C	16kB x 8	33	44 TQFP
DS89C430-ENL+	-40°C to +85°C	16kB x 8	33	44 TQFP
DS89C430-MNG	-40°C to +85°C	16kB x 8	25	40 PDIP
DS89C430-MNG+	-40°C to +85°C	16kB x 8	25	40 PDIP
DS89C430-QNG	-40°C to +85°C	16kB x 8	25	44 PLCC
DS89C430-QNG+	-40°C to +85°C	16kB x 8	25	44 PLCC
DS89C430-ENG	-40°C to +85°C	16kB x 8	25	44 TQFP
DS89C430-ENG+	-40°C to +85°C	16kB x 8	25	44 TQFP
DS89C440-xxx	Contact factory or replace with DS89C430 or DS89C450.			
DS89C450-MNL	-40°C to +85°C	64kB x 8	33	40 PDIP
DS89C450-MNL+	-40°C to +85°C	64kB x 8	33	40 PDIP
DS89C450-QNL	-40°C to +85°C	64kB x 8	33	44 PLCC
DS89C450-QNL+	-40°C to +85°C	64kB x 8	33	44 PLCC
DS89C450-ENL	-40°C to +85°C	64kB x 8	33	44 TQFP
DS89C450-ENL+	-40°C to +85°C	64kB x 8	33	44 TQFP
DS89C450-MNG	-40°C to +85°C	64kB x 8	25	40 PDIP
DS89C450-MNG+	-40°C to +85°C	64kB x 8	25	40 PDIP
DS89C450-QNG	-40°C to +85°C	64kB x 8	25	44 PLCC
DS89C450-QNG+	-40°C to +85°C	64kB x 8	25	44 PLCC
DS89C450-ENG	-40°C to +85°C	64kB x 8	25	44 TQFP
DS89C450-ENG+	-40°C to +85°C	64kB x 8	25	44 TQFP

+ Denotes a lead(Pb)-free/RoHS-compliant device.

REVISION HISTORY

DATE	DESCRIPTION
111003	New product release.
032204	*DC Electrical Characteristics* table: Corrected typo—Under Supply Current for Active and Idle Mode, changed Units from "µA" to "mA." Note 15: Changed number of external clock cyles per system clock and minimum external clock speeds. *Flash Memory Programming Characteristics* table: Removed Note 20 (room temperature only) from the Data Retention parameter.
060204	Changed Write/Erase Endurance parameter from 20,000 cycles to 10,000 cycles. Removed original *Table 5. Parallel Programming Instruction Set*, and replaced it with a paragraph introducing the subject and advising interested parties to contact the factory for more information. Clarified IAP programming sequence.
060805	Added lead-free devices to *Ordering Information* table.
091906	Removed references to DS89C440 and/or added "Contact factory or replace with DS89C430 or DS89C450."
040507	Added clarification to the *Security Features* section and *Table 3* that flash security levels 1, 2, and 3 should not be used when executing external code (page 22); corrected Figure 8 to show PSEN high through the second machine cycle (page 28).

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