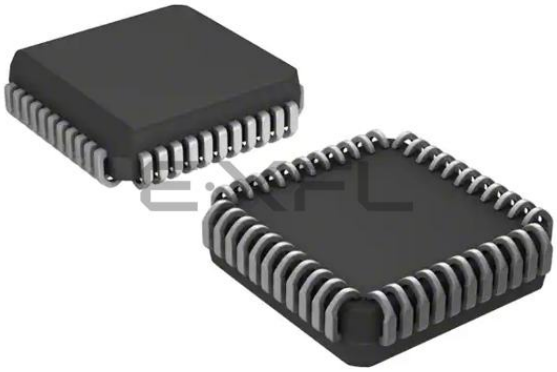

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds89c440-qnl

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……..-0.3V to +6.0V
Ambient Temperature Range (under bias)……-40°C to +85°C
Storage Temperature Range……-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (Notes 2, 3)	V_{CC}	4.5	5.0	5.5	V
Power-Fail Warning (Notes 2, 4)	V_{PFW}	4.2	4.375	4.6	V
Reset Trip Point (Min Operating Voltage) (Notes 2, 3, 4)	V_{RST}	3.95	4.125	4.35	V
Supply Current, Active Mode (Note 5)	I_{CC}		75	110	mA
Supply Current, Idle Mode at 33MHz (Note 6)	I_{IDLE}		40	50	mA
Supply Current, Stop Mode, Bandgap Disabled (Note 7)	I_{STOP}		1	100	μA
Supply Current, Stop Mode, Bandgap Enabled (Note 7)	I_{SPBG}		150	300	μA
Input Low Level (Note 2)	V_{IL}	-0.3		+0.8	V
Input High Level (Note 2)	V_{IH}	2.0		V_{CC} + 0.3	V
Input High Level XTAL and RST (Note 2)	V_{IH2}	3.5		V_{CC} + 0.3	V
Output Low Voltage, Port 1 and 3 at I_{OL} = 1.6mA (Note 2)	V_{OL1}		0.15	0.45	V
Output Low Voltage, Port 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA (Note 2)	V_{OL2}		0.15	0.45	V
Output High Voltage, Port 1, 2, and 3, at I_{OH} = -50μA (Notes 2, 8)	V_{OH1}	2.4			V
Output High Voltage, Port 1, 2, and 3 at I_{OH} = -1.5mA (Notes 2, 9)	V_{OH2}	2.4			V
Output High Voltage, Port 0, 1, 2, ALE, $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$ in Bus Mode at I_{OH} = -8mA (Notes 2, 10)	V_{OH3}	2.4			V
Output High Voltage, RST at I_{OL} = -0.4mA (Note 2, 11)	V_{OH4}	2.4			V
Input Low Current, Port 1, 2, and 3 at 0.4V	I_{IL}	-50			μA
Transition Current from 1 to 0, Port 1, 2, and 3 at 2V (Note 12)	I_{TL}	-650			μA
Input Leakage Current, Port 0 in I/O Mode and $\overline{EA}$ (Note 13)	I_L	-10		+10	μA
Input Current, Port 0 in Bus Mode (Note 14)	I_L	-300		+300	μA
RST Pulldown Resistance (Note 13)	R_{RST}	50	120	200	kΩ

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

Note 2: All voltages are referenced to ground.

Note 3: The user should note that this part is tested and guaranteed to operate down to 4.5V (10%) and that V_{RST} (min) is specified below that point. This indicates that there is a range of voltages [(V_{MIN} to V_{RST} (min)] where the processor's operation is not guaranteed, but the reset trip point has not been reached. This should not be an issue in most applications, but should be considered when proper operation must be maintained at all times. For these applications, it may be desirable to use a more accurate external reset.

Note 4: While the specifications for V_{PFW} and V_{RST} overlap, the design of the hardware makes it so this is not possible. Within the ranges given, there is guaranteed separation between these two voltages.

Note 5: Active current is measured with a 33MHz clock source driving XTAL1, V_{CC} = RST = 5.5V. All other pins are disconnected.

Note 6: Idle mode current is measured with a 33MHz clock source driving XTAL1, V_{CC} = 5.5V, RST at ground. All other pins are disconnected.

Note 7: Stop mode is measured with XTAL and RST grounded, V_{CC} = 5.5V. All other pins are disconnected.

Note 8: RST = 5.5V. This condition mimics the operation of pins in I/O mode.

Note 9: During a 0-to-1 transition, a one shot drives the ports hard for two clock cycles. This measurement reflects a port pin in transition mode.

Note 10: When addressing external memory.

Note 11: Guaranteed by design.

Note 12: Ports 1, 2, and 3 source transition current when pulled down externally. The current reaches its maximum at approximately 2V.

Note 13: RST = 5.5V. Port 0 is floating during reset and when in the logic-high state during I/O mode.

Note 14: This port is a weak address holding latch in bus mode. Peak current occurs near the input transition point of the holding latch at approximately 2V.

Figure 2. Page Mode 1 Timing

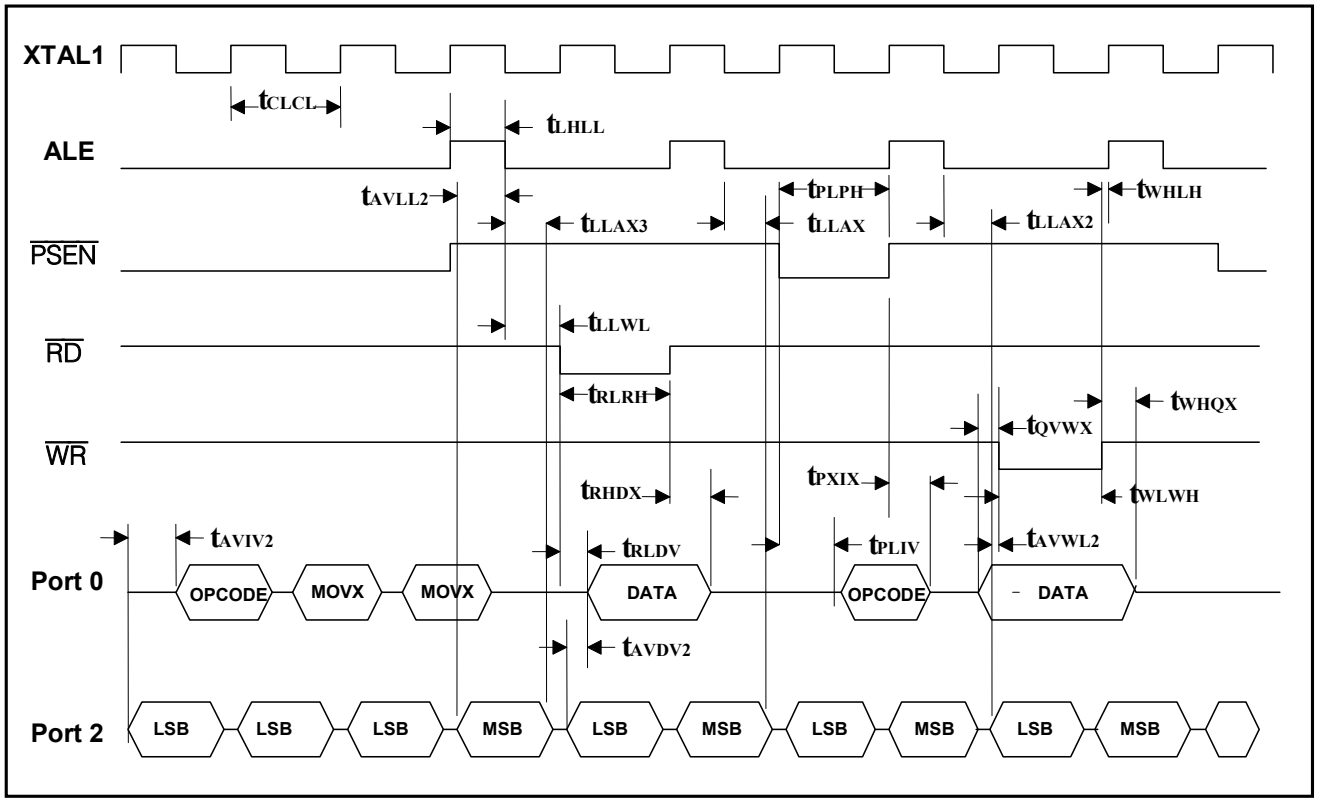


Figure 3. Page Mode 2 Timing

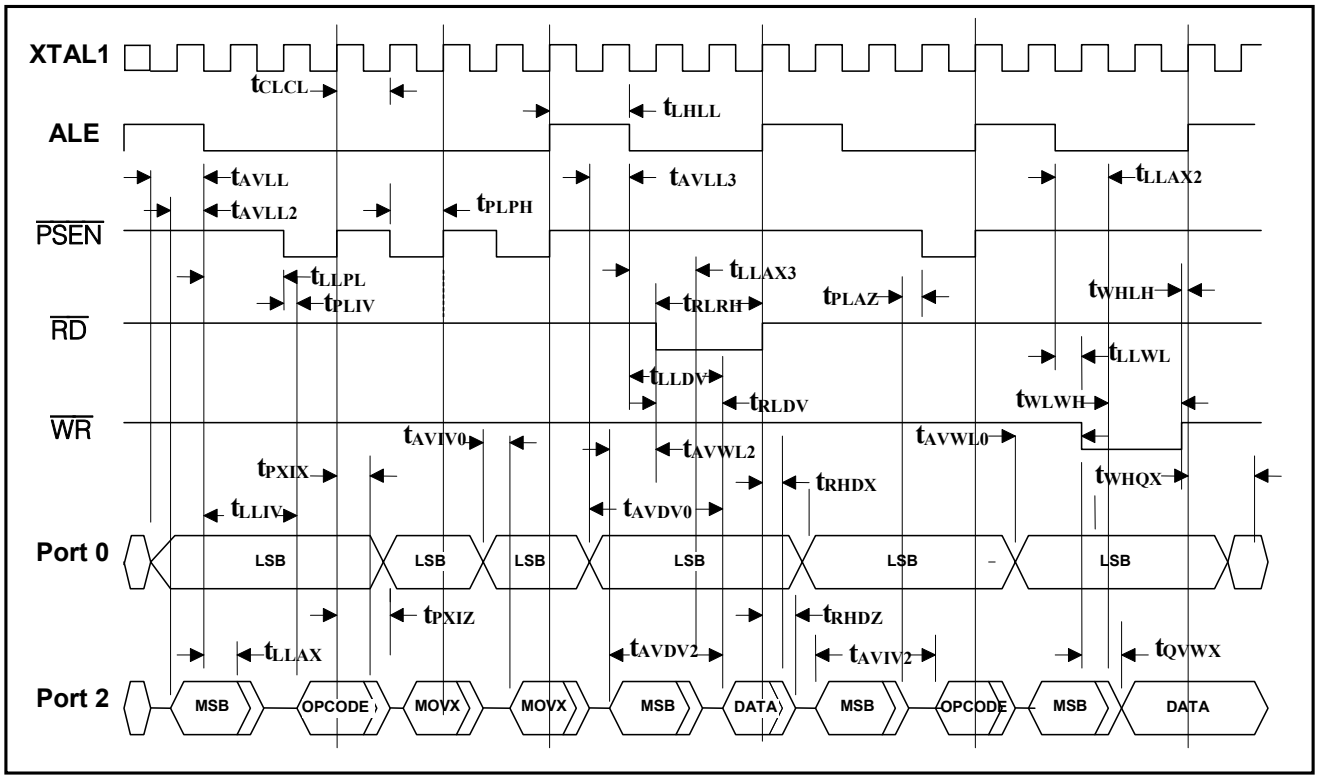
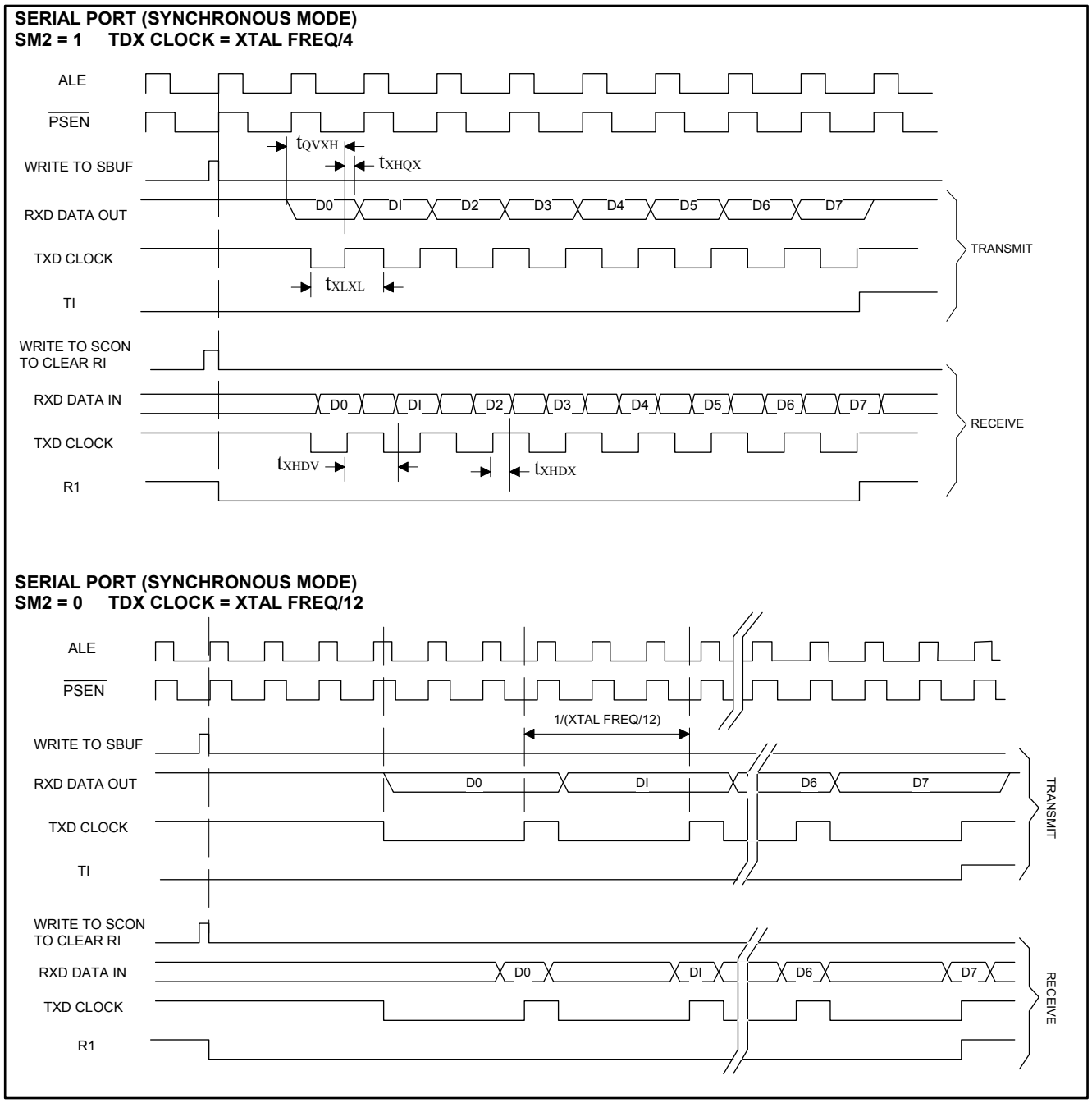


Figure 4. Serial Port Timing



POWER-CYCLE TIMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_O = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Startup Time (Note 18)	t_{CSU}		8		ms
Power-On Reset Delay (Note 19)	t_{POR}		65,536		t_{CLCL}

Note 18: Startup time for a crystal varies with load capacitance and manufacturer. The time shown is for an 11.0592MHz crystal manufactured by Fox Electronics.

Note 19: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

FLASH MEMORY PROGRAMMING CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data Retention	t_{DR}	100			years
Write/Erase Endurance	t_{ENDURE}	10,000			cycles
Program/Time	t_{PROG}			40	µs
Erase Time	t_{ERASE}	4			ms

PIN DESCRIPTION

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
40	12, 44	6, 38	V_{CC}	**+5V**
20	1, 22, 23, 34	16, 17, 28, 39	GND	**Logic Ground**
9	10	4	RST	**External Reset.** The RST input pin is bidirectional and contains a Schmitt Trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, as the device provides this function internally.
19	21	15	XTAL1	**Crystal Oscillators.** These pins provide support for fundamental-mode parallel-resonant AT-cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
18	20	14	XTAL2	
29	32	26	$\overline{PSEN}$	**Program Store Enable.** This signal is commonly connected to optional external program memory as a chip enable. $\overline{PSEN}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In one-cycle page mode 1, $\overline{PSEN}$ remains low for consecutive page hits.
30	33	27	ALE/$\overline{PROG}$	**Address Latch Enable.** This signal functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373-family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{PROG}$) is used to execute the parallel program function.
39	43	37	P0.0 (AD0)	**Port 0 (AD0–AD7), I/O.** Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of port 0 is tri-state. Pullup resistors are required only when using port 0 as an I/O port.
38	42	36	P0.1 (AD1)	
37	41	35	P0.2 (AD2)	
36	40	34	P0.3 (AD3)	
35	39	33	P0.4 (AD4)	
34	38	32	P0.5 (AD5)	
33	37	31	P0.6 (AD6)	
32	36	30	P0.7 (AD7)	

Table 1. SFR Register Map (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TH1	8Dh								
CKCON	8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
P1	90h	P1.7/$\overline{INT5}$	P1.6/INT4	P1.5/$\overline{INT3}$	P1.4/INT2	P1.3/TXD1	P1.2/RXD1	P1.1/T2EX	P1.0/T2
EXIF	91h	IE5	IE4	IE3	IE2	CKRY	RGMD	RGSL	BGS
CKMOD	96h			T2MH	T1MH	T0MH	—	—	—
SCON0	98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
SBUF0	99h								
ACON	9Dh	PAGEE	PAGES1	PAGES0	—	—	—	—	—
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
SADDR0	A9h								
SADDR1	AAh								
P3	B0h	P3.7/$\overline{RD}$	P3.6/$\overline{WR}$	P3.5/T1	P3.4/T0	P3.3/$\overline{INT1}$	P3.2/$\overline{INT0}$	P3.1/TXD0	P3.0/RXD0
IP1	B1h	—	MPS1	MPT2	MPS0	MPT1	MPX1	MPT0	MPX0
IP0	B8h	—	LPS1	LPT2	LPS0	LPT1	LPX1	LPT0	LPX0
SADEN0	B9h								
SADEN1	BAh								
SCON1	C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
SBUF1	C1h								
ROMSIZE	C2h					PRAME	RMS2	RMS1	RMS0
PMR	C4h	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEON	DME1	DME0
STATUS	C5h	PIS2	PIS1	PIS0	—	SPTA1	SPRA1	SPTA0	SPRA0
TA	C7h								
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9h							T2OE	DCEN
RCAP2L	CAh								
RCAP2H	CBh								
TL2	CCh								
TH2	CDh								
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P
FCNTL	D5h	$\overline{FBUSY}$	FERR			FC3	FC2	FC1	FC0
FDATA	D6h								
WDCON	D8h	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
ACC	E0h								
EIE	E8h	—	—	—	EWDI	EX5	EX4	EX3	EX2
B	F0h								
EIP1	F1h	—	—	—	MPWDI	MPX5	MPX4	MPX3	MPX2
EIP0	F8h	—	—	—	LPWDI	LPX5	LPX4	LPX3	LPX2

Note: Shaded bits are timed-access protected.

Table 2. SFR Reset Value

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	1	1	1	1	1	1	1	1
SP	81h	0	0	0	0	0	1	1	1
DPL	82h	0	0	0	0	0	0	0	0
DPH	83h	0	0	0	0	0	0	0	0
DPL1	84h	0	0	0	0	0	0	0	0
DPH1	85h	0	0	0	0	0	0	0	0
DPS	86h	0	0	0	0	0	1	0	0
PCON	87h	0	0	Special	Special	0	0	0	0
TCON	88h	0	0	0	0	0	0	0	0
TMOD	89h	0	0	0	0	0	0	0	0
TL0	8Ah	0	0	0	0	0	0	0	0
TL1	8Bh	0	0	0	0	0	0	0	0
TH0	8Ch	0	0	0	0	0	0	0	0
TH1	8Dh	0	0	0	0	0	0	0	0
CKCON	8Eh	0	0	0	0	0	0	0	1
P1	90h	1	1	1	1	1	1	1	1
EXIF	91h	0	0	0	0	Special	Special	Special	0
CKMOD	96h	1	1	0	0	0	1	1	1
SCON0	98h	0	0	0	0	0	0	0	0
SBUF0	99h	0	0	0	0	0	0	0	0
ACON	9Dh	0	0	0	1	1	1	1	1
P2	A0h	1	1	1	1	1	1	1	1
IE	A8h	0	0	0	0	0	0	0	0
SADDR0	A9h	0	0	0	0	0	0	0	0
SADDR1	AAh	0	0	0	0	0	0	0	0
P3	B0h	1	1	1	1	1	1	1	1
IP1	B1h	1	0	0	0	0	0	0	0
IP0	B8h	1	0	0	0	0	0	0	0
SADEN0	B9h	0	0	0	0	0	0	0	0
SADEN1	BAh	0	0	0	0	0	0	0	0
SCON1	C0h	0	0	0	0	0	0	0	0
SBUF1	C1h	0	0	0	0	0	0	0	0
ROMSIZE	C2h	1	1	1	1	0	1	0	1
PMR	C4h	1	0	0	0	0	0	0	0
STATUS	C5h	0	0	0	1	0	0	0	0
TA	C7h	1	1	1	1	1	1	1	1
T2CON	C8h	0	0	0	0	0	0	0	0
T2MOD	C9h	1	1	1	1	1	1	0	0
RCAP2L	CAh	0	0	0	0	0	0	0	0
RCAP2H	CBh	0	0	0	0	0	0	0	0

Table 2. SFR Reset Value (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TL2	CCh	0	0	0	0	0	0	0	0
TH2	CDh	0	0	0	0	0	0	0	0
PSW	D0h	0	0	0	0	0	0	0	0
FCNTL	D5h	1	0	1	1	0	0	0	0
FDATA	D6h	0	0	0	0	0	0	0	0
WDCON	D8h	0	Special	0	Special	0	Special	Special	0
ACC	E0h	0	0	0	0	0	0	0	0
EIE	E8h	1	1	1	0	0	0	0	0
B	F0h	0	0	0	0	0	0	0	0
EIP1	F1h	1	1	1	0	0	0	0	0
EIP0	F8h	1	1	1	0	0	0	0	0

Note: Consult the *Ultra-High-Speed Flash Microcontroller User's Guide* for more information about the bits marked "Special."

Memory Organization

There are three distinct memory areas in the DS89C430: scratchpad registers, program memory, and data memory. The registers are located on-chip but the program and data memory spaces can be on-chip, off-chip, or both. The DS89C430/DS89C450 have 16kB/64kB of on-chip program memory, respectively, implemented in flash memory and also have 1kB of on-chip data memory space that can be configured as program space using the PRAME bit in the ROMSIZE feature. The DS89C430 uses a memory-addressing scheme that separates program memory from data memory. The program and data segments can be overlapped since they are accessed in different manners. If the maximum address of on-chip program or data memory is exceeded, the DS89C430 performs an external memory access using the expanded memory bus. The $\overline{PSEN}$ signal goes active low to serve as a chip enable or output enable when performing a code fetch from external program memory. MOVX instructions activate the $\overline{RD}$ or $\overline{WR}$ signal for external MOVX data memory access. The program memory ROMSIZE feature allows software to dynamically configure the maximum address of on-chip program memory. This allows the DS89C430 to act as a bootloader for an external memory. It also enables the use of the overlapping external program spaces. The lower 128 bytes of on-chip flash memory—if ROMSIZE is greater than 0—are used to store reset and interrupt vectors. 256 bytes of on-chip RAM serve as a register area and program stack, which are separated from the data memory.

Register Space

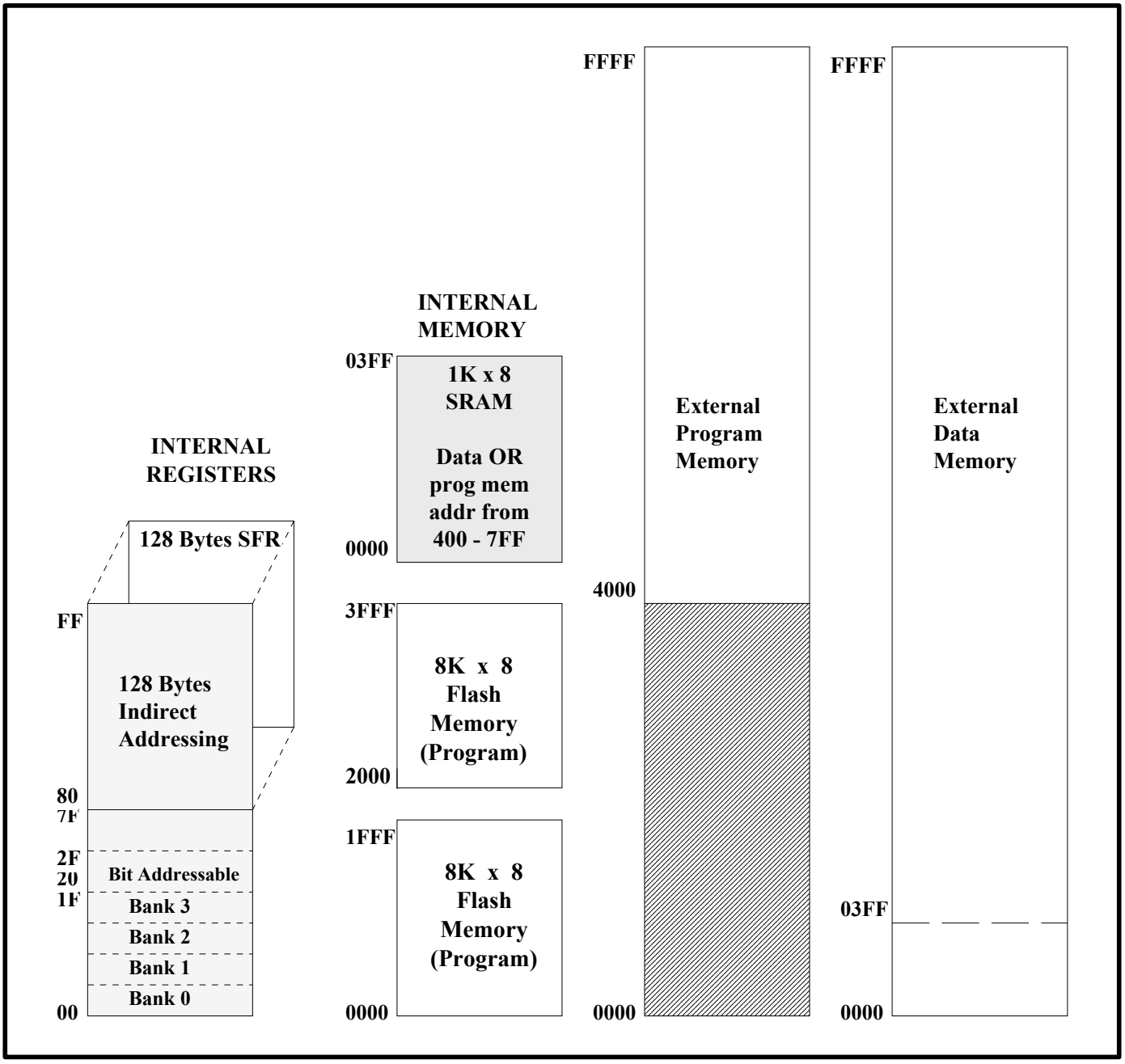
Registers are located in the 256 bytes of on-chip RAM labeled "internal registers" (Figure 6), which can be divided into two sub areas of 128 bytes each. Separate classes of instructions are used to access the registers and the program/data memory. The upper 128 bytes are overlapped with the 128 bytes of SFRs in the memory map. Indirect addressing is used to access the upper 128 bytes of scratchpad RAM, while the SFR area is accessed using direct addressing. The lower 128 bytes can be accessed using direct or indirect addressing.

There are four banks of eight working registers in the lower 128 bytes of scratchpad RAM. The working registers are general-purpose RAM locations that can be addressed within the selected bank by any instructions that use R0–R7. The register bank selection is controlled through the program status register in the SFR area. The contents of the working registers can be used for indirect addressing of the upper 128 bytes of scratchpad RAM.

Individually addressable bits in the RAM and SFR areas support Boolean operations. In the scratchpad RAM area, registers 20h–2Fh are bit addressable by software using Boolean operation instructions.

Another use of the scratchpad RAM area is for the stack. The stack pointer, contained in the SFRs, is used to select storage locations for program variables and for return addresses of control operations.

Figure 6. Memory Map (as shown for the DS89C430)



Memory Configuration

As illustrated in Figure 6, the DS89C430 incorporates two 8kB flash areas for on-chip program memory and 1kB of SRAM for on-chip data memory or a particular range (400–7FF) of “alternate” program memory space. The DS89C450 incorporates two 32kB flash memories. The DS89C430 uses an address scheme that separates program memory from data memory such that the 16-bit address bus can address each memory area up to maximum of 64kB.

Program Memory Access

On-chip program memory begins at address 0000h and is contiguous through 3FFFh (16kB) on the DS89C430 and through FFFFh (64kB) on the DS89C450. Exceeding the maximum address of on-chip program memory causes the device to access off-chip memory. The maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS89C430 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory is used. The maximum memory size is dynamically variable. Thus a portion of memory can be removed from the memory map to access off-chip memory and then be restored to access on-chip memory. In fact, all the on-chip memory can be removed from the memory map allowing the full 64kB memory space to be addressed from off-chip memory. Program memory addresses that are larger than the selected maximum are automatically fetched from outside the part through ports 0 and 2. Figure 6 shows a depiction of the memory map.

The ROMSIZE register is used to select the maximum on-chip decoded address for program memory. Bits RMS2, RMS1, and RMS0 have the following effect:

RMS2	RMS1	RMS0	Maximum On-Chip Program Memory Address (Size/Address)
0	0	0	0kB
0	0	1	1kB/03FFh
0	1	0	2kB/07FFh
0	1	1	4kB/0FFFh
1	0	0	8kB/1FFFh
1	0	1	16kB/3FFFh (DS89C430 default)
1	1	0	32kB/7FFFh
1	1	1	64kB/FFFFh (DS89C450 default)

The reset default condition for all devices is to their maximum on-chip program memory size. When accessing external program memory, that amount of external memory would be inaccessible. To select a smaller effective program memory size, software must alter bits RMS2–RMS0. Altering these bits requires a timed-access procedure, as explained later.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that a DS89C430 is executing instructions from internal program memory near the 12kB boundary (~3000h) and that the ROMSIZE register is currently configured for a 16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device immediately jumps to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that is internal (or external) both before and after the operation. In the above example, the instruction that modifies the ROMSIZE register should be located below the 4kB (1000h) boundary or above the 16kB (3FFFh) boundary so that it is unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

For nonpage mode operations, off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip program memory access also occurs if the $\overline{EA}$ pin is a logic 0. $\overline{EA}$ overrides all ROMSIZE bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when ports 0 and 2 fetch from external program memory.

The $\overline{RD}$ and $\overline{WR}$ signals are used to control the external data memory device. Data memory is accessed by MOVX instructions. The MOVX@Ri instruction uses the value in the designated working register to provide the LSB of the address, while port 2 supplies the address MSB. The MOVX@DPTR instruction uses one of the two data pointers to move data over the entire 64kB external data memory space. Software selects the data pointer used by writing to the SEL bit (DPS.0).

The DS89C430 also provides a user option for high-speed external memory access by reconfiguring the external memory interface into page mode operation.

Note: When using the original 8051 expanded bus structure, the throughput is reduced by 75% compared with that of internal operations. This is because of the CPU being stalled for three out of four clocks, waiting for the data

The signature bytes can be read in ROM loader mode or in parallel programming mode. Reading data from addresses 30h, 31h, and 60h provides signature information on manufacturer, part, and extension as follows:

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer ID
31h	43h	DS89C430 Device ID
31h	44h	DS89C440 Device ID (Contact factory or replace with DS89C430 or DS89C450.)
31h	45h	DS89C450 Device ID
60h	01h	Device Extension

Note: *The read/write accessibility of the flash memory during in-application programming is not affected by the state of the lock bits. However, the lock bits do affect the read/write accessibility in ROM loader and parallel programming modes.*

In-Application Programming by User Software

The DS89C430 supports in-application programming of on-chip flash memory by user software. In-application programming is initiated by writing a flash command into the flash control (FCNTL:D5h) register to enable the flash memory for erase/program/verify operations. Address and data are input into the MMU through the flash data (FDATA:D6h) register. The flash command also enables read/write accesses to the FDATA. The MMU's sequencer provides the operation sequences and control functions to the flash memory. The MMU is designed to operate independently from the processor, except for read/write access to the SFRs.

Only the upper bank of the on-chip program memory can be in-application programmed by the user software. The lower bank of the on-chip program memory contains system hardware-dependent codes that are crucial to system operation and should not be altered during in-application programming.

All flash operations are self-timed. The user software can monitor the progress of an erase or programming operation through the flash busy (FBUSY;FCNTL.7) bit with a reset value at logic 1. A selected operation automatically starts when required data is written to the FDATA SFR. The MMU clears the FBUSY bit to indicate the start of a write/erase operation. The FBUSY bit may not change state for up to 1μs after the operation is requested. During this time, the application should poll the status of the FBUSY bit waiting for it to change state. This bit is held low until either the end of the operation or until an error indicator is returned. A flash operating failure terminates the current operation and sets the flash error flag (FERR;FCNTL.6) to logic 1. Both the busy and error flags are read-only bits.

Read/write access during in-application programming is not affected by the state of the lock bits.

A sample programming sequence for a "write upper program memory bank" is shown below. The command must be reentered each time an operation is requested, i.e., it is not permissible to issue the "write upper program memory bank" command once and then repeatedly load address and data values to program a block of memory.

1. Make sure the $\overline{\text{FBUSY}}$ bit is 1 to indicate flash MMU is idle.
2. Write 0Bh to the FCNTL register using the timed access sequence.
3. Write address_MSB to the FDATA register.
4. Write address_LSB to the FDATA register.
5. Write data_value to the FDATA register.
6. Make sure the $\overline{\text{FBUSY}}$ bit is 0 to indicate programming has started.
7. Wait for $\overline{\text{FBUSY}}$ bit to return to 1 to indicate end of programming operation.
8. Make sure FERR is 0 to indicate no programming error.

The flash command (FC3–FC0;FCNTL.3:0) bits provide flash commands as listed in Table 4.

Table 4. In-Application Programming Commands

FC3:FC0	COMMAND	OPERATION
0000	Read Mode	Default state. All flash blocks are in read mode. **Note:** The upper bank of flash memory is inaccessible for execution unless the FC3:0 bits are in the read mode (0000b) state.
0001	Verify Option Control Register	Read data from the option control register. Data is available in the FDATA at the end of the following machine cycle. FDATA.3 is the logic value of the watchdog POR default setting.
0010	Verify Security Block	Read a byte of data from the security block. After the address byte is written to the FDATA, data is available in the FDATA at the end of the following machine cycle. (Lock bits are addressed at 40h and FDATA.5:3 are the logic value of LB1, LB2 and LB3, respectively.)
0011	Verify Upper Program Memory Bank	Read a byte of data from upper flash memory bank (address range from 2000h to 3FFFh). The first and second byte writes to the FDATA are the upper and lower byte of the address. Data is available in the FDATA at the end of the following machine cycle after the second address byte is written.
0100	Reserved for Future Use	This command should not be modified by user programs.
1000	Reserved for Future Use	This command should not be modified by user programs.
1001	Write Option Control Register	Write to the option control register as data is written to FDATA. Bit 3 of the data byte represents the watchdog POR default setting.
1010	Write Security Block	Write a byte of data to the security block at a selected locations addressed by the first byte write to the FDATA. The second write to the FDATA is the data byte. (Lock bits are addressed at 40h and the FDATA 5:3 represents lock bits LB3, LB2, and LB1, respectively.)
1011	Write Upper Program Memory Bank	Write a byte of code to the upper flash memory bank (address range from 2000h to 3FFFh). The first and second byte writes to the FDATA are the upper byte and the lower byte of the address. The third write to the FDATA is the data byte.
1100	Erase Option Control Register	Erase the option control register. The contents of this register are returned to FFh. This operation disables the watchdog reset function on power-up.
1101	Erase Security Block	Erase the security flash block that contains the 64-byte encryption array and the lock bits. The content of every memory location is turned into FFh.
1110	Erase Upper Program Memory Bank	Erase the upper bank of flash memory bank. The contents of every memory location are returned to FFh.
1111	System Reset	This command is used to cause a system reset.

The flash command bits are cleared to 0 on all forms of reset, and it is important for the user software to clear these bits to 0 to return the flash memory to read mode from erase/program operation. This setting is a “no operation” condition for the MMU, which allows the processor to return to its normal execution. Note that the busy and error flags have no function in normal flash-read mode.

The FCNTL SFR can only be written using timed access. This procedure provides protection against inadvertent erase/program operation on the flash memory. Any command written to the FCNTL during a flash operation is ignored (FBUSY = 0). To ensure data integrity, an erase command sequence should be reinitiated if an erase or program operation is interrupted by a reset.

External Data Memory Interface in Nonpage Mode Operation

Just like the program memory cycle, the external data memory cycle is four times slower than the internal data memory cycle in nonpage mode. A basic internal memory cycle contains one system clock and a basic external memory cycle contains four system clocks for nonpage mode operation.

The DS89C430 allows software to adjust the speed of external data memory access by stretching the memory bus cycle. CKCON (8Eh) provides an application-selectable stretch value for this purpose. Software can change the stretch value dynamically by changing the setting of CKCON.2–CKCON.0. Table 5 shows the data memory cycle stretch values and their effect on the external MOVX memory bus cycle and the control signal pulse width in terms of the number of oscillator clocks. A stretch machine cycle always contains four system clocks.

Table 5. Data Memory Cycle Stretch Values

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

As Table 5 shows, the stretch feature supports eight stretched external data memory access cycles, which can be categorized into three timing groups. When the stretch value is cleared to 000b, there is no stretch on external data memory access and a MOVX instruction is completed in two basic memory cycles. When the stretch value is set to 1, 2, or 3, the external data memory access is extended by 1, 2, or 3 stretch machine cycles, respectively. Note that the first stretch value does not result in adding four system clocks to the $\overline{RD}/\overline{WR}$ control signals. This is because the first stretch uses one system clock to create additional setup time and one system clock to create additional address hold time. When using very slow RAM and peripherals, a larger stretch value (4–7) can be selected. In this stretch category, one stretch machine cycle (4 system clocks) is used to stretch the ALE pulse width, one stretch machine cycle is used to create additional setup, one stretch machine cycle is used to create additional hold time, and one stretch machine cycle is added to the $\overline{RD}$ or $\overline{WR}$ strobes.

The following diagrams illustrate the timing relationship for external data memory access in full speed (stretch value = 0), in the default stretch setting (stretch value = 1), and slow data memory accessing (stretch value = 4), when the system clock is in divide-by-1 mode (CD1:CD0 = 10b).

Table 7. Page Mode 1, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 00)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.25	0.5	1	1024
001	1	0.75	1.5	3	3072
010	2	1.75	3.5	7	7168
011	3	2.75	5.5	11	11,264
100	7	3.75	7.5	15	15,360
101	8	4.75	9.5	19	19,456
110	9	5.75	11.5	23	23,552
111	10	6.75	13.5	27	27,648

Table 8. Page Mode 1, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 01)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.25	0.5	1	1024
001	1	0.75	1.5	3	3072
010	2	1.75	3.5	7	7168
011	3	2.75	5.5	11	11,264
100	7	3.75	7.5	15	15,360
101	8	4.75	9.5	19	19,456
110	9	5.75	11.5	23	23,552
111	10	6.75	13.5	27	27,648

Table 9. Page Mode 1, Data Memory Cycle Stretch Values (PAGES1:PAGES0 = 10)

MD2:MD0	STRETCH CYCLES	$\overline{RD}/\overline{WR}$ PULSE WIDTH (IN NUMBER OF OSCILLATOR CLOCKS)			
		4X/$\overline{2X}$, CD1, CD0 = 100	4X/$\overline{2X}$, CD1, CD0 = 000	4X/$\overline{2X}$, CD1, CD0 = X10	4X/$\overline{2X}$, CD1, CD0 = X11
000	0	0.5	1	2	2048
001	1	1	2	4	4096
010	2	2	4	8	8192
011	3	3	6	12	12,288
100	7	4	8	16	16,384
101	8	5	10	20	20,480
110	9	6	12	24	24,576
111	10	7	14	28	28,672

Timer/Counters

The DS89C430 incorporates three 16-bit timers. All three timers can be used as either counters of external events, where 1-to-0 transitions on a port pin are monitored and counted, or timers that count oscillator cycles. Table 12 summarizes the timer functions.

Timers 0 and 1 both have three modes of operations. They can each be used as a 13-bit timer/counter, a 16-bit timer/counter, or an 8-bit timer/counter with autoreload. Timer 0 has a fourth operating mode as two 8-bit timer/counters without autoreload. Each timer can also be used as a counter of external pulses on the corresponding T0/T1 pin for 1-to-0 transitions. The timer mode (TMOD) register controls the mode of operation. Each timer consists of a 16-bit register in 2 bytes, which can be found in the SFR map as TL0, TH0, TL1, and TH1. The timer control (TCON) register enables timers 0 and 1.

Table 12. Timer Functions

FUNCTIONS	TIMER 0	TIMER 1	TIMER 2
Timer/Counter	13/16/8*/2x8 bit	13/16/8* bit	16 bit
Timer with Capture	No	No	Yes
External Control Pulse Counter	Yes	Yes	No
Up/Down Autoreload Timer/Counter	No	No	Yes
Baud Rate Generator	No	Yes	Yes
Timer Output Clock Generator	No	No	Yes

**8-bit timer/counter includes autoreload feature. 2x8-bit mode does not.*

Each timer has a selectable time base (Table 14). Following a reset, the timers default to divide by 12 to maintain drop-in compatibility with the 8051. If timer 2 is used as a baud rate generator or clock output, its time base is fixed at divide by 2, regardless of the setting of its timer mode bits.

Timer 2 is a true 16-bit timer/counter that, with a 16-bit capture (RCAP2L and RCAP2H) register, is able to provide some unique functions like up/down autoreload timer/counter and timer output-clock generation. Timer 2 (registers TL2 and TH2) is enabled by the T2CON register. Its mode of operation is selected by the T2MOD register.

For operation details, refer to *Section 11: Programmable Timers* in the *Ultra-High-Speed Flash Microcontroller User's Guide.*

Timed Access

The timed-access function prevents an errant CPU from making accidental changes to certain SFR bits that are considered vital to proper system operation. This is achieved by using software control when accessing the following SFR control bits:

SFR	BIT	FUNCTION
WDCON.0	RWT	Reset Watchdog Timer
WDCON.1	EWT	Watchdog Reset Enable
WDCON.3	WDIF	Watchdog Interrupt Flag
WDCON.6	POR	Power-On Reset Flag
EXIF.0	BGS	Bandgap Select
ACON.5	PAGES0	Page Mode Select Bit 0
ACON.6	PAGES1	Page Mode Select Bit 1
ACON.7	PAGEE	Page Mode Enable
ROMSIZE.0	RMS0	Program Memory Size Select Bit 0
ROMSIZE.1	RMS1	Program Memory Size Select Bit 1
ROMSIZE.2	RMS2	Program Memory Size Select Bit 2
ROMSIZE.3	PRAME	Program RAM Enable
FCNTL.0	FC0	Flash Command Bit 0
FCNTL.1	FC1	Flash Command Bit 1
FCNTL.2	FC2	Flash Command Bit 2
FCNTL.3	FC3	Flash Command Bit 3

Before these bits can be altered, the processor must execute the timed-access sequence. This sequence consists of writing an AAh to the timed access (TA, C7h) register, followed by writing a 55h to the same register within three machine cycles. This timed sequence of steps allows any of the timed access-protected SFR bits to be altered

during the three machine cycles following the writing of the 55h. Writing to a timed-access-protected bit outside of these three machine cycles has no effect on the bit.

The timed-access process is address, data, and time dependent. A processor running out of control and not executing system software statistically is not able to perform this timed sequence of steps, and as such, does not accidentally alter the protected bits. It should be noted that this method should be used in the main body of the system software and *never* used in an interrupt routine in conjunction with the watchdog reset. Interrupt routines using the timed-access watchdog-reset bit (RWT) can recover a lost system and allow the resetting of the watchdog, but the system returns to a lost condition once the RETI is executed, unless the stack is modified. Also, it is advisable that interrupts be disabled (EA = 0) when executing the timed-access sequence, since an interrupt during the sequence adds time, making the timed-access attempt fail.

Power Management and Clock-Divide Control

Power-management features are available that monitor the power-supply voltage levels and support low-power operation with three power-saving modes. Such features include a bandgap voltage monitor, watchdog timer, selectable internal ring oscillator, and programmable system clock speed. The SFRs that provide control and application software access are the watchdog control (WDCON, D8h), extended interrupt enable (EIE, E8h), extended interrupt flag (EXIF, 91h) and power control (PCON, 87h) registers.

System Clock-Divide Control

The programmable clock-divide control bits (CD1 and CD0) provide the processor with the ability to adapt to different crystals and to slow the system clocks, providing lower power operation when required. An on-chip crystal multiplier allows the DS89C430 to operate at two or four times the crystal frequency by setting the 4X/$\overline{2X}$ bit, and is enabled by setting the CTM bit to a logic 1. An additional circuit provides a clock source at divide by 1024. When used with a 7.372MHz crystal, for example, the processor executes the machine cycle in times ranging from 33.9ns (mulitply-by-4 mode) to 138.9µs (divide-by-1024 mode) and maintains a highly accurate serial port baud rate, while allowing the use of more cost-effective lower frequency crystals. Although the clock-divide control bits can be written at any time, certain hardware features enhance the use of these clock controls to guarantee proper serial port operation and to allow for a high-speed response to an external interrupt. The 01b setting of CD1 and CD0 is reserved. It has the same effect as the setting of 10b, which forces the system clock into a divide-by-1 mode. The DS89C430 defaults to divide-by-1 clock mode on all forms of reset.

When in divide-by-1024 mode, in order to allow a quick response to incoming data on a serial port, the system uses the switchback mode to automatically revert to divide-by-1 mode whenever a start bit is detected. This automatic switchback is only enabled in divide-by-1024 mode when the switchback bit (PMR.5:SWB) is set. All other clock modes are unaffected by interrupts and serial port activity.

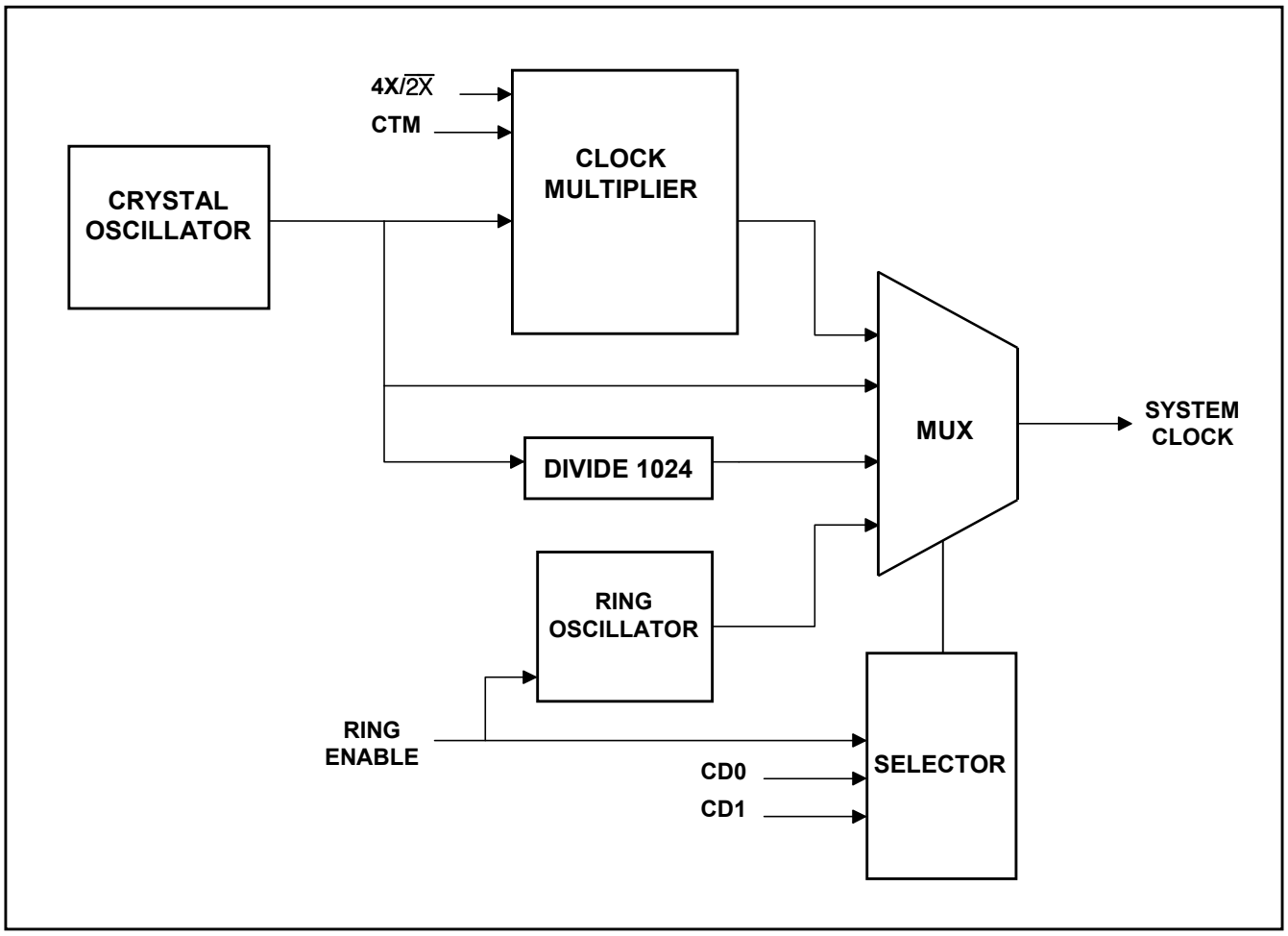
The oscillator multiply ratios of 4, 2, and 1 are also used to provide standard baud-rate generation for the serial ports through a forced divide-by-12 input clock (TxMH,TxM = 00b, x = 1, 2, or 3) to the timers.

Use of the multiply-by-4 or multiply-by-2 options through the clock-divide control bits requires that the crystal multiplier be enabled and the specific system-clock-multiply value be established by the 4X/$\overline{2X}$ bit in the PMR register. The multiplier is enabled through the CTM (PMR.4) bit but cannot be automatically selected until a startup delay has been established through the CKRY bit in the status register. The 4X/$\overline{2X}$ bit can only be altered when the CTM bit is cleared to a logic 0. This prevents the system from changing the multiplier until the system has moved back to the divide-by-1 mode and the multiplier has been disabled by the CTM bit. The CTM bit can only be altered when the CD1 and CD0 bits are set to divide-by-1 mode and the RGMD bit is cleared to 0. Setting the CTM to a logic 1 from a previous logic 0 automatically clears the CKRY bit in the status register and starts the multiplier startup timeout in the multiplier startup counter. During the multiplier startup period, the CKRY bit remains cleared and the CD1 and CD0 clock controls cannot be set to 00b. The CTM bit is cleared to a logic 0 on all resets.

Note that the rated maximum speed of operation applies to the speed of the microcontroller core, not the external clock source. When using the clock multiplier feature, the external clock source frequency, multiplied by the clock multiplier (2X or 4X) can never be faster than the maximum rated speed of the device. Thus, if a designer wished to use the 4X clock multiplier on a device rated at 33MHz, the maximum external clock speed would be 8.25MHz.

Figure 14 gives a simplified description of the generation of the system clocks. Specifics of hardware restrictions associated with the use of the 4X/$\overline{2X}$ CTM, CKRY, CD1, and CD0 bits are outlined in the *SFR* section.

Figure 14. System Clock Sources



Bandgap-Monitored Interrupt and Reset Generation

The power monitor in the DS89C430 monitors the V_{CC} pin in relation to the on-chip bandgap voltage reference. Whenever V_{CC} falls below V_{PFW}, an interrupt is generated if the corresponding power-fail interrupt-enable bit EPFI (WDCON.5) is set, causing the device to vector to address 33h. The power-fail interrupt status bit PFI (WDCON.4) is set any time V_{CC} transitions below V_{PFW}, and can only be cleared by software once set. Similarly, as V_{CC} falls below V_{RST}, a reset is issued internally to halt program execution. Following power-up, a power-on reset initiates a power-on reset timeout before starting program execution. When V_{CC} is first applied to the DS89C430, the processor is held in reset until $V_{CC} > V_{RST}$ and a delay of 65,536 oscillator cycles has elapsed, to ensure that power is within tolerance and the clock source has had time to stabilize. Once the reset timeout period has elapsed, the reset condition is removed automatically and software execution begins at the reset vector location of 0000h. The power-on reset flag POR (WDCON.6) is set to logic 1 to indicate a power-on reset has occurred, and can only be cleared by software.

When the DS89C430 enters stop mode, the bandgap, reset comparator, and power-fail interrupt comparator are automatically disabled to conserve power if the BGS (EXIF.0) bit is set to logic 0. This is the lowest power mode. If BGS is set to logic 1, the bandgap reference, reset comparator, and the power-fail comparator are powered up, although in a mode that reduces their power consumption.

Watchdog Timer

The watchdog timer functions as the source of both the watchdog interrupt and the watchdog reset. When the clock divider is set to 10b, the interrupt timeout has a default divide ratio of 2^{17} of the crystal oscillator clock, with the watchdog reset set to time out 512 system clock cycles later. This results in a 33MHz crystal oscillator producing an interrupt timeout every 3.9718ms, followed 15.5µs later by a watchdog reset. The watchdog timer is reset to the default divide ratio following any reset. Using the WD0 and WD1 bits in the clock control (CKCON.6 and 7) register, other divide ratios can be selected for longer watchdog interrupt periods. Table 13 summarizes the watchdog bits settings and the timeout values. **Note:** All watchdog timer reset timeouts follow the programmed interrupt timeouts by 512 system clock cycles, which equates to varying numbers of oscillator cycles depending on the clock divide (CD1:0) and crystal multiplier settings.

Table 13. Watchdog Timeout Value (In Number of Oscillator Clocks)

4X/$\overline{2X}$	CD1:0	WATCHDOG INTERRUPT TIMEOUT				WATCHDOG RESET TIMEOUT			
		WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11	WD1:0 = 00	WD1:0 = 01	WD1:0 = 10	WD1:0 = 11
1	00	2^{15}	2^{18}	2^{21}	2^{24}	2^{15} + 128	2^{18} + 128	2^{21} + 128	2^{24} + 128
0	00	2^{16}	2^{19}	2^{22}	2^{25}	2^{16} + 256	2^{19} + 256	2^{22} + 256	2^{25} + 256
x	01	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	10	2^{17}	2^{20}	2^{23}	2^{26}	2^{17} + 512	2^{20} + 512	2^{23} + 512	2^{26} + 512
x	11	2^{27}	2^{30}	2^{33}	2^{36}	2^{27} + 524,288	2^{30} + 524,288	2^{33} + 524,288	2^{36} + 524,288

A watchdog control (WDCON) SFR is used for programming the functions. EWT (WDCON.1) is the enable for the watchdog timer-reset function and RWT (WDCON.0) is the bit used to restart the watchdog timer. Setting the RWT bit restarts the timer for another full interval. If the watchdog timer-reset function is masked by the EWT bit and no resets are issued to the timer through the RWT bit, the watchdog timer generates interrupt timeouts at a rate determined by the programmed divide ratio. WDIF (WDCON.3) is the interrupt flag set at timer termination and WTRF (WDCON.2) is the reset flag set following a watchdog reset timeout. Setting the EWDI bit (EIE.4) enables the watchdog interrupt. The watchdog timer reset and interrupt timeouts are measured by counting system clock cycles.

An independent watchdog timer functions as the crystal startup counter to count 65,536 crystal clock cycles before allowing the crystal oscillator to function as the system clock. This warmup time is verified by the watchdog timer following each power-up as well as each time the crystal is restarted following a stop mode. The watchdog is also used to establish a startup time whenever the CTM in the PMR register is set to enable the crystal multiplier (4X/$\overline{2X}$).

One of the watchdog timer applications is for the watchdog to wake up the system from idle mode. The watchdog interrupt can be programmed to allow a system to wake up periodically to sample the external world.

Internal System Reset

A software reset can be initiated by writing a system reset command to the flash control SFR. The reset state is maintained for approximately 90 external clock cycles. During this time, the RST pin is driven to a logic high. Once the reset is removed, the RST pin is driven low, and operation begins from address 0000h.

REVISION HISTORY

DATE	DESCRIPTION
111003	New product release.
032204	*DC Electrical Characteristics* table: Corrected typo—Under Supply Current for Active and Idle Mode, changed Units from "µA" to "mA." Note 15: Changed number of external clock cyles per system clock and minimum external clock speeds. *Flash Memory Programming Characteristics* table: Removed Note 20 (room temperature only) from the Data Retention parameter.
060204	Changed Write/Erase Endurance parameter from 20,000 cycles to 10,000 cycles. Removed original *Table 5. Parallel Programming Instruction Set*, and replaced it with a paragraph introducing the subject and advising interested parties to contact the factory for more information. Clarified IAP programming sequence.
060805	Added lead-free devices to *Ordering Information* table.
091906	Removed references to DS89C440 and/or added "Contact factory or replace with DS89C430 or DS89C450."
040507	Added clarification to the *Security Features* section and *Table 3* that flash security levels 1, 2, and 3 should not be used when executing external code (page 22); corrected Figure 8 to show PSEN high through the second machine cycle (page 28).