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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	CIP-51™
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f850-c-gm

1. Electrical Specifications

1.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 1.1, unless stated otherwise.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		2.2	—	3.6	V
System Clock Frequency	f _{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T _A	Commercial Grade Devices (-GM, -GS, -GU)	-40	—	85	°C
		Industrial Grade Devices (-IM, -IS, -IU)	-40	—	125	°C

Note: All voltages with respect to GND

Table 1.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (–Gx Devices, -40°C to +85°C)						
Normal Mode—Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 24.5 MHz ²	—	4.45	4.85	mA
		F _{SYSCLK} = 1.53 MHz ²	—	915	1150	μA
		F _{SYSCLK} = 80 kHz ³ , T _A = 25 °C	—	250	290	μA
		F _{SYSCLK} = 80 kHz ³	—	250	380	μA
Idle Mode—Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 24.5 MHz ²	—	2.05	2.3	mA
		F _{SYSCLK} = 1.53 MHz ²	—	550	700	μA
		F _{SYSCLK} = 80 kHz ³ , T _A = 25 °C	—	125	130	μA
		F _{SYSCLK} = 80 kHz ³	—	125	200	μA
Stop Mode—Core halted and all clocks stopped, Supply monitor off.	I _{DD}	Internal LDO ON, T _A = 25 °C	—	105	120	μA
		Internal LDO ON	—	105	170	μA
		Internal LDO OFF	—	0.2	—	μA

Notes:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

3. Pin Definitions

3.1. C8051F850/1/2/3/4/5 QSOP24 Pin Definitions

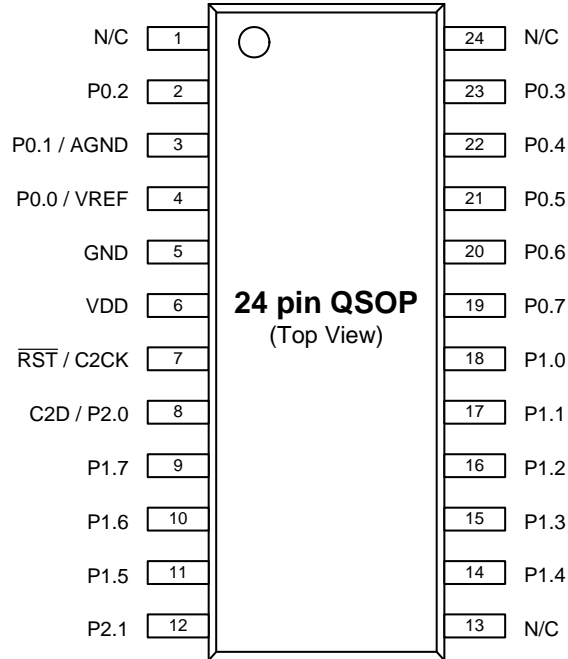


Figure 3.1. C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU Pinout

Table 3.1. Pin Definitions for C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	5			
VDD	Power	6			
RST / C2CK	Active-low Reset / C2 Debug Clock	7			

6. QFN-20 Package Specifications

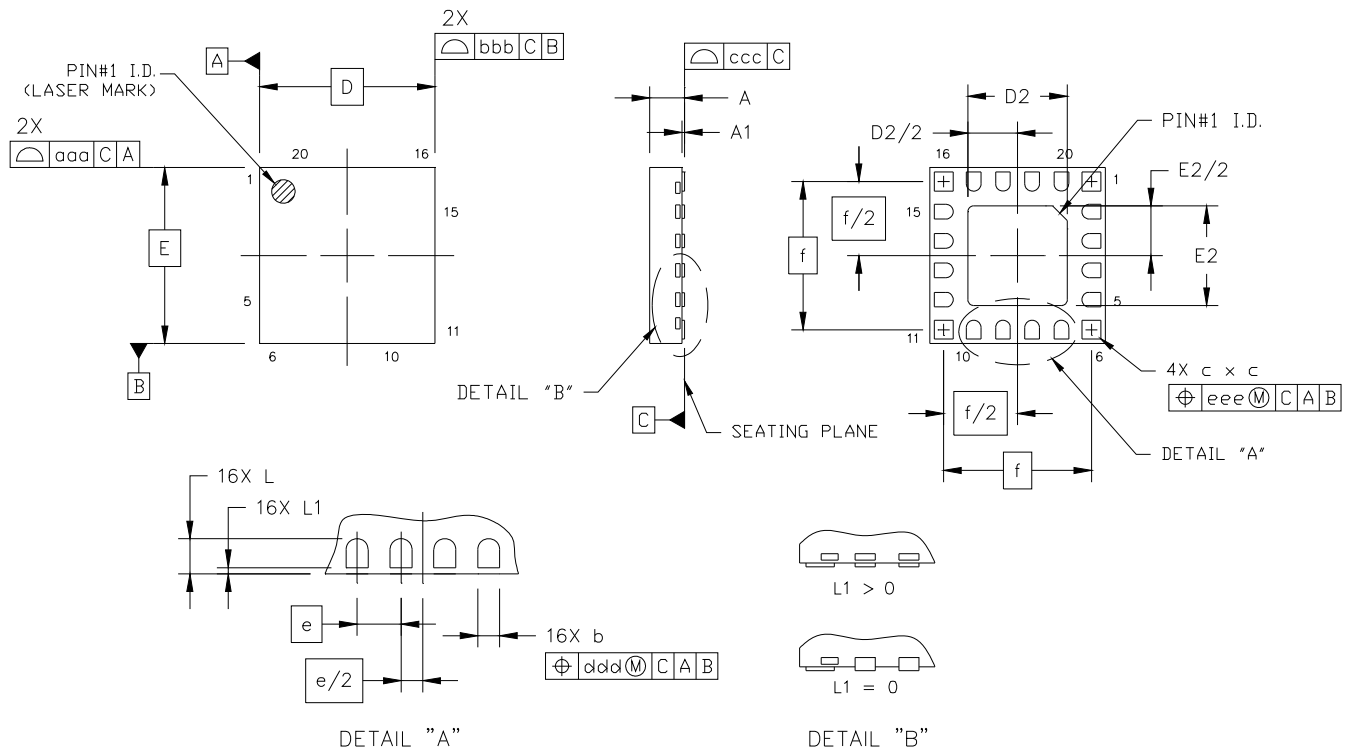


Figure 6.1. QFN-20 Package Drawing

Table 6.1. QFN-20 Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.25	0.30	0.35
D	3.00 BSC		
D2	1.6	1.70	1.8
e	0.50 BSC		
E	3.00 BSC		
E2	1.6	1.70	1.8
f	2.53 BSC		
L	0.3	0.40	0.5
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

Table 10.1. Flash Security Summary (Continued)

Read contents of Lock Byte (if no pages are locked)	Permitted	Permitted	N/A
Read contents of Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Erase page containing Lock Byte (if no pages are locked)	Permitted	Permitted	N/A
Erase page containing Lock Byte—Unlock all pages (if any page is locked)	C2 Device Erase Only	Flash Error Reset	Flash Error Reset
Lock additional pages (change 1s to 0s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Unlock individual pages (change 0s to 1s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Read, Write or Erase Reserved Area	Not Permitted	Flash Error Reset	Flash Error Reset

C2 Device Erase—Erases all flash pages including the page containing the Lock Byte.

Flash Error Reset —Not permitted; Causes Flash Error Device Reset (FERROR bit in RSTSRC is '1' after reset).

- All prohibited operations that are performed via the C2 interface are ignored (do not cause device reset).
- Locking any flash page also locks the page containing the Lock Byte.
- Once written to, the Lock Byte cannot be modified except by performing a C2 Device Erase.
- If user code writes to the Lock Byte, the Lock does not take effect until the next device reset.

11.1. Device Identification Registers

Register 11.1. DEVICEID: Device Identification

Bit	7	6	5	4	3	2	1	0
Name	DEVICEID							
Type	R							
Reset	0	0	1	1	0	0	0	0
SFR Address: 0xB5								

Table 11.2. DEVICEID Register Bit Descriptions

Bit	Name	Function
7:0	DEVICEID	Device ID. This read-only register returns the 8-bit device ID: 0x30 (C8051F85x/86x).

13.1.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the controller core to enter stop mode as soon as the instruction that sets the bit completes execution. Before entering stop mode, the system clock must be sourced by the internal high-frequency oscillator. In stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering stop mode. Stop mode can only be terminated by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout.

13.2. LDO Regulator

C8051F85x/86x devices include an internal regulator that regulates the internal core and logic supply. Under default conditions, the internal regulator will remain on when the device enters STOP mode. This allows any enabled reset source to generate a reset for the device and bring the device out of STOP mode. For additional power savings, the STOPCF bit can be used to shut down the regulator and the internal power network of the device when the part enters STOP mode. When STOPCF is set to 1, the $\overline{\text{RST}}$ pin and a full power cycle of the device are the only methods of generating a reset.

13.3. Power Control Registers

Register 13.1. PCON: Power Control

Bit	7	6	5	4	3	2	1	0
Name	GF						STOP	IDLE
Type	RW						RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x87								

Table 13.1. PCON Register Bit Descriptions

Bit	Name	Function
7:2	GF	General Purpose Flags 5-0. These are general purpose flags for use under software control.
1	STOP	Stop Mode Select. Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0.
0	IDLE	Idle Mode Select. Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0.

Register 14.3. ADC0CF: ADC0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	ADSC					AD8BE	ADTM	ADGN
Type	RW					RW	RW	RW
Reset	1	1	1	1	1	0	0	0

SFR Address: 0xBC

Table 14.6. ADC0CF Register Bit Descriptions

Bit	Name	Function
7:3	ADSC	SAR Clock Divider. This field sets the ADC clock divider value. It should be configured to be as close to the maximum SAR clock speed as the datasheet will allow. The SAR clock frequency is given by the following equation: $F_{CLKSAR} = \frac{F_{ADCCLK}}{ADSC + 1}$ F_{ADCCLK} is equal to the selected SYSCCLK when ADBMEN is 0 and the high-frequency oscillator when ADBMEN is 1.
2	AD8BE	8-Bit Mode Enable. 0: ADC0 operates in 10-bit or 12-bit mode (normal operation). 1: ADC0 operates in 8-bit mode.
1	ADTM	Track Mode. Selects between Normal or Delayed Tracking Modes. 0: Normal Track Mode. When ADC0 is enabled, conversion begins immediately following the start-of-conversion signal. 1: Delayed Track Mode. When ADC0 is enabled, conversion begins 4 SAR clock cycles following the start-of-conversion signal. The ADC is allowed to track during this time.
0	ADGN	Gain Control. 0: The on-chip PGA gain is 0.5. 1: The on-chip PGA gain is 1.

15. CIP-51 Microcontroller Core

The C8051F85x/86x uses the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The MCU family has a superset of all the peripherals included with a standard 8051. The CIP-51 also includes on-chip debug hardware and interfaces directly with the analog and digital subsystems providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 15.1 for a block diagram). The CIP-51 includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 25 MIPS Peak Throughput with 25 MHz Clock
- 0 to 25 MHz Clock Frequency
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- On-chip Debug Logic
- Program and Data Memory Security

15.1. Performance

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. The CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

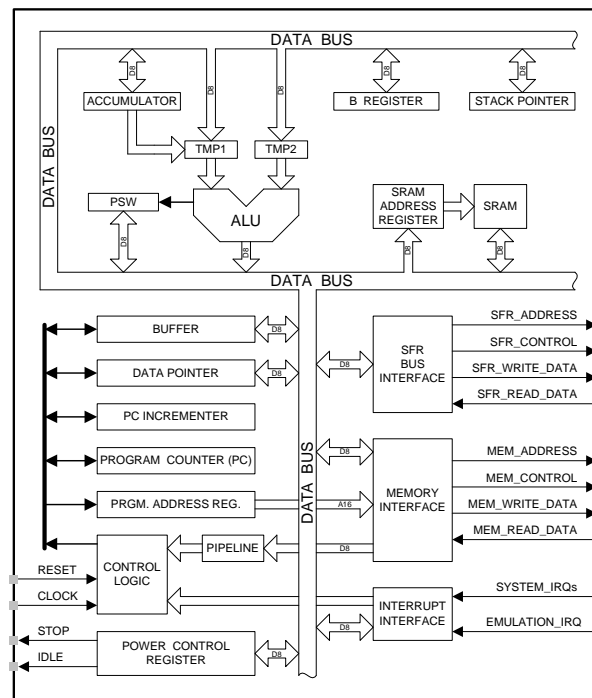


Figure 15.1. CIP-51 Block Diagram

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
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16.3. External Clock

An external CMOS clock source is also supported by the C8051F85x/86x family. The EXTCLK pin on the device serves as the external clock input when running in this mode. The EXTCLK input may also be used to clock some of the digital peripherals (e.g., Timers, PCA, etc.) while SYSCLK runs from one of the internal oscillator sources. When not selected as the SYSCLK source, the EXTCLK input is always re-synchronized to SYSCLK.

16.4. Clock Selection

The CLKSEL register is used to select the clock source for the system. The CLKSL field selects which oscillator source is used as the system clock, while CLKDIV controls the programmable divider. CLKSL must be set to 01b for the system clock to run from the external oscillator; however the external oscillator may still clock certain peripherals (timers, PCA) when the internal oscillator is selected as the system clock. In these cases, the external oscillator source is synchronized to the SYSCLK source. The system clock may be switched on-the-fly between any of the oscillator sources so long as the selected clock source is enabled and has settled, and CLKDIV may be changed at any time.

The internal high-frequency and low-frequency oscillators require little start-up time and may be selected as the system clock immediately following the register write which enables the oscillator. When selecting the EXTCLK pin as a clock input source, the pin should be skipped in the crossbar and configured as a digital input. Firmware should ensure that the external clock source is present or enable the missing clock detector before switching the CLKSL field.

Table 17.1. CMP0 Positive Input Multiplexer Channels

CMXP Setting in Register CPT0MX	Signal Name	QSOP24 Pin Name	QFN20 Pin Name	SOIC16 Pin Name
0000	CP0P.0	P0.0	P0.0	P0.0
0001	CP0P.1	P0.1	P0.1	P0.1
0010	CP0P.2	P0.2	P0.2	P0.2
0011	CP0P.3	P0.3	P0.3	P0.3
0100	CP0P.4	P0.4	P0.4	P0.4
0101	CP0P.5	P0.5	P0.5	P0.5
0110	CP0P.6	P0.6	P0.6	Reserved
0111	CP0P.7	P0.7	P0.7	Reserved
1000	LDO	Internal 1.8 V LDO Output		
1001-1111	None	No connection		

Table 17.2. CMP0 Negative Input Multiplexer Channels

CMXN Setting in Register CPT0MX	Signal Name	QSOP24 Pin Name	QFN20 Pin Name	SOIC16 Pin Name
0000	CP0N.0	P0.0	P0.0	P0.0
0001	CP0N.1	P0.1	P0.1	P0.1
0010	CP0N.2	P0.2	P0.2	P0.2
0011	CP0N.3	P0.3	P0.3	P0.3
0100	CP0N.4	P0.4	P0.4	P0.4
0101	CP0N.5	P0.5	P0.5	P0.5
0110	CP0N.6	P0.6	P0.6	Reserved
0111	CP0N.7	P0.7	P0.7	Reserved
1000	GND	GND		
1001-1111	None	No connection		

Register 18.4. CRC0AUTO: CRC0 Automatic Control

Bit	7	6	5	4	3	2	1	0
Name	AUTOEN	Reserved	CRCST					
Type	RW	R	RW					
Reset	0	0	0	0	0	0	0	0

SFR Address: 0xD2

Table 18.5. CRC0AUTO Register Bit Descriptions

Bit	Name	Function
7	AUTOEN	Automatic CRC Calculation Enable. When AUTOEN is set to 1, any write to CRC0CN will initiate an automatic CRC starting at flash sector CRCST and continuing for CRCCNT sectors.
6	Reserved	Must write reset value.
5:0	CRCST	Automatic CRC Calculation Starting Block. These bits specify the flash block to start the automatic CRC calculation. The starting address of the first flash block included in the automatic CRC calculation is CRCST x block_size, where block_size is 256 bytes.

Register 20.6. PCA0L: PCA Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0L							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xF9								

Table 20.8. PCA0L Register Bit Descriptions

Bit	Name	Function
7:0	PCA0L	PCA Counter/Timer Low Byte. The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.

Register 20.7. PCA0H: PCA Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0H							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xFA								

Table 20.9. PCA0H Register Bit Descriptions

Bit	Name	Function
7:0	PCA0H	PCA Counter/Timer High Byte. The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer. Reads of this register will read the contents of a snapshot register, whose contents are updated only when the contents of PCA0L are read.

Register 21.10. P0SKIP: Port 0 Skip

Bit	7	6	5	4	3	2	1	0
Name	P0SKIP							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xD4								

Table 21.13. P0SKIP Register Bit Descriptions

Bit	Name	Function
7:0	P0SKIP	Port 0 Skip. These bits select port pins to be skipped by the crossbar decoder. Port pins used for analog, special functions or GPIO should be skipped. 0: Corresponding P0.x pin is not skipped by the crossbar. 1: Corresponding P0.x pin is skipped by the crossbar.

23.3. SPI0 Slave Mode Operation

When SPI0 is enabled and not configured as a master, it will operate as a SPI slave. As a slave, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter in the SPI0 logic counts SCK edges. When 8 bits have been shifted through the shift register, the SPIF flag is set to logic 1, and the byte is copied into the receive buffer. Data is read from the receive buffer by reading SPI0DAT. A slave device cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPI0DAT. Writes to SPI0DAT are double-buffered, and are placed in the transmit buffer first. If the shift register is empty, the contents of the transmit buffer will immediately be transferred into the shift register. When the shift register already contains data, the SPI will load the shift register with the transmit buffer's contents after the last SCK edge of the next (or current) SPI transfer.

When configured as a slave, SPI0 can be configured for 4-wire or 3-wire operation. The default, 4-wire slave mode, is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In 4-wire mode, the NSS signal is routed to a port pin and configured as a digital input. SPI0 is enabled when NSS is logic 0, and disabled when NSS is logic 1. The bit counter is reset on a falling edge of NSS. Note that the NSS signal must be driven low at least 2 system clocks before the first active edge of SCK for each byte transfer. Figure 23.4 shows a connection diagram between two slave devices in 4-wire slave mode and a master device.

The 3-wire slave mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. NSS is not used in this mode, and is not mapped to an external port pin through the crossbar. Since there is no way of uniquely addressing the device in 3-wire slave mode, SPI0 must be the only slave device present on the bus. It is important to note that in 3-wire slave mode there is no external means of resetting the bit counter that determines when a full byte has been received. The bit counter can only be reset by disabling and re-enabling SPI0 with the SPIEN bit. Figure 23.3 shows a connection diagram between a slave device in 3-wire slave mode and a master device.

23.4. SPI0 Interrupt Sources

When SPI0 interrupts are enabled, the following four flags will generate an interrupt when they are set to logic 1:

All of the following bits must be cleared by software.

- The SPI Interrupt Flag, SPIF (SPI0CN.7) is set to logic 1 at the end of each byte transfer. This flag can occur in all SPI0 modes.
- The Write Collision Flag, WCOL (SPI0CN.6) is set to logic 1 if a write to SPI0DAT is attempted when the transmit buffer has not been emptied to the SPI shift register. When this occurs, the write to SPI0DAT will be ignored, and the transmit buffer will not be written. This flag can occur in all SPI0 modes.
- The Mode Fault Flag MODF (SPI0CN.5) is set to logic 1 when SPI0 is configured as a master, and for multi-master mode and the NSS pin is pulled low. When a Mode Fault occurs, the MSTEN and SPIEN bits in SPI0CN are set to logic 0 to disable SPI0 and allow another master device to access the bus.
- The Receive Overrun Flag RXOVRN (SPI0CN.4) is set to logic 1 when configured as a slave, and a transfer is completed and the receive buffer still holds an unread byte from a previous transfer. The new byte is not transferred to the receive buffer, allowing the previously received data byte to be read. The data byte which caused the overrun is lost.

23.5. Serial Clock Phase and Polarity

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI0 Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0

24. System Management Bus / I²C (SMBus0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

Reads and writes to the SMBus by the system controller are byte oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/20th of the system clock as a master or slave (this can be faster than allowed by the SMBus specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation. The SMBus peripherals can be fully driven by software (i.e., software accepts/rejects slave addresses, and generates ACKs), or hardware slave address recognition and automatic ACK generation can be enabled to minimize software overhead. A block diagram of the SMBus0 peripheral is shown in Figure 24.1.

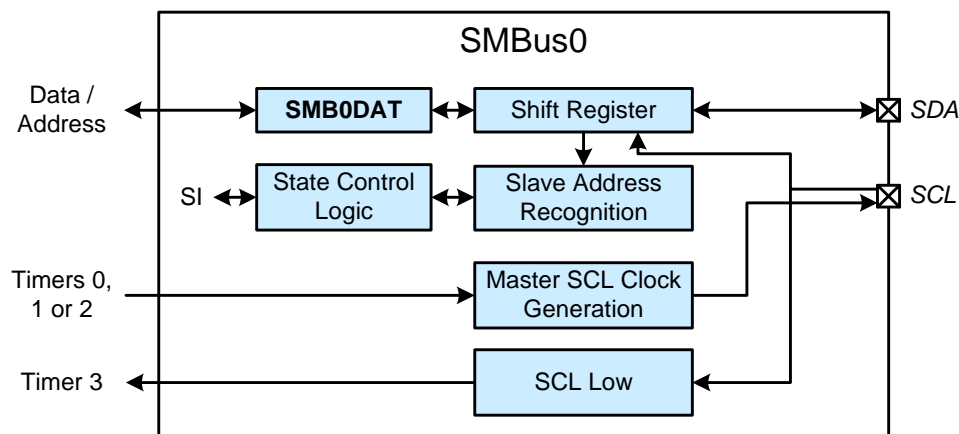


Figure 24.1. SMBus0 Block Diagram

24.7. I2C / SMBus Control Registers

Register 24.1. SMB0CF: SMBus0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	ENSMB	INH	BUSY	EXTHOLD	SMBTOE	SMBFTE	SMBCS	
Type	RW	RW	R	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xC1								

Table 24.7. SMB0CF Register Bit Descriptions

Bit	Name	Function
7	ENSMB	SMBus0 Enable. This bit enables the SMBus0 interface when set to 1. When enabled, the interface constantly monitors the SDA and SCL pins.
6	INH	SMBus0 Slave Inhibit. When this bit is set to logic 1, the SMBus0 does not generate an interrupt when slave events occur. This effectively removes the SMBus0 slave from the bus. Master Mode interrupts are not affected.
5	BUSY	SMBus0 Busy Indicator. This bit is set to logic 1 by hardware when a transfer is in progress. It is cleared to logic 0 when a STOP or free-timeout is sensed.
4	EXTHOLD	SMBus0 Setup and Hold Time Extension Enable. This bit controls the SDA setup and hold times. 0: SDA Extended Setup and Hold Times disabled. 1: SDA Extended Setup and Hold Times enabled.
3	SMBTOE	SMBus0 SCL Timeout Detection Enable. This bit enables SCL low timeout detection. If set to logic 1, the SMBus0 forces Timer 3 to reload while SCL is high and allows Timer 3 to count when SCL goes low. If Timer 3 is configured to Split Mode, only the High Byte of the timer is held in reload while SCL is high. Timer 3 should be programmed to generate interrupts at 25 ms, and the Timer 3 interrupt service routine should reset SMBus0 communication.
2	SMBFTE	SMBus0 Free Timeout Detection Enable. When this bit is set to logic 1, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods.

25. Timers (Timer0, Timer1, Timer2 and Timer3)

Each MCU in the C8051F85x/86x family includes four counter/timers: two are 16-bit counter/timers compatible with those found in the standard 8051, and two are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 and Timer 3 are also identical and offer both 16-bit and split 8-bit timer functionality with auto-reload capabilities. Timer 2 and Timer 3 both offer a capture function, but are different in their system-level connections. Timer 2 is capable of performing a capture function on an external signal input routed through the crossbar, while the Timer 3 capture is dedicated to the low-frequency oscillator output. Table 25.1 summarizes the modes available to each timer.

Table 25.1. Timer Modes

Timer 0 and Timer 1 Modes	Timer 2 Modes	Timer 3 Modes
13-bit counter/timer	16-bit timer with auto-reload	16-bit timer with auto-reload
16-bit counter/timer	Two 8-bit timers with auto-reload	Two 8-bit timers with auto-reload
8-bit counter/timer with auto-reload	Input pin capture	Low-frequency oscillator capture
Two 8-bit counter/timers (Timer 0 only)		

Timers 0 and 1 may be clocked by one of five sources, determined by the Timer Mode Select bits (T1M–T0M) and the Clock Scale bits (SCA1–SCA0). The Clock Scale bits define a pre-scaled clock from which Timer 0 and/or Timer 1 may be clocked.

Timer 0/1 may then be configured to use this pre-scaled clock signal or the system clock. Timer 2 and Timer 3 may be clocked by the system clock, the system clock divided by 12, or the external oscillator clock source divided by 8.

Timer 0 and Timer 1 may also be operated as counters. When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin (T0 or T1). Events with a frequency of up to one-fourth the system clock frequency can be counted. The input signal need not be periodic, but it must be held at a given level for at least two full system clock cycles to ensure the level is properly sampled.

All four timers are capable of clocking other peripherals and triggering events in the system. The individual peripherals select which timer to use for their respective functions. Table 25.2 summarizes the peripheral connections for each timer. Note that the Timer 2 and Timer 3 high overflows apply to the full timer when operating in 16-bit mode or the high-byte timer when operating in 8-bit split mode.

Table 25.2. Timer Peripheral Clocking / Event Triggering

Function	T0 Overflow	T1 Overflow	T2 High Overflow	T2 Low Overflow	T3 High Overflow	T3 Low Overflow
UART0 Baud Rate		X				
SMBus0 Clock Rate	X	X	X	X		
SMBus0 SCL Low Timeout					X	
PCA0 Clock	X					

Register 25.3. TMOD: Timer 0/1 Mode

Bit	7	6	5	4	3	2	1	0
Name	GATE1	CT1	T1M		GATE0	CT0	T0M	
Type	RW	RW	RW		RW	RW	RW	
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x89								

Table 25.5. TMOD Register Bit Descriptions

Bit	Name	Function
7	GATE1	Timer 1 Gate Control. 0: Timer 1 enabled when TR1 = 1 irrespective of INT1 logic level. 1: Timer 1 enabled only when TR1 = 1 and INT1 is active as defined by bit IN1PL in register IT01CF.
6	CT1	Counter/Timer 1 Select. 0: Timer Mode. Timer 1 increments on the clock defined by T1M in the CKCON register. 1: Counter Mode. Timer 1 increments on high-to-low transitions of an external pin (T1).
5:4	T1M	Timer 1 Mode Select. These bits select the Timer 1 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Timer 1 Inactive
3	GATE0	Timer 0 Gate Control. 0: Timer 0 enabled when TR0 = 1 irrespective of INT0 logic level. 1: Timer 0 enabled only when TR0 = 1 and INT0 is active as defined by bit IN0PL in register IT01CF.
2	CT0	Counter/Timer 0 Select. 0: Timer Mode. Timer 0 increments on the clock defined by T0M in the CKCON register. 1: Counter Mode. Timer 0 increments on high-to-low transitions of an external pin (T0).
1:0	T0M	Timer 0 Mode Select. These bits select the Timer 0 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Two 8-bit Counter/Timers

Table 26.2. SCON0 Register Bit Descriptions

Bit	Name	Function
0	RI	Receive Interrupt Flag. Set to 1 by hardware when a byte of data has been received by UART0 (set at the STOP bit sampling time). When the UART0 interrupt is enabled, setting this bit to 1 causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.