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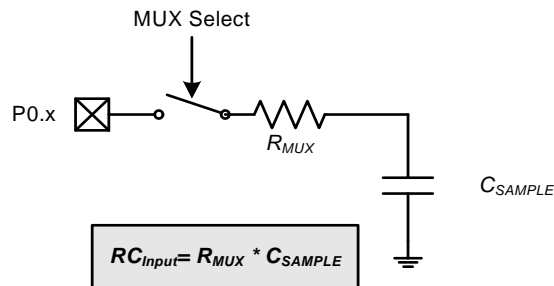
Details

Product Status	Active
Core Processor	CIP-51™
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f850-c-gmr

Table 3.2. Pin Definitions for C8051F850/1/2/3/4/5-GM and C8051F850/1/2/3/4/5-IM

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
P0.0	Standard I/O	2	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0 VREF
P0.1	Standard I/O	1	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CP0P.1 CP0N.1 AGND
P0.2	Standard I/O	20	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CP0P.2 CP0N.2
P0.3	Standard I/O	19	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CP0P.3 CP0N.3
P0.4	Standard I/O	18	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CP0P.4 CP0N.4
P0.5	Standard I/O	17	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CP0P.5 CP0N.5
P0.6	Standard I/O	16	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CP0P.6 CP0N.6
P0.7	Standard I/O	15	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CP0P.7 CP0N.7

n is the ADC resolution in bits (8/10/12).



Note: The value of CSAMPLE depends on the PGA Gain. See electrical specifications for details.

Figure 14.4. ADC0 Equivalent Input Circuits

14.2.5. Gain Setting

The ADC has gain settings of 1x and 0.5x. In 1x mode, the full scale reading of the ADC is determined directly by VREF. In 0.5x mode, the full-scale reading of the ADC occurs when the input voltage is VREF x 2. The 0.5x gain setting can be useful to obtain a higher input voltage range when using a small VREF voltage, or to measure input voltages that are between VREF and VDD. Gain settings for the ADC are controlled by the ADGN bit in register ADC0CF. Note that even with a gain setting of 0.5, voltages above the supply rail cannot be measured directly by the ADC.

14.3. 8-Bit Mode

Setting the ADC08BE bit in register ADC0CF to 1 will put the ADC in 8-bit mode. In 8-bit mode, only the 8 MSBs of data are converted, allowing the conversion to be completed in fewer SAR clock cycles than a 10-bit conversion. The two LSBs of a conversion are always 00 in this mode, and the ADC0L register will always read back 0x00.

14.4. 12-Bit Mode

When configured for 12-bit conversions, the ADC performs four 10-bit conversions using four different reference voltages and combines the results into a single 12-bit value. Unlike simple averaging techniques, this method provides true 12-bit resolution of AC or DC input signals without depending on noise to provide dithering. The converter also employs a hardware dynamic element matching algorithm that reconfigures the largest elements of the internal DAC for each of the four 10-bit conversions. This reconfiguration cancels any matching errors and enables the converter to achieve 12-bit linearity performance to go along with its 12-bit resolution.

The 12-bit mode is enabled by setting the AD12BE bit in register ADC0AC to logic 1 and configuring the ADC in burst mode (ADBMEN = 1) for four or more conversions. The conversion can be initiated using any of the conversion start sources, and the 12-bit result will appear in the ADC0H and ADC0L registers. Since the 12-bit result is formed from a combination of four 10-bit results, the maximum output value is $4 \times (1023) = 4092$, rather than the max value of $(2^{12} - 1) = 4095$ that is produced by a traditional 12-bit converter. To further increase resolution, the burst mode repeat value may be configured to any multiple of four conversions. For example, if a repeat value of 16 is selected, the ADC0 output will be a 14-bit number (sum of four 12-bit numbers) with 13 effective bits of resolution.

The AD12SM bit in register ADC0TK controls when the ADC will track and sample the input signal. When AD12SM is set to 1, the selected input signal will be tracked before the first conversion of a set and held internally during all four conversions. When AD12SM is cleared to 0, the ADC will track and sample the selected input before each of the four conversions in a set. When maximum throughput (180-200 ksp/s) is

Table 15.1. CIP-51 Instruction Set Summary

Mnemonic	Description	Bytes	Clock Cycles
Arithmetic Operations			
ADD A, Rn	Add register to A	1	1
ADD A, direct	Add direct byte to A	2	2
ADD A, @Ri	Add indirect RAM to A	1	2
ADD A, #data	Add immediate to A	2	2
ADDC A, Rn	Add register to A with carry	1	1
ADDC A, direct	Add direct byte to A with carry	2	2
ADDC A, @Ri	Add indirect RAM to A with carry	1	2
ADDC A, #data	Add immediate to A with carry	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	1	2
SUBB A, #data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	2
INC @Ri	Increment indirect RAM	1	2
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	2
DEC @Ri	Decrement indirect RAM	1	2
INC DPTR	Increment Data Pointer	1	1
MUL AB	Multiply A and B	1	4
DIV AB	Divide A by B	1	8
DA A	Decimal adjust A	1	1
Logical Operations			
ANL A, Rn	AND Register to A	1	1
ANL A, direct	AND direct byte to A	2	2
ANL A, @Ri	AND indirect RAM to A	1	2
ANL A, #data	AND immediate to A	2	2
ANL direct, A	AND A to direct byte	2	2
ANL direct, #data	AND immediate to direct byte	3	3
ORL A, Rn	OR Register to A	1	1
ORL A, direct	OR direct byte to A	2	2
ORL A, @Ri	OR indirect RAM to A	1	2
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	2
ORL direct, #data	OR immediate to direct byte	3	3

Register 18.3. CRC0DAT: CRC0 Data Output

Bit	7	6	5	4	3	2	1	0
Name	CRC0DAT							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xDE								

Table 18.4. CRC0DAT Register Bit Descriptions

Bit	Name	Function
7:0	CRC0DAT	CRC Data Output. Each read or write performed on CRC0DAT targets the CRC result bits pointed to by the CRC0 Result Pointer (CRC0PNT bits in CRC0CN).
Note: CRC0DAT may not be valid for one cycle after setting the CRC0INIT bit in the CRC0CN register to 1. Any time CRC0INIT is written to 1 by firmware, at least one instruction should be performed before reading CRC0DAT.		

20.1. PCA Counter/Timer

The 16-bit PCA counter/timer consists of two 8-bit SFRs: PCA0L and PCA0H. PCA0H is the high byte of the 16-bit counter/timer and PCA0L is the low byte. Reading PCA0L automatically latches the value of PCA0H into a “snapshot” register; the following PCA0H read accesses this “snapshot” register. **Reading the PCA0L Register first guarantees an accurate reading of the entire 16-bit PCA0 counter.** Reading PCA0H or PCA0L does not disturb the counter operation. The CPS2–CPS0 bits in the PCA0MD register select the timebase for the counter/timer as shown in Table 20.1.

When the counter/timer overflows from 0xFFFF to 0x0000, the Counter Overflow Flag (CF) in PCA0MD is set to logic 1 and an interrupt request is generated if CF interrupts are enabled. Setting the ECF bit in PCA0MD to logic 1 enables the CF flag to generate an interrupt request. The CF bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Clearing the CIDL bit in the PCA0MD register allows the PCA to continue normal operation while the CPU is in Idle mode.

Table 20.1. PCA Timebase Input Options

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)*
1	0	0	System clock
1	0	1	External oscillator source divided by 8*
1	1	0	Low frequency oscillator divided by 8*
1	1	1	Reserved

*Note: Synchronized with the system clock.

20.2. PCA0 Interrupt Sources

The PCA0 module shares one interrupt vector among all of its modules. There are several event flags that can be used to generate a PCA0 interrupt. They are: the main PCA counter overflow flag (CF), which is set upon a 16-bit overflow of the PCA0 counter, an intermediate overflow flag (COVF), which can be set on an overflow from the 8th - 11th bit of the PCA0 counter, and the individual flags for each PCA channel (CCFn), which are set according to the operation mode of that module. These event flags are always set when the trigger condition occurs. Each of these flags can be individually selected to generate a PCA0 interrupt, using the corresponding interrupt enable flag (ECF for CF, ECOV for COVF, and ECCFn for each CCFn). PCA0 interrupts must be globally enabled before any individual interrupt sources are recognized by the processor. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1.

Equation 20.4 describes the duty cycle when CEXnPOL in the PCA0POL register is cleared to 0. Equation 20.5 describes the duty cycle when CEXnPOL in the PCA0POL register is set to 1. The equations are true only when the lowest N bits of the PCA0CPn register are not all 0's or all 1's. With CEXnPOL equal to zero, 100% duty cycle is produced when the lowest N bits of PCA0CPn are all 0, and 0% duty cycle is produced when the lowest N bits of PCA0CPn are all 1. For a given PCA resolution, the unused high bits in the PCA0 counter and the PCA0CPn compare registers are ignored, and only the used bits of the PCA0CPn register determine the duty cycle.

Note that although the PCA0CPn compare register determines the duty cycle, it is not always appropriate for firmware to update this register directly. See the sections on 8 to 11-bit and 16-bit PWM mode for additional details on adjusting duty cycle in the various modes.

$$\text{Duty Cycle} = \frac{(2^N - \text{PCA0CPn}) - \frac{1}{2}}{2^N}$$

Equation 20.4. N-bit Center-Aligned PWM Duty Cycle With CEXnPOL = 0 (N = PWM resolution)

$$\text{Duty Cycle} = \frac{\text{PCA0CPn} + \frac{1}{2}}{2^N}$$

Equation 20.5. N-bit Center-Aligned PWM Duty Cycle With CEXnPOL = 1 (N = PWM resolution)

20.4.4. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. 16-bit PWM mode is independent of the other (8 through 11-bit) PWM modes. The entire PCA0CP register is used to determine the duty cycle in 16-bit PWM mode.

To output a varying duty cycle, new value writes should be synchronized with the PCA CCFn match flag to ensure seamless updates.

16-Bit PWM mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, the match interrupt flag should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. If the MATn bit is set to 1, the CCFn flag for the module will be set each time a match edge or up edge occurs. The CF flag in PCA0CN can be used to detect the overflow or down edge.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

Register 20.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	Reserved			CPS			ECF
Type	RW	R			RW			RW
Reset	0	0	0	0	0	0	0	0

SFR Address: 0xD9

Table 20.4. PCA0MD Register Bit Descriptions

Bit	Name	Function
7	CIDL	<p>PCA Counter/Timer Idle Control. Specifies PCA behavior when CPU is in Idle Mode. 0: PCA continues to function normally while the system controller is in Idle Mode. 1: PCA operation is suspended while the system controller is in Idle Mode.</p>
6:4	Reserved	Must write reset value.
3:1	CPS	<p>PCA Counter/Timer Pulse Select. These bits select the timebase source for the PCA counter. 000: System clock divided by 12. 001: System clock divided by 4. 010: Timer 0 overflow. 011: High-to-low transitions on ECI (max rate = system clock divided by 4). 100: System clock. 101: External clock divided by 8 (synchronized with the system clock). 110: Low frequency oscillator divided by 8. 111: Reserved.</p>
0	ECF	<p>PCA Counter/Timer Overflow Interrupt Enable. This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.</p>

Register 21.3. XBR2: Port I/O Crossbar 2

Bit	7	6	5	4	3	2	1	0
Name	WEAKPUD	XBARE	Reserved					
Type	RW	RW	R					
Reset	0	0	0	0	0	0	0	0

SFR Address: 0xE3

Table 21.6. XBR2 Register Bit Descriptions

Bit	Name	Function
7	WEAKPUD	Port I/O Weak Pullup Disable. 0: Weak Pullups enabled (except for Ports whose I/O are configured for analog mode). 1: Weak Pullups disabled.
6	XBARE	Crossbar Enable. 0: Crossbar disabled. 1: Crossbar enabled.
5:0	Reserved	Must write reset value.

Register 21.15. P1MDOUT: Port 1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xA5								

Table 21.18. P1MDOUT Register Bit Descriptions

Bit	Name	Function
7:0	P1MDOUT	<p>Port 1 Output Mode.</p> <p>These bits are only applicable when the pin is configured for digital mode using the P1MDIN register.</p> <p>0: Corresponding P1.n Output is open-drain.</p> <p>1: Corresponding P1.n Output is push-pull.</p>
<p>Note: Port 1 consists of 8 bits (P1.0-P1.7) on QSOP24 packages and 7 bits (P1.0-P1.6) on QFN20 packages and 4 bits (P1.0-P1.3) on SOIC16 packages.</p>		

-
1. Enable the VDD supply monitor (VMONEN = 1).
 2. Wait for the VDD supply monitor to stabilize (optional).
 3. Enable the VDD monitor as a reset source in the RSTSRC register.

22.4. External Reset

The external $\overline{\text{RST}}$ pin provides a means for external circuitry to force the device into a reset state. Asserting an active-low signal on the $\overline{\text{RST}}$ pin generates a reset; an external pullup and/or decoupling of the $\overline{\text{RST}}$ pin may be necessary to avoid erroneous noise-induced resets. The PINRSF flag is set on exit from an external reset.

22.5. Missing Clock Detector Reset

The Missing Clock Detector (MCD) is a one-shot circuit that is triggered by the system clock. If the system clock remains high or low for more than the MCD time window, the one-shot will time out and generate a reset. After a MCD reset, the MCDRSF flag will read 1, signifying the MCD as the reset source; otherwise, this bit reads 0. Writing a 1 to the MCDRSF bit enables the Missing Clock Detector; writing a 0 disables it. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

22.6. Comparator0 Reset

Comparator0 can be configured as a reset source by writing a 1 to the CORSEF flag. Comparator0 should be enabled and allowed to settle prior to writing to CORSEF to prevent any turn-on chatter on the output from generating an unwanted reset. The Comparator0 reset is active-low: if the non-inverting input voltage (on CP0+) is less than the inverting input voltage (on CP0-), the device is put into the reset state. After a Comparator0 reset, the CORSEF flag will read 1 signifying Comparator0 as the reset source; otherwise, this bit reads '0'. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

22.7. Watchdog Timer Reset

The programmable Watchdog Timer (WDT) can be used to prevent software from running out of control during a system malfunction. The WDT function can be enabled or disabled by software as described in the watchdog timer section. If a system malfunction prevents user software from updating the WDT, a reset is generated and the WDTRSF bit is set to '1'. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

22.8. Flash Error Reset

If a flash read/write/erase or program read targets an illegal address, a system reset is generated. This may occur due to any of the following:

- A flash write or erase is attempted above user code space.
- A flash read is attempted above user code space.
- A program read is attempted above user code space (i.e. a branch instruction to the reserved area).
- A flash read, write or erase attempt is restricted due to a flash security setting.

The FERROR bit is set following a flash error reset. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

22.9. Software Reset

Software may force a reset by writing a 1 to the SWRSF bit. The SWRSF bit will read 1 following a software forced reset. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

Table 23.3. SPI0CN Register Bit Descriptions

Bit	Name	Function
0	SPIEN	SPI0 Enable. 0: SPI disabled. 1: SPI enabled.

minimum setup and hold times for the two EXTHOLD settings. Setup and hold time extensions are typically necessary for SMBus compliance when SYSCLK is above 10 MHz.

Table 24.2. Minimum SDA Setup and Hold Times

EXTHOLD	Minimum SDA Setup Time	Minimum SDA Hold Time
0	$T_{low} - 4$ system clocks or 1 system clock + s/w delay*	3 system clocks
1	11 system clocks	12 system clocks

Note: Setup Time for ACK bit transmissions and the MSB of all data transfers. When using software acknowledgment, the s/w delay occurs between the time SMB0DAT or ACK is written and when SI0 is cleared. Note that if SI is cleared in the same write that defines the outgoing ACK value, s/w delay is zero.

With the SMBTOE bit set, Timer 3 should be configured to overflow after 25 ms in order to detect SCL low timeouts (see Section “24.3.4. SCL Low Timeout” on page 235). The SMBus interface will force the associated timer to reload while SCL is high, and allow the timer to count when SCL is low. The timer interrupt service routine should be used to reset SMBus communication by disabling and re-enabling the SMBus.

SMBus Free Timeout detection can be enabled by setting the SMBFTE bit. When this bit is set, the bus will be considered free if SDA and SCL remain high for more than 10 SMBus clock source periods (see Figure 24.4).

24.4.2. SMBus Pin Swap

The SMBus peripheral is assigned to pins using the priority crossbar decoder. By default, the SMBus signals are assigned to port pins starting with SDA on the lower-numbered pin, and SCL on the next available pin. The SWAP bit in the SMBTC register can be set to 1 to reverse the order in which the SMBus signals are assigned.

24.4.3. SMBus Timing Control

The SDD field in the SMBTC register is used to restrict the detection of a START condition under certain circumstances. In some systems where there is significant mismatch between the impedance or the capacitance on the SDA and SCL lines, it may be possible for SCL to fall after SDA during an address or data transfer. Such an event can cause a false START detection on the bus. These kind of events are not expected in a standard SMBus or I2C-compliant system. **In most systems this parameter should not be adjusted, and it is recommended that it be left at its default value.**

By default, if the SCL falling edge is detected after the falling edge of SDA (i.e. one SYSCLK cycle or more), the device will detect this as a START condition. The SDD field is used to increase the amount of hold time that is required between SDA and SCL falling before a START is recognized. An additional 2, 4, or 8 SYSCLKs can be added to prevent false START detection in systems where the bus conditions warrant this.

24.4.4. SMB0CN Control Register

SMB0CN is used to control the interface and to provide status information. The higher four bits of SMB0CN (MASTER, TXMODE, STA, and STO) form a status vector that can be used to jump to service routines. MASTER indicates whether a device is the master or slave during the current transfer. TXMODE indicates whether the device is transmitting or receiving data for the current byte.

Table 24.4. Hardware Address Recognition Examples (EHACK = 1)

Hardware Slave Address SLV	Slave Address Mask SLVM	GC bit	Slave Addresses Recognized by Hardware
0x34	0x7E	1	0x34, 0x35, 0x00 (General Call)
0x70	0x73	0	0x70, 0x74, 0x78, 0x7C

24.4.6. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

Register 24.3. SMB0CN: SMBus0 Control

Bit	7	6	5	4	3	2	1	0
Name	MASTER	TXMODE	STA	STO	ACKRQ	ARBLOST	ACK	SI
Type	R	R	RW	RW	R	R	RW	RW
Reset	0	0	0	0	0	0	0	0

SFR Address: 0xC0 (bit-addressable)

Table 24.9. SMB0CN Register Bit Descriptions

Bit	Name	Function
7	MASTER	SMBus0 Master/Slave Indicator. This read-only bit indicates when the SMBus0 is operating as a master. 0: SMBus0 operating in slave mode. 1: SMBus0 operating in master mode.
6	TXMODE	SMBus0 Transmit Mode Indicator. This read-only bit indicates when the SMBus0 is operating as a transmitter. 0: SMBus0 in Receiver Mode. 1: SMBus0 in Transmitter Mode.
5	STA	SMBus0 Start Flag. When reading STA, a 1 indicates that a start or repeated start condition was detected on the bus. Writing a 1 to the STA bit initiates a start or repeated start on the bus.
4	STO	SMBus0 Stop Flag. When reading STO, a 1 indicates that a stop condition was detected on the bus (in slave mode) or is pending (in master mode). When acting as a master, writing a 1 to the STO bit initiates a stop condition on the bus. This bit is cleared by hardware.
3	ACKRQ	SMBus0 Acknowledge Request. 0: No ACK requested. 1: ACK requested.
2	ARBLOST	SMBus0 Arbitration Lost Indicator. 0: No arbitration error. 1: Arbitration error occurred.
1	ACK	SMBus0 Acknowledge. When read as a master, the ACK bit indicates whether an ACK (1) or NACK (0) is received during the most recent byte transfer. As a slave, this bit should be written to send an ACK (1) or NACK (0) to a master request. Note that the logic level of the ACK bit on the SMBus interface is inverted from the logic of the register ACK bit.

25.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 in TCON is set and an interrupt will occur if Timer 0 interrupts are enabled.

The CT0 bit in the TMOD register selects the counter/timer's clock source. When CT0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register. Clearing CT selects the clock defined by the T0M bit in register CKCON. When T0M is set, Timer 0 is clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON.

Setting the TR0 bit enables the timer when either GATE0 in the TMOD register is logic 0 or the input signal $\overline{INT0}$ is active as defined by bit IN0PL in register IT01CF. Setting GATE0 to 1 allows the timer to be controlled by the external input signal $\overline{INT0}$, facilitating pulse width measurements.

TR0	GATE0	$\overline{INT0}$	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled

Note: X = Don't Care

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal $\overline{INT1}$ is used with Timer 1; the $\overline{INT1}$ polarity is defined by bit IN1PL in register IT01CF.

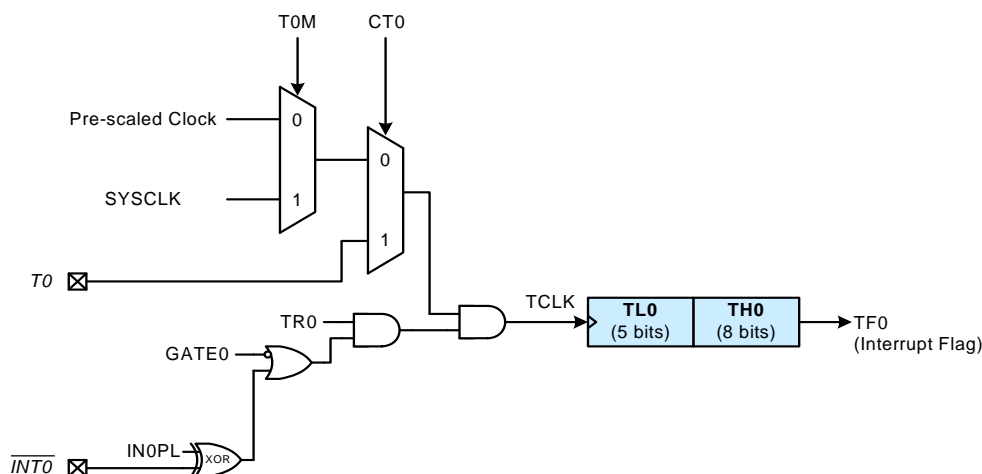


Figure 25.1. T0 Mode 0 Block Diagram

Register 25.7. TH1: Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH1							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x8D								

Table 25.9. TH1 Register Bit Descriptions

Bit	Name	Function
7:0	TH1	Timer 1 High Byte. The TH1 register is the high byte of the 16-bit Timer 1.

Table 25.10. TMR2CN Register Bit Descriptions

Bit	Name	Function
0	T2XCLK	<p>Timer 2 External Clock Select.</p> <p>This bit selects the external clock source for Timer 2. If Timer 2 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 2 Clock Select bits (T2MH and T2ML in register CKCON) may still be used to select between the external clock and the system clock for either timer.</p> <p>0: Timer 2 clock is the system clock divided by 12. 1: Timer 2 clock is the external clock divided by 8 (synchronized with SYSCLK).</p>

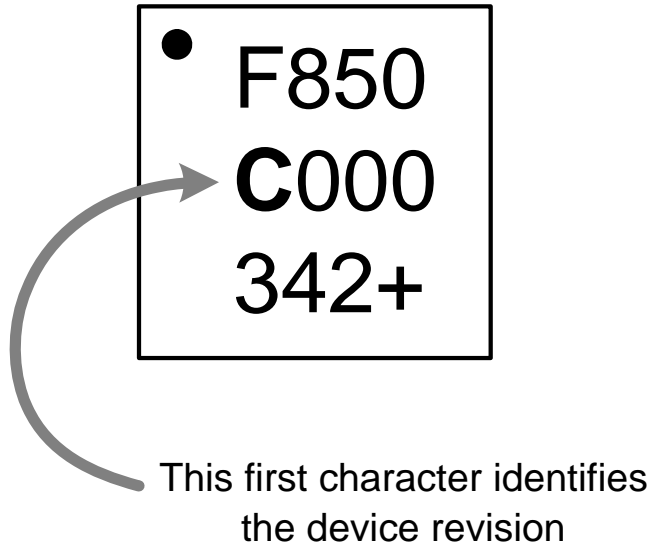


Figure 28.2. QFN-20 Package Revision Marking

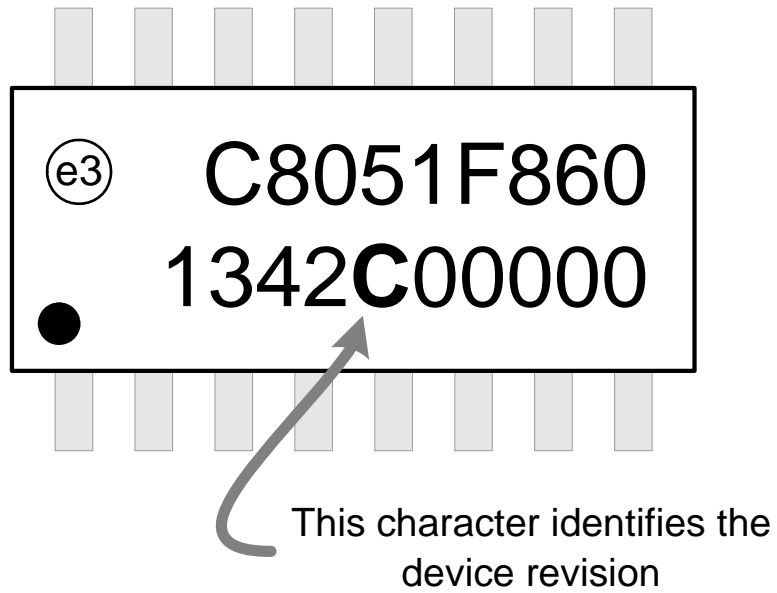


Figure 28.3. SOIC-16 Package Revision Marking

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 0.6

- Updated front page block diagram.
- Updated ADC supply current parameters in Table 1.2, "Power Consumption," on page 8.
- Corrected flash programming voltage range in "Table 1.4. Flash Memory" on page 11.
- Added ADC Power-On Time specification in Table 1.7, "ADC," on page 13.
- Added section "1.2. Typical Performance Curves" on page 19.
- Corrected DERIVID Information in Table 11.3, "DERIVID Register Bit Descriptions," on page 70.
- Updated ADC chapter ("14. Analog-to-Digital Converter (ADC0)" on page 85) and expanded section "14.5. Power Considerations" on page 85 with recommended power configuration settings.
- Updated Figure 21.1, "Port I/O Functional Block Diagram," on page 184.
- Corrected reset value in Register 24.5, "SMB0ADM: SMBus0 Slave Address Mask," on page 257.
- Corrected description of IE0 in "Table 25.4. TCON Register Bit Descriptions" on page 259.

Revision 0.6 to Revision 0.7

- Added mention of the UID to the front page.
- Updated some TBD values in the "1. Electrical Specifications" on page 8 section.
- Updated Power-On Reset (POR) Threshold maximum Falling Voltage on V_{DD} specification in Table 1.3.
- Updated Reset Delay from non-POR source typical specification in Table 1.3.
- Removed V_{DD} Ramp Time maximum specification in Table 1.3.
- Updated Flash Memory Erase Time specification and added Note 2 to Table 1.4.
- Updated maximum ADC DC performance specifications in Table 1.7.
- Updated minimum and maximum ADC offset error and slope error specifications in Table 1.7.
- Updated conditions on Internal Fast Settling Reference Output Voltage (Full Temperature and Supply Range) in Table 1.8.
- Added a new section "1.2.3. Port I/O Output Drive" on page 21.
- Updated pinout Figure 3.1, Figure 3.2, Figure 3.3, Table 3.1, Table 3.2, and Table 3.3 titles to the correct part numbers.
- Updated the Ordering Information ("4. Ordering Information" on page 42.) for Revision C devices.
- Added mention of the unique identifier to "8. Memory Organization" on page 52.
- Added unique identifier information to "11. Device Identification and Unique Identifier" on page 68.
- Updated device part numbers listed in Table 11.3, "DERIVID Register Bit Descriptions," on page 70 to include the revision.
- Added "28. Revision-Specific Behavior" on page 301.

Revision 0.7 to Revision 1.0

- Updated Digital Core, ADC, and Temperature Sensor electrical specifications information for -I devices.
- Updated -I part number information in "4. Ordering Information" on page 42.
- Replaced reference to AMX0P and AMX0N with ADC0MX in Table 21.1, "Port I/O Assignment for Analog Functions," on page 186.
- Added a note to Table 1.13, "Absolute Maximum Ratings," on page 22 and added a link to the Quality and Reliability Monitor Report.
- Added Operating Junction Temperature to Table 1.13, "Absolute Maximum Ratings," on page 22.
- Updated all TBDs in "1. Electrical Specifications" on page 8.