



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	CIP-51™
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f850-c-im

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Parameter	Symbol	Test Condition	Min	Tvp	Max	Unit
ADC0 Rurat Mada, 10 bit ain				400	max	
ale conversions, internal ref-	IADC	$200 \text{ ksps}, \text{ v}_{\text{DD}} = 3.0 \text{ v}$		490		μΑ
erence, Low power bias		100 ksps, V _{DD} = 3.0 V		245		μA
settings		10 ksps, V _{DD} = 3.0 V		23	—	μA
ADC0 Burst Mode, 12-bit sin-	I _{ADC}	100 ksps, V _{DD} = 3.0 V	_	530	—	μA
gle conversions, external ref-		50 ksps, V _{DD} = 3.0 V	_	265	_	μA
		10 ksps, V _{DD} = 3.0 V		53		μA
ADC0 Burst Mode, 12-bit sin- gle conversions, internal ref-	I _{ADC}	100 ksps, V _{DD} = 3.0 V, Normal bias		950	_	μA
erence		50 ksps, V _{DD} = 3.0 V, Low power bias		420	_	μA
		10 ksps, V _{DD} = 3.0 V, Low power bias		85	_	μA
Internal ADC0 Reference,	I _{IREF}	Normal Power Mode	_	680	790	μA
Always-on ⁵		Low Power Mode	_	160	210	μA
Temperature Sensor	I _{TSENSE}		_	75	120	μA
Comparator 0 (CMP0),	I _{CMP}	CPnMD = 11	_	0.5		μA
Comparator 1 (CMP1)		CPnMD = 10	_	3	_	μA
		CPnMD = 01	_	10	_	μA
		CPnMD = 00	_	25	_	μA
Voltage Supply Monitor (VMON0)	I _{VMON}			15	20	μA

Table 1.2. Power Consumption (Continued)

Notes:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.

2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.

3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.

4. ADC0 always-on power excludes internal reference supply current.

5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.



1.4. Absolute Maximum Ratings

Stresses above those listed under Table 1.13 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T _{BIAS}		-55	125	°C
Storage Temperature	T _{STG}		-65	150	°C
Voltage on V _{DD}	V _{DD}		GND-0.3	4.2	V
Voltage on I/O pins or RST	V _{IN}	V _{DD} ≥ 3.3 V	GND-0.3	5.8	V
		V _{DD} < 3.3 V	GND-0.3	V _{DD} +2.5	V
Total Current Sunk into Supply Pin	I _{VDD}			400	mA
Total Current Sourced out of Ground Pin	I _{GND}		400	_	mA
Current Sourced or Sunk by Any I/O Pin or RST	I _{PIO}		-100	100	mA
Operating Junction Temperature	TJ	Commercial Grade Devices (-GM, -GS, -GU)	-40	105	°C
		Industrial Grade Devices (-IM, -IS, -IU)	-40	125	°C
Note: Exposure to maximum ratir	ng condition	ns for extended periods may affe	ect device relia	bility.	. <u>I</u>

Table 1.13. Absolute Maximum Ratings



Pin Name	Туре	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
P0.1	Standard I/O	2	Yes	POMAT.1 INT0.1 INT1.1	ADC0.1 CP0P.1 CP0N.1
P0.2	Standard I/O	1	Yes	POMAT.2 INT0.2 INT1.2	ADC0.2 CP0P.2 CP0N.2
P0.3 / EXTCLK	Standard I/O / External CMOS Clock Input	16	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CP0P.3 CP0N.3
P0.4	Standard I/O	15	Yes	POMAT.4 INT0.4 INT1.4	ADC0.4 CP0P.4 CP0N.4
P0.5	Standard I/O	14	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CP0P.5 CP0N.5
P0.6	Standard I/O	13	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CP1P.0 CP1N.0
P0.7	Standard I/O	12	Yes	POMAT.7 INT0.7 INT1.7	ADC0.7 CP1P.1 CP1N.1
P1.0	Standard I/O	11	Yes	P1MAT.0	ADC0.8 CP1P.2 CP1N.2

Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS



The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory organization of the C8051F85x/ 86x.

Revision C C8051F852/5 and C8051F862/5 devices implement the upper four bytes of internal RAM as a 32-bit Unique Identifier. More information can be found in "Device Identification and Unique Identifier" on page 68.

8.2.1.1. General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word (PSW) register, RS0 and RS1, select the active register bank. This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

8.2.1.2. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination).

The MCS-51[™] assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

MOV C, 22.3h

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

8.2.1.3. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

8.2.2. External RAM

On devices with 512 bytes total RAM, there are 256 bytes of on-chip RAM mapped into the external data memory space. All of these address locations may be accessed using the external move instruction (MOVX) and the data pointer (DPTR), or using MOVX indirect addressing mode. Note: The 16-bit MOVX instruction is also used for writes to the flash memory. See Section "10. Flash Memory" on page 61 for details. The MOVX instruction accesses XRAM by default.

For a 16-bit MOVX operation (@DPTR), the upper 8 bits of the 16-bit external data memory address word are "don't cares". As a result, addresses 0x0000 through 0x00FF are mapped modulo style over the entire 64 k external data memory address range. For example, the XRAM byte at address 0x0000 is shadowed at addresses 0x0100, 0x0200, 0x0300, 0x0400, etc.

Revision C C8051F850/1/3/4 and C8051F860/1/3/4 devices implement the upper four bytes of external RAM as a 32-bit Unique Identifier. More information can be found in "Device Identification and Unique Identifier" on page 68.



Register 11.3. REVID: Revision Identifcation

Bit	7	6	5	4	3	2	1	0		
Name	REVID									
Туре	R									
Reset	Х	Х	Х	Х	Х	Х	Х	Х		
SFR Add	SFR Address: 0xB6									

Table 11.4. REVID Register Bit Descriptions

Bit	Name	Function
7:0	REVID	Revision ID.
		This read-only register returns the 8-bit revision ID. 00000000: Revision A 00000001: Revision B 00000010: Revision C 00000011-11111111: Reserved.



12. Interrupts

The C8051F85x/86x includes an extended interrupt system supporting multiple interrupt sources with two priority levels. The allocation of interrupt sources between on-chip peripherals and external input pins varies according to the specific version of the device. Each interrupt source has one or more associated interrupt-pending flag(s) located in an SFR. When a peripheral or external source meets a valid interrupt condition, the associated interrupt-pending flag is set to logic 1.

If interrupts are enabled for the source, an interrupt request is generated when the interrupt-pending flag is set. As soon as execution of the current instruction is complete, the CPU generates an LCALL to a predetermined address to begin execution of an interrupt service routine (ISR). Each ISR must end with an RETI instruction, which returns program execution to the next instruction that would have been executed if the interrupt request had not occurred. If interrupts are not enabled, the interrupt-pending flag is ignored by the hardware and program execution continues as normal. The interrupt-pending flag is set to logic 1 regardless of the interrupt's enable/disable state.

Each interrupt source can be individually enabled or disabled through the use of an associated interrupt enable bit in an SFR (IE and EIE1). However, interrupts must first be globally enabled by setting the EA bit in the IE register to logic 1 before the individual interrupt enables are recognized. Setting the EA bit to logic 0 disables all interrupt sources regardless of the individual interrupt-enable settings.

Some interrupt-pending flags are automatically cleared by the hardware when the CPU vectors to the ISR. However, most are not cleared by the hardware and must be cleared by software before returning from the ISR. If an interrupt-pending flag remains set after the CPU completes the return-from-interrupt (RETI) instruction, a new interrupt request will be generated immediately and the CPU will re-enter the ISR after the completion of the next instruction.

12.1. MCU Interrupt Sources and Vectors

The C8051F85x/86x MCUs support interrupt sources for each peripheral on the device. Software can simulate an interrupt by setting any interrupt-pending flag to logic 1. If interrupts are enabled for the flag, an interrupt request will be generated and the CPU will vector to the ISR address associated with the interrupt-pending flag. MCU interrupt sources, associated vector addresses, priority order and control bits are summarized in Table 12.1. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

12.1.1. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. Each interrupt has an associated interrupt priority bit in an SFR (IP or EIP1) used to configure its priority level. Low priority is the default. If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate, given in Table 12.1.

12.1.2. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock



13. Power Management and Internal Regulator

All internal circuitry on the C8051F85x/86x devices draws power from the VDD supply pin. Circuits with external connections (I/O pins, analog muxes) are powered directly from the VDD supply voltage, while most of the internal circuitry is supplied by an on-chip LDO regulator. The regulator output is fully internal to the device, and is available also as an ADC input or reference source for the comparators and ADC.

The devices support the standard 8051 power modes: idle and stop. For further power savings in stop mode, the internal LDO regulator may be disabled, shutting down the majority of the power nets on the device.

Although the C8051F85x/86x has idle and stop modes available, more control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

13.1. Power Modes

Idle mode halts the CPU while leaving the peripherals and clocks active. In stop mode, the CPU is halted, all interrupts and timers are inactive, and the internal oscillator is stopped (analog peripherals remain in their selected states; the external oscillator is not affected). Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode consumes the least power because the majority of the device is shut down with no clocks active. The Power Control Register (PCON) is used to control the C8051F85x/86x's Stop and Idle power management modes.

13.1.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the hardware to halt the CPU and enter idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

Note: If the instruction following the write of the IDLE bit is a single-byte instruction and an interrupt occurs during the execution phase of the instruction that sets the IDLE bit, the CPU may not wake from Idle mode when a future interrupt occurs. Therefore, instructions that set the IDLE bit should be followed by an instruction that has two or more opcode bytes, for example:

// 111	
PCON $ = 0 \times 01;$	// set IDLE bit
PCON = PCON;	// followed by a 3-cycle dummy instruction
; in assembly:	
ORL PCON, #01h	; set IDLE bit
MOV PCON, PCON	; followed by a 3-cycle dummy instruction

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system.



14.8. Voltage and Ground Reference Options

The voltage reference multiplexer is configurable to use an externally connected voltage reference, the internal voltage reference, or one of two power supply voltages. The ground reference mux allows the ground reference for ADC0 to be selected between the ground pin (GND) or a port pin dedicated to analog ground (AGND).

The voltage and ground reference options are configured using the REF0CN register.

Important Note About the VREF and AGND Inputs: Port pins are used as the external VREF and AGND inputs. When using an external voltage reference, VREF should be configured as an analog input and skipped by the digital crossbar. When using AGND as the ground reference to ADC0, AGND should be configured as an analog input and skipped by the Digital Crossbar.

14.8.1. External Voltage Reference

To use an external voltage reference, REFSL should be set to 00. Bypass capacitors should be added as recommended by the manufacturer of the external voltage reference. If the manufacturer does not provide recommendations, a 4.7uF in parallel with a 0.1uF capacitor is recommended.

14.8.2. Internal Voltage Reference

For applications requiring the maximum number of port I/O pins, or very short VREF turn-on time, the highspeed reference will be the best internal reference option to choose. The internal reference is selected by setting REFSL to 11. When selected, the internal reference will be automatically enabled/disabled on an as-needed basis by the ADC. The reference can be set to one of two voltage values: 1.65 V or 2.4 V, depending on the value of the IREFLVL bit.

For applications with a non-varying power supply voltage, using the power supply as the voltage reference can provide the ADC with added dynamic range at the cost of reduced power supply noise rejection. To use the external supply pin (VDD) or the 1.8 V regulated digital supply voltage as the reference source, REFSL should be set to 01 or 10, respectively.

Internal reference sources are not routed to the VREF pin, and do not require external capacitors. The electrical specifications tables detail SAR clock and throughput limitations for each reference source.

14.8.3. Analog Ground Reference

To prevent ground noise generated by switching digital logic from affecting sensitive analog measurements, a separate analog ground reference option is available. When enabled, the ground reference for the ADC during both the tracking/sampling and the conversion periods is taken from the AGND pin. Any external sensors sampled by the ADC should be referenced to the AGND pin. If an external voltage reference is used, the AGND pin should be connected to the ground of the external reference and its associated decoupling capacitor. The separate analog ground reference option is enabled by setting GNDSL to 1. Note that when sampling the internal temperature sensor, the internal chip ground is always used for the sampling operation, regardless of the setting of the GNDSL bit. Similarly, whenever the internal 1.65 V high-speed reference is selected, the internal chip ground is always used during the conversion period, regardless of the setting of the GNDSL bit.



Register 14.6. ADC0TK: ADC0 Burst Mode Track Time

Bit	7	6	5	4	3	2	1	0		
Name	AD12SM	Reserved		ADTK						
Туре	RW	RW		RW						
Reset	0	0	0	1	1	1	1	0		
SFR Address: 0xB9										

Table 14.9. ADC0TK Register Bit Descriptions

Bit	Name	Function
7	AD12SM	12-Bit Sampling Mode.
		This bit controls the way that the ADC samples the input when in 12-bit mode. When the ADC is configured for multiple 12-bit conversions in burst mode, the AD12SM bit should be cleared to 0.
		0: The ADC will re-track and sample the input four times during a 12-bit conversion.
		1: The ADC will sample the input once at the beginning of each 12-bit conversion. The ADTK field can be set to 63 to maximize throughput.
6	Reserved	Must write reset value.
5:0	ADTK	Burst Mode Tracking Time.
		This field sets the time delay between consecutive conversions performed in Burst Mode. When ADTM is set, an additional 4 SARCLKs are added to this time.
		$T_{BMTK} = \frac{64 - ADTK}{F_{HFOSC}}$
		The Burst Mode track delay is not inserted prior to the first conversion. The required tracking time for the first conversion should be defined with the ADPWR field.



Number of Instructions	26	50	5	14	7	3	1	2	1

15.2. Programming and Debugging Support

In-system programming of the flash program memory and communication with on-chip debug support logic is accomplished via the Silicon Labs 2-Wire Development Interface (C2).

The on-chip debug support logic facilitates full speed in-circuit debugging, allowing the setting of hardware breakpoints, starting, stopping and single stepping through program execution (including interrupt service routines), examination of the program's call stack, and reading/writing the contents of registers and memory. This method of on-chip debugging is completely non-intrusive, requiring no RAM, Stack, timers, or other on-chip resources.

The CIP-51 is supported by development tools from Silicon Labs and third party vendors. Silicon Labs provides an integrated development environment (IDE) including editor, debugger and programmer. The IDE's debugger and programmer interface to the CIP-51 via the C2 interface to provide fast and efficient in-system device programming and debugging. Third party macro assemblers and C compilers are also available.

15.3. Instruction Set

The instruction set of the CIP-51 System Controller is fully compatible with the standard MCS-51[™] instruction set. Standard 8051 development tools can be used to develop software for the CIP-51. All CIP-51 instructions are the binary and functional equivalent of their MCS-51[™] counterparts, including opcodes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051.

15.3.1. Instruction and CPU Timing

In many 8051 implementations, a distinction is made between machine cycles and clock cycles, with machine cycles varying from 2 to 12 clock cycles in length. However, the CIP-51 implementation is based solely on clock cycle timing. All instruction timings are specified in terms of clock cycles.

Due to the pipelined architecture of the CIP-51, most instructions execute in the same number of clock cycles as there are program bytes in the instruction. Conditional branch instructions take one less clock cycle to complete when the branch is not taken as opposed to when the branch is taken. Table 15.1 is the CIP-51 Instruction Set Summary, which includes the mnemonic, number of bytes, and number of clock cycles for each instruction.



Rev. 1.0

Mnemonic	Description	Bytes	Clock Cycles
ADD A, Rn	Add register to A	1	1
ADD A, direct	Add direct byte to A	2	2
ADD A, @Ri	Add indirect RAM to A	1	2
ADD A, #data	Add immediate to A	2	2
ADDC A, Rn	Add register to A with carry	1	1
ADDC A, direct	Add direct byte to A with carry	2	2
ADDC A, @Ri	Add indirect RAM to A with carry	1	2
ADDC A, #data	Add immediate to A with carry	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	1	2
SUBB A, #data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	2
INC @Ri	Increment indirect RAM	1	2
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	2
DEC @Ri	Decrement indirect RAM	1	2
INC DPTR	Increment Data Pointer	1	1
MUL AB	Multiply A and B	1	4
DIV AB	Divide A by B	1	8
DA A	Decimal adjust A	1	1
	Logical Operations		
ANL A, Rn	AND Register to A	1	1
ANL A, direct	AND direct byte to A	2	2
ANL A, @Ri	AND indirect RAM to A	1	2
ANL A, #data	AND immediate to A	2	2
ANL direct, A	AND A to direct byte	2	2
ANL direct, #data	AND immediate to direct byte	3	3
ORL A, Rn	OR Register to A	1	1
ORL A, direct	OR direct byte to A	2	2
ORL A, @Ri	OR indirect RAM to A	1	2
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	2
ORL direct, #data	OR immediate to direct byte	3	3

Table 15.1. CIP-51 Instruction Set Summary



Register 15.5. B: B Register

Bit	7	6	5	4	3	2	1	0		
Name	B									
Туре		RW								
Reset	0	0	0	0	0	0	0	0		
SFR Add	SFR Address: 0xF0 (bit-addressable)									

Table 15.6. B Register Bit Descriptions

Bit	Name	Function			
7:0	В	B Register.			
		his register serves as a second accumulator for certain arithmetic operations.			



16.3. External Clock

An external CMOS clock source is also supported by the C8051F85x/86x family. The EXTCLK pin on the device serves as the external clock input when running in this mode. The EXTCLK input may also be used to clock some of the digital peripherals (e.g., Timers, PCA, etc.) while SYSCLK runs from one of the internal oscillator sources. When not selected as the SYSCLK source, the EXTCLK input is always resynchronized to SYSCLK.

16.4. Clock Selection

The CLKSEL register is used to select the clock source for the system. The CLKSL field selects which oscillator source is used as the system clock, while CLKDIV controls the programmable divider. CLKSL must be set to 01b for the system clock to run from the external oscillator; however the external oscillator may still clock certain peripherals (timers, PCA) when the internal oscillator is selected as the system clock. In these cases, the external oscillator source is synchronized to the SYSCLK source. The system clock may be switched on-the-fly between any of the oscillator sources so long as the selected clock source is enabled and has settled, and CLKDIV may be changed at any time.

The internal high-frequency and low-frequency oscillators require little start-up time and may be selected as the system clock immediately following the register write which enables the oscillator. When selecting the EXTCLK pin as a clock input source, the pin should be skipped in the crossbar and configured as a digital input. Firmware should ensure that the external clock source is present or enable the missing clock detector before switching the CLKSL field.



17. Comparators (CMP0 and CMP1)

C8051F85x/86x devices include two on-chip programmable voltage comparators, CMP0 and CMP1. The two comparators are functionally identical, but have different connectivity within the device. A functional block diagram is shown in Figure 17.1.





17.1. System Connectivity

Comparator inputs are routed to port I/O pins or internal signals using the comparator mux registers. The comparator's synchronous and asynchronous outputs can optionally be routed to port I/O pins through the port I/O crossbar. The output of either comparator may also be configured to generate a system interrupt. CMP0 may also be used as a reset source, or as a trigger to kill a PCA output channel.

The CMP0 inputs are selected in the CPT0MX register, while CPT1MX selects the CMP1 inputs. The CMXP field selects the comparator's positive input (CPnP.x); the CMXN field selects the comparator's negative input (CPnN.x). Table 17.1 through Table 17.4 detail the comparator input multiplexer options on the C8051F85x/86x family. See the port I/O crossbar sections for details on configuring comparator outputs via the digital crossbar. Comparator inputs can be externally driven from -0.25 V to (V_{DD}) + 0.25 V without damage or upset.

Important Note About Comparator Inputs: The port pins selected as comparator inputs should be configured as analog inputs in their associated port configuration register, and configured to be skipped by the crossbar.



18.6. CRC Control Registers

Register 18.1. CRC0CN: CRC0 Control

Bit	7	6	5	4	3	2	1	0
Name		Rese	erved		CRCINIT	CRCVAL	Reserved	CRCPNT
Туре		F	२		RW	RW	R	RW
Reset	0	0	0	0	0	0	0	
SFR Address: 0xCE								

Table 18.2. CRC0CN Register Bit Descriptions

Bit	Name	Function					
7:4	Reserved	Must write reset value.					
3	CRCINIT	CRC Result Initialization Bit.					
		Writing a 1 to this bit initializes the entire CRC result based on CRCVAL.					
2	CRCVAL	CRC Set Value Initialization Bit.					
		This bit selects the set value of the CRC result.					
		0: CRC result is set to 0x0000 on write of 1 to CRCINIT.					
		1: CRC result is set to 0xFFFF on write of 1 to CRCINIT.					
1	Reserved	Must write reset value.					
0	CRCPNT	CRC Result Pointer.					
		Specifies the byte of the CRC result to be read/written on the next access to CRC0DA					
		This bit will automatically toggle upon each read or write.					
		0: CRC0DAT accesses bits 7-0 of the 16-bit CRC result.					
	1: CRC0DAT accesses bits 15-8 of the 16-bit CRC result.						
Note:	ote: Upon initiation of an automatic CRC calculation, the three cycles following a write to CRC0CN that initiate a CRC						
	operation must only contain instructions which execute in the same number of cycles as the number of bytes in the						
	instruction. An example of such an instruction is a 3-byte MOV that targets the CRC0FLIP register. When programming						
	byte MOV instruction.						



Register 20.3. PCA0PWM: PCA PWM Configuration

Bit	7	6	5	4	3	2	1	0		
Name	ARSEL	ECOV	COVF	Rese	erved	CLSEL				
Туре	RW	RW	RW	F	२	RW				
Reset	0	0	0	0	0	0 0 0				
SFR Address: 0xF7										

Table 20.5. PCA0PWM Register Bit Descriptions

Bit	Name	Function
7	ARSEL	Auto-Reload Register Select.
		This bit selects whether to read and write the normal PCA capture/compare registers (PCA0CPn), or the Auto-Reload registers at the same SFR addresses. This function is used to define the reload value for 9 to 11-bit PWM modes. In all other modes, the Auto-Reload registers have no function. 0: Read/Write Capture/Compare Registers at PCA0CPHn and PCA0CPLn. 1: Read/Write Auto-Reload Registers at PCA0CPHn and PCA0CPLn.
6	ECOV	Cycle Overflow Interrupt Enable.
		This bit sets the masking of the Cycle Overflow Flag (COVF) interrupt.
		0: COVF will not generate PCA interrupts.
5		Cycle Overfley: Fler
5	COVF	This bit indicates an overflow of the 8th to 11th bit of the main PCA counter (PCA0). The specific bit used for this flag depends on the setting of the Cycle Length Select bits. The bit can be set by hardware or software, but must be cleared by software. 0: No overflow has occurred since the last time this bit was cleared. 1: An overflow has occurred since the last time this bit was cleared.
4:3	Reserved	Must write reset value.
2:0	CLSEL	Cycle Length Select.
		 When 16-bit PWM mode is not selected, these bits select the length of the PWM cycle. This affects all channels configured for PWM which are not using 16-bit PWM mode. These bits are ignored for individual channels configured to16-bit PWM mode. 000: 8 bits. 001: 9 bits. 010: 10 bits. 011: 11 bits. 100-111: Reserved.



22.1. Power-On Reset

During power-up, the POR circuit will fire. When POR fires, the device is held in a reset state and the \overline{RST} pin is driven low until V_{DD} settles above V_{RST}. Two delays are present during the supply ramp time. First, a delay will occur before the POR circuitry fires and pulls the \overline{RST} pin low. A second delay occurs before the device is released from reset; the delay decreases as the V_{DD} ramp time increases (V_{DD} ramp time is defined as how fast V_{DD} ramps from 0 V to V_{RST}). Figure 22.2. plots the power-on reset timing. For ramp times less than 1 ms, the power-on reset time (T_{POR}) is typically less than 0.3 ms. Additionally, the power supply must reach V_{RST} before the POR circuit will release the device from reset.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. When PORSF is set, all of the other reset flags in the RSTSRC Register are indeterminate (PORSF is cleared by all other resets). Since all resets cause program execution to begin at the same location (0x0000) software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset. The V_{DD} monitor is enabled following a power-on reset.



Figure 22.2. Power-on Reset Timing







23.6. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following figures.



	Valı	Jes	Rea	d				ues Vrit	;to e	tus ected	
Mode	Status Vector	ACKRQ	ARBLOST	ACK	Current SMbus State	STA	STO	ACK	Next Sta Vector Exp		
-		0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	Х	0001	
smitte	0100	0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	Х	0100	
⁄e Tran		0	1	x	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	Х	0001	
Slav	0101 0 X X An illegal STOP or bus error was detected while a Slave Transmission C was in progress.		An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	Х				
Γ						If Write, Acknowledge received address	0	0	1	0000	
		1	0	x	A slave address + R/W was received; ACK requested.	If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100	
						NACK received address.	0	0	0	—	
	0010					If Write, Acknowledge received address	0	0	1	0000	
iver		1	1	x	Lost arbitration as master; slave address + R/W received; ACK	If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100	
kece					requested.	NACK received address.	0	0	0	—	
slave F						Reschedule failed transfer; NACK received address.	1	0	0	1110	
0,	0001	0	0	x	A STOP was detected while addressed as a Slave Transmitter or Slave Receiver.	Clear STO.	0	0	X		
		1	1	x	Lost arbitration while attempting a STOP.	No action required (transfer complete/aborted).	0	0	0		
	0000	1	0	x	A slave byte was received; ACK	Acknowledge received byte; Read SMB0DAT.	0	0	1	0000	
						requested.	NACK received byte.	0	0	0	

Table 24.5. SMBus Status Decoding: Hardware ACK Disabled (EHACK = 0) (Continued)



25. Timers (Timer0, Timer1, Timer2 and Timer3)

Each MCU in the C8051F85x/86x family includes four counter/timers: two are 16-bit counter/timers compatible with those found in the standard 8051, and two are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 and Timer 3 are also identical and offer both 16-bit and split 8-bit timer functionality with auto-reload capabilities. Timer 2 and Timer 3 both offer a capture function, but are different in their system-level connections. Timer 2 is capable of performing a capture function on an external signal input routed through the crossbar, while the Timer 3 capture is dedicated to the low-frequency oscillator output. Table 25.1 summarizes the modes available to each timer.

Timer 0 and Timer 1 Modes	Timer 2 Modes	Timer 3 Modes
13-bit counter/timer	16-bit timer with auto-reload	16-bit timer with auto-reload
16-bit counter/timer	Two 8-bit timers with auto-reload	Two 8-bit timers with auto-reload
8-bit counter/timer with auto-reload	Input pin capture	Low-frequency oscillator capture
Two 8-bit counter/timers (Timer 0 only)		

Table 25.1. Timer Modes

Timers 0 and 1 may be clocked by one of five sources, determined by the Timer Mode Select bits (T1M–T0M) and the Clock Scale bits (SCA1–SCA0). The Clock Scale bits define a pre-scaled clock from which Timer 0 and/or Timer 1 may be clocked.

Timer 0/1 may then be configured to use this pre-scaled clock signal or the system clock. Timer 2 and Timer 3 may be clocked by the system clock, the system clock divided by 12, or the external oscillator clock source divided by 8.

Timer 0 and Timer 1 may also be operated as counters. When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin (T0 or T1). Events with a frequency of up to one-fourth the system clock frequency can be counted. The input signal need not be periodic, but it must be held at a given level for at least two full system clock cycles to ensure the level is properly sampled.

All four timers are capable of clocking other peripherals and triggering events in the system. The individual peripherals select which timer to use for their respective functions. Table 25.2 summarizes the peripheral connections for each timer. Note that the Timer 2 and Timer 3 high overflows apply to the full timer when operating in 16-bit mode or the high-byte timer when operating in 8-bit split mode.

Function	T0 Overflow	T1 Overflow	T2 High Overflow	T2 Low Overflow	T3 High Overflow	T3 Low Overflow
UART0 Baud Rate		Х				
SMBus0 Clock Rate	Х	Х	Х	Х		
SMBus0 SCL Low Timeout					Х	
PCA0 Clock	Х					

