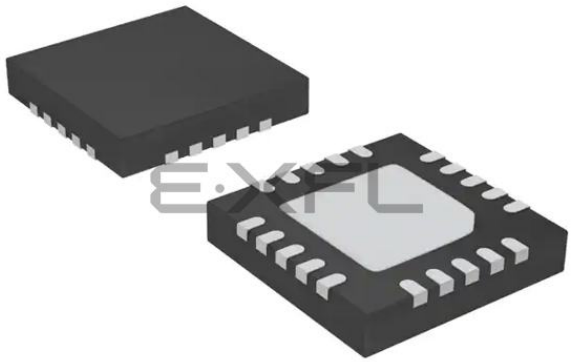

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51™
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f850-c-imr

Table 1.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	490	—	µA
		100 ksps, V_{DD} = 3.0 V	—	245	—	µA
		10 ksps, V_{DD} = 3.0 V	—	23	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	530	—	µA
		50 ksps, V_{DD} = 3.0 V	—	265	—	µA
		10 ksps, V_{DD} = 3.0 V	—	53	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	950	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	420	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	85	—	µA
Internal ADC0 Reference, Always-on[5]	I_{IREF}	Normal Power Mode	—	680	790	µA
		Low Power Mode	—	160	210	µA
Temperature Sensor	I_{TSENSE}		—	75	120	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CPnMD = 11	—	0.5	—	µA
		CPnMD = 10	—	3	—	µA
		CPnMD = 01	—	10	—	µA
		CPnMD = 00	—	25	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	µA

Notes:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

Table 1.8. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, $V_{DD} \geq 2.6$ V	2.35	2.4	2.45	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 800 ksps; VREF = 3.0 V	—	5	—	µA

Table 1.9. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	757	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	17	—	mV
Slope	M		—	2.85	—	mV/°C
Slope Error*	E_M		—	70	—	µV/°C
Linearity			—	0.5	—	°C
Turn-on Time			—	1.8	—	µs
***Note:** Represents one standard deviation from the mean.						

Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
P1.1	Standard I/O	10	Yes	P1MAT.1	ADC0.9 CP1P.3 CP1N.3
P1.2	Standard I/O	9	Yes	P1MAT.2	ADC0.10 CP1P.4 CP1N.4
P1.3	Standard I/O	8	Yes	P1MAT.3	ADC0.11 CP1P.5 CP1N.5
P2.0 / C2D	Standard I/O / C2 Debug Data	7			

4. Ordering Information

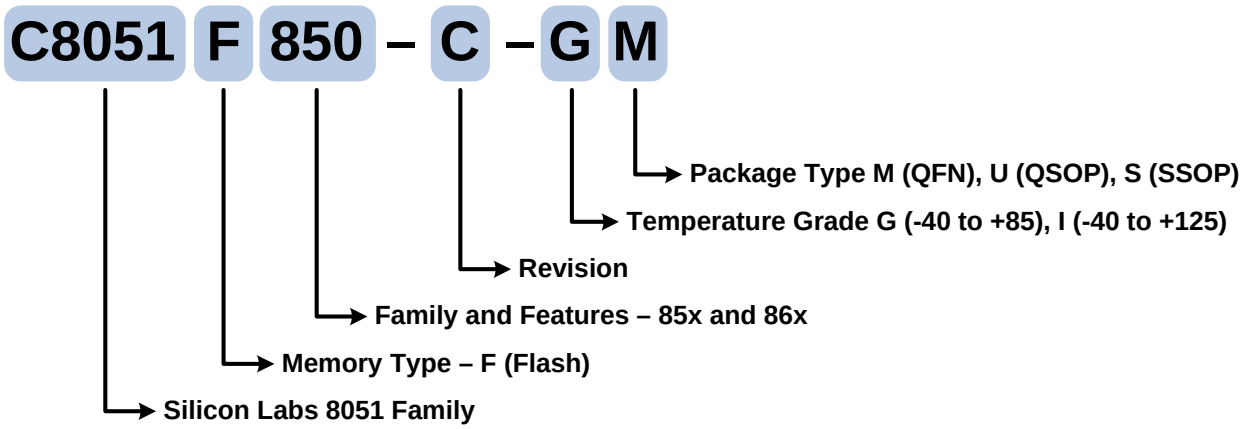


Figure 4.1. C8051F85x/86x Part Numbering

All C8051F85x/86x family members have the following features:

- CIP-51 Core running up to 25 MHz
- Two Internal Oscillators (24.5 MHz and 80 kHz)
- I2C/SMBus
- SPI
- UART
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 16-bit CRC Unit

In addition to these features, each part number in the C8051F85x/86x family has a set of features that vary across the product line. The product selection guide in Table 4.1 shows the features available on each family member.

All devices in Table 4.1 are also available in an industrial version. For the industrial version, the -G in the ordering part number is replaced with -I. For example, the industrial version of the C8051F850-C-GM is the C8051F850-C-IM.

Table 6.2. QFN-20 Landing Diagram Dimensions

Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
D	2.71 REF		GE	2.10	—
D2	1.60	1.80	W	—	0.34
e	0.50 BSC		X	—	0.28
E	2.71 REF		Y	0.61 REF	
E2	1.60	1.80	ZE	—	3.31
f	2.53 BSC		ZD	—	3.31
GD	2.10	—			

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 9.2. Special Function Registers (Continued)

Register	Address	Register Description	Page
ADC0L	0xBD	ADC0 Data Word Low Byte	106
ADC0LTH	0xC6	ADC0 Less-Than High Byte	109
ADC0LTL	0xC5	ADC0 Less-Than Low Byte	110
ADC0MX	0xBB	ADC0 Multiplexer Selection	111
ADC0PWR	0xDF	ADC0 Power Control	103
ADC0TK	0xB9	ADC0 Burst Mode Track Time	104
B	0xF0	B Register	123
CKCON	0x8E	Clock Control	269
CLKSEL	0xA9	Clock Selection	129
CPT0CN	0x9B	Comparator 0 Control	134
CPT0MD	0x9D	Comparator 0 Mode	135
CPT0MX	0x9F	Comparator 0 Multiplexer Selection	136
CPT1CN	0xBF	Comparator 1 Control	137
CPT1MD	0xAB	Comparator 1 Mode	138
CPT1MX	0xAA	Comparator 1 Multiplexer Selection	139
CRC0AUTO	0xD2	CRC0 Automatic Control	146
CRC0CN	0xCE	CRC0 Control	143
CRC0CNT	0xD3	CRC0 Automatic Flash Sector Count	147
CRC0DAT	0xDE	CRC0 Data Output	145
CRC0FLIP	0xCF	CRC0 Bit Flip	148
CRC0IN	0xDD	CRC0 Data Input	144
DERIVID	0xAD	Derivative Identification	70
DEVICEID	0xB5	Device Identification	69
DPH	0x83	Data Pointer Low	120
DPL	0x82	Data Pointer High	119
EIE1	0xE6	Extended Interrupt Enable 1	78
EIP1	0xF3	Extended Interrupt Priority 1	80
FLKEY	0xB7	Flash Lock and Key	67

Register 11.3. REVID: Revision Identifcation

Bit	7	6	5	4	3	2	1	0
Name	REVID							
Type	R							
Reset	X	X	X	X	X	X	X	X
SFR Address: 0xB6								

Table 11.4. REVID Register Bit Descriptions

Bit	Name	Function
7:0	REVID	**Revision ID.** This read-only register returns the 8-bit revision ID. 00000000: Revision A 00000001: Revision B 00000010: Revision C 00000011-11111111: Reserved.

Register 12.3. EIE1: Extended Interrupt Enable 1

Bit	7	6	5	4	3	2	1	0
Name	ET3	ECP1	ECP0	EPCA0	EADC0	EWADC0	EMAT	ESMB0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xE6								

Table 12.4. EIE1 Register Bit Descriptions

Bit	Name	Function
7	ET3	**Enable Timer 3 Interrupt.** This bit sets the masking of the Timer 3 interrupt. 0: Disable Timer 3 interrupts. 1: Enable interrupt requests generated by the TF3L or TF3H flags.
6	ECP1	**Enable Comparator1 (CP1) Interrupt.** This bit sets the masking of the CP1 interrupt. 0: Disable CP1 interrupts. 1: Enable interrupt requests generated by the comparator 1 CPRIF or CPFIF flags.
5	ECP0	**Enable Comparator0 (CP0) Interrupt.** This bit sets the masking of the CP0 interrupt. 0: Disable CP0 interrupts. 1: Enable interrupt requests generated by the comparator 0 CPRIF or CPFIF flags.
4	EPCA0	**Enable Programmable Counter Array (PCA0) Interrupt.** This bit sets the masking of the PCA0 interrupts. 0: Disable all PCA0 interrupts. 1: Enable interrupt requests generated by PCA0.
3	EADC0	**Enable ADC0 Conversion Complete Interrupt.** This bit sets the masking of the ADC0 Conversion Complete interrupt. 0: Disable ADC0 Conversion Complete interrupt. 1: Enable interrupt requests generated by the ADINT flag.
2	EWADC0	**Enable Window Comparison ADC0 Interrupt.** This bit sets the masking of ADC0 Window Comparison interrupt. 0: Disable ADC0 Window Comparison interrupt. 1: Enable interrupt requests generated by ADC0 Window Compare flag (ADWINT).
1	EMAT	**Enable Port Match Interrupts.** This bit sets the masking of the Port Match Event interrupt. 0: Disable all Port Match interrupts. 1: Enable interrupt requests generated by a Port Match.

14.1. ADC0 Analog Multiplexer

ADC0 on C8051F85x/86x has an analog multiplexer capable of selecting any pin on ports P0 and P1 (up to 16 total), the on-chip temperature sensor, the internal regulated supply, the VDD supply, or GND. ADC0 input channels are selected using the ADC0MX register.

Table 14.1. ADC0 Input Multiplexer Channels

ADC0MX setting	Signal Name	QSOP24 Pin Name	QFN20 Pin Name	SOIC16 Pin Name
00000	ADC0.0	P0.0	P0.0	P0.0
00001	ADC0.1	P0.1	P0.1	P0.1
00010	ADC0.2	P0.2	P0.2	P0.2
00011	ADC0.3	P0.3	P0.3	P0.3
00100	ADC0.4	P0.4	P0.4	P0.4
00101	ADC0.5	P0.5	P0.5	P0.5
00110	ADC0.6	P0.6	P0.6	P0.6
00111	ADC0.7	P0.7	P0.7	P0.7
01000	ADC0.8	P1.0	P1.0	P1.0
01001	ADC0.9	P1.1	P1.1	P1.1
01010	ADC0.10	P1.2	P1.2	P1.2
01011	ADC0.11	P1.3	P1.3	P1.3
01100	ADC0.12	P1.4	P1.4	Reserved
01101	ADC0.13	P1.5	P1.5	Reserved
01110	ADC0.14	P1.6	P1.6	Reserved
01111	ADC0.15	P1.7	Reserved	Reserved
10000	Temp Sensor	Internal Temperature Sensor		
10001	LDO	Internal 1.8 V LDO Output		
10010	VDD	VDD Supply Pin		
10011	GND	GND Supply Pin		
10100-11111	None	No connection		

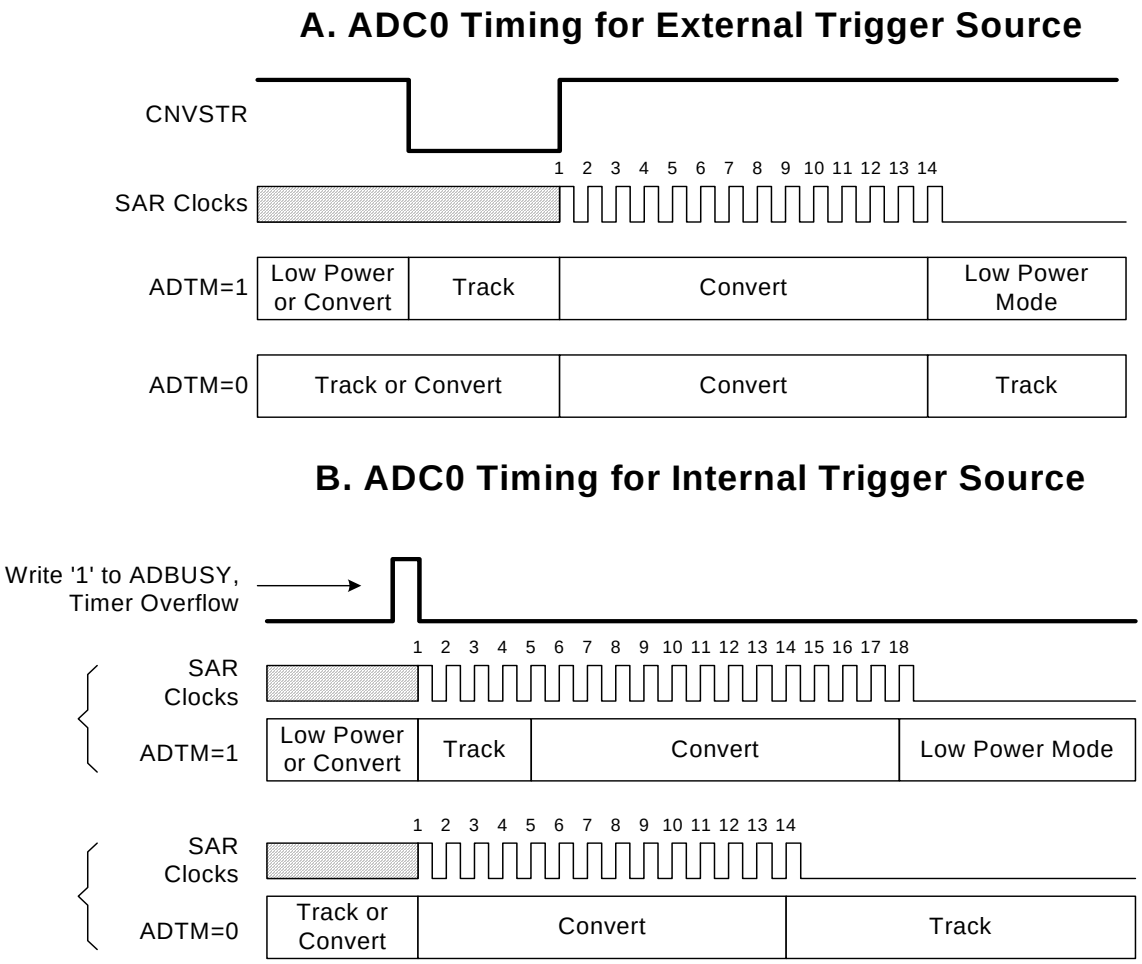


Figure 14.2. 10-Bit ADC Track and Conversion Example Timing (ADBMEN = 0)

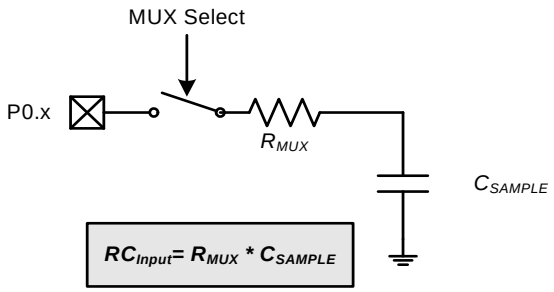
14.2.3. Burst Mode

Burst Mode is a power saving feature that allows ADC0 to remain in a low power state between conversions. When Burst Mode is enabled, ADC0 wakes from a low power state, accumulates 1, 4, 8, 16, 32, or 64 samples using the internal low-power high-frequency oscillator, then re-enters a low power state. Since the Burst Mode clock is independent of the system clock, ADC0 can perform multiple conversions then enter a low power state within a single system clock cycle, even if the system clock is slow (e.g. 80 kHz).

Burst Mode is enabled by setting ADBMEN to logic 1. When in Burst Mode, ADEN controls the ADC0 idle power state (i.e. the state ADC0 enters when not tracking or performing conversions). If ADEN is set to logic 0, ADC0 is powered down after each burst. If ADEN is set to logic 1, ADC0 remains enabled after each burst. On each convert start signal, ADC0 is awakened from its Idle Power State. If ADC0 is powered down, it will automatically power up and wait the programmable Power-Up Time controlled by the ADPWR bits. Otherwise, ADC0 will start tracking and converting immediately. Figure 14.3 shows an example of Burst Mode Operation with a slow system clock and a repeat count of 4.

When Burst Mode is enabled, a single convert start will initiate a number of conversions equal to the repeat count. When Burst Mode is disabled, a convert start is required to initiate each conversion. In both modes, the ADC0 End of Conversion Interrupt Flag (ADINT) will be set after “repeat count” conversions have been accumulated. Similarly, the Window Comparator will not compare the result to the greater-than and less-than registers until “repeat count” conversions have been accumulated.

n is the ADC resolution in bits (8/10/12).



Note: The value of CSAMPLE depends on the PGA Gain. See electrical specifications for details.

Figure 14.4. ADC0 Equivalent Input Circuits

14.2.5. Gain Setting

The ADC has gain settings of 1x and 0.5x. In 1x mode, the full scale reading of the ADC is determined directly by VREF. In 0.5x mode, the full-scale reading of the ADC occurs when the input voltage is VREF x 2. The 0.5x gain setting can be useful to obtain a higher input voltage range when using a small VREF voltage, or to measure input voltages that are between VREF and VDD. Gain settings for the ADC are controlled by the ADGN bit in register ADC0CF. Note that even with a gain setting of 0.5, voltages above the supply rail cannot be measured directly by the ADC.

14.3. 8-Bit Mode

Setting the ADC08BE bit in register ADC0CF to 1 will put the ADC in 8-bit mode. In 8-bit mode, only the 8 MSBs of data are converted, allowing the conversion to be completed in fewer SAR clock cycles than a 10-bit conversion. The two LSBs of a conversion are always 00 in this mode, and the ADC0L register will always read back 0x00.

14.4. 12-Bit Mode

When configured for 12-bit conversions, the ADC performs four 10-bit conversions using four different reference voltages and combines the results into a single 12-bit value. Unlike simple averaging techniques, this method provides true 12-bit resolution of AC or DC input signals without depending on noise to provide dithering. The converter also employs a hardware dynamic element matching algorithm that reconfigures the largest elements of the internal DAC for each of the four 10-bit conversions. This reconfiguration cancels any matching errors and enables the converter to achieve 12-bit linearity performance to go along with its 12-bit resolution.

The 12-bit mode is enabled by setting the AD12BE bit in register ADC0AC to logic 1 and configuring the ADC in burst mode (ADBMEN = 1) for four or more conversions. The conversion can be initiated using any of the conversion start sources, and the 12-bit result will appear in the ADC0H and ADC0L registers. Since the 12-bit result is formed from a combination of four 10-bit results, the maximum output value is 4 x (1023) = 4092, rather than the max value of (2^12 – 1) = 4095 that is produced by a traditional 12-bit converter. To further increase resolution, the burst mode repeat value may be configured to any multiple of four conversions. For example, if a repeat value of 16 is selected, the ADC0 output will be a 14-bit number (sum of four 12-bit numbers) with 13 effective bits of resolution.

The AD12SM bit in register ADC0TK controls when the ADC will track and sample the input signal. When AD12SM is set to 1, the selected input signal will be tracked before the first conversion of a set and held internally during all four conversions. When AD12SM is cleared to 0, the ADC will track and sample the selected input before each of the four conversions in a set. When maximum throughput (180-200 ksps) is

17.2. Functional Description

The comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the port pins: a synchronous “latched” output (CPn), or an asynchronous “raw” output (CPnA). The asynchronous CPnA signal is available even when the system clock is not active. This allows the comparator to operate and generate an output with the device in STOP mode.

When disabled, the comparator output (if assigned to a port I/O pin via the crossbar) defaults to the logic low state, and the power supply to the comparator is turned off.

The comparator response time may be configured in software via the CPTnMD register. Selecting a longer response time reduces the comparator supply current.

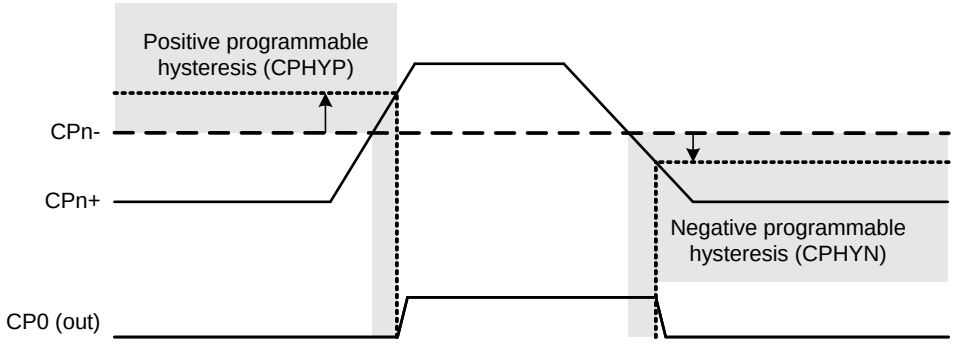


Figure 17.2. Comparator Hysteresis Plot

The comparator hysteresis is software-programmable via its Comparator Control register CPTnCN. The user can program both the amount of hysteresis voltage (referred to the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage.

The comparator hysteresis is programmable using the CPHYN and CPHYP fields in the Comparator Control Register CPTnCN. The amount of negative hysteresis voltage is determined by the settings of the CPHYN bits. As shown in Figure 17.2, settings of 20, 10, or 5 mV (nominal) of negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of positive hysteresis is determined by the setting the CPHYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. The CPFIF flag is set to logic 1 upon a comparator falling-edge occurrence, and the CPRIF flag is set to logic 1 upon the comparator rising-edge occurrence. Once set, these bits remain set until cleared by software. The comparator rising-edge interrupt mask is enabled by setting CPRIE to a logic 1. The comparator falling-edge interrupt mask is enabled by setting CPFIE to a logic 1.

The output state of the comparator can be obtained at any time by reading the CPOUT bit. The comparator is enabled by setting the CPEN bit to logic 1, and is disabled by clearing this bit to logic 0.

Note that false rising edges and falling edges can be detected when the comparator is first powered on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed, before enabling comparator interrupts.

Register 21.5. P0MASK: Port 0 Mask

Bit	7	6	5	4	3	2	1	0
Name	P0MASK							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xFE								

Table 21.8. P0MASK Register Bit Descriptions

Bit	Name	Function
7:0	P0MASK	**Port 0 Mask Value.** Selects P0 pins to be compared to the corresponding bits in P0MAT. 0: P0.x pin logic value is ignored and will cause a port mismatch event. 1: P0.x pin logic value is compared to P0MAT.x.

Register 21.7. P0: Port 0 Pin Latch

Bit	7	6	5	4	3	2	1	0
Name	P0							
Type	RW							
Reset	1	1	1	1	1	1	1	1
SFR Address: 0x80 (bit-addressable)								

Table 21.10. P0 Register Bit Descriptions

Bit	Name	Function
7:0	P0	**Port 0 Data.** Writing this register sets the port latch logic value for the associated I/O pins configured as digital I/O. Reading this register returns the logic value at the pin, regardless if it is configured as output or input.

23.1. Signal Descriptions

The four signals used by SPI0 (MOSI, MISO, SCK, NSS) are described below.

23.1.1. Master Out, Slave In (MOSI)

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI0 is operating as a master and an input when SPI0 is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

23.1.2. Master In, Slave Out (MISO)

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI0 is operating as a master and an output when SPI0 is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

23.1.3. Serial Clock (SCK)

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines. SPI0 generates this signal when operating as a master. The SCK signal is ignored by a SPI slave when the slave is not selected (NSS = 1) in 4-wire slave mode.

23.1.4. Slave Select (NSS)

The function of the slave-select (NSS) signal is dependent on the setting of the NSSMD1 and NSSMD0 bits in the SPI0CN register. There are three possible modes that can be selected with these bits:

1. NSSMD[1:0] = 00: 3-Wire Master or 3-Wire Slave Mode: SPI0 operates in 3-wire mode, and NSS is disabled. When operating as a slave device, SPI0 is always selected in 3-wire mode. Since no select signal is present, SPI0 must be the only slave on the bus in 3-wire mode. This is intended for point-to-point communication between a master and one slave.
2. NSSMD[1:0] = 01: 4-Wire Slave or Multi-Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an input. When operating as a slave, NSS selects the SPI0 device. When operating as a master, a 1-to-0 transition of the NSS signal disables the master function of SPI0 so that multiple master devices can be used on the same SPI bus.
3. NSSMD[1:0] = 1x: 4-Wire Master Mode: SPI0 operates in 4-wire mode, and NSS is enabled as an output. The setting of NSSMD0 determines what logic level the NSS pin will output. This configuration should only be used when operating SPI0 as a master device.

See Figure 23.2, Figure 23.3, and Figure 23.4 for typical connection diagrams of the various operational modes. **Note that the setting of NSSMD bits affects the pinout of the device.** When in 3-wire master or 3-wire slave mode, the NSS pin will not be mapped by the crossbar. In all other modes, the NSS signal will be mapped to a pin on the device.

Table 24.6. SMBus Status Decoding: Hardware ACK Enabled (EHACK = 1) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Receiver	1000	0	0	1	A master data byte was received; ACK sent.	Set ACK for next data byte; Read SMB0DAT.	0	0	1	1000
						Set NACK to indicate next data byte as the last data byte; Read SMB0DAT.	0	0	0	1000
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100
		0	0	0	A master data byte was received; NACK sent (last byte).	Read SMB0DAT; send STOP.	0	1	0	—
						Read SMB0DAT; Send STOP followed by START.	1	1	0	1110
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	—

Register 25.5. TL1: Timer 1 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL1							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x8B								

Table 25.7. TL1 Register Bit Descriptions

Bit	Name	Function
7:0	TL1	**Timer 1 Low Byte.** The TL1 register is the low byte of the 16-bit Timer 1.

Register 25.8. TMR2CN: Timer 2 Control

Bit	7	6	5	4	3	2	1	0
Name	TF2H	TF2L	TF2LEN	TF2CEN	T2SPLIT	TR2	Reserved	T2XCLK
Type	RW	RW	RW	RW	RW	RW	R	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xC8 (bit-addressable)								

Table 25.10. TMR2CN Register Bit Descriptions

Bit	Name	Function
7	TF2H	**Timer 2 High Byte Overflow Flag.** Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF2L	**Timer 2 Low Byte Overflow Flag.** Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. TF2L will be set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.
5	TF2LEN	**Timer 2 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 2 Low Byte interrupts. If Timer 2 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 2 overflows.
4	TF2CEN	**Timer 2 Capture Enable.** When set to 1, this bit enables Timer 2 Capture Mode. If TF2CEN is set and Timer 2 interrupts are enabled, an interrupt will be generated on a falling edge of the selected T2 input pin, and the current 16-bit timer value in TMR2H:TMR2L will be copied to TMR2RLH:TMR2RLL.
3	T2SPLIT	**Timer 2 Split Mode Enable.** When this bit is set, Timer 2 operates as two 8-bit timers with auto-reload. 0: Timer 2 operates in 16-bit auto-reload mode. 1: Timer 2 operates as two 8-bit auto-reload timers.
2	TR2	**Timer 2 Run Control.** Timer 2 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in split mode.
1	Reserved	Must write reset value.

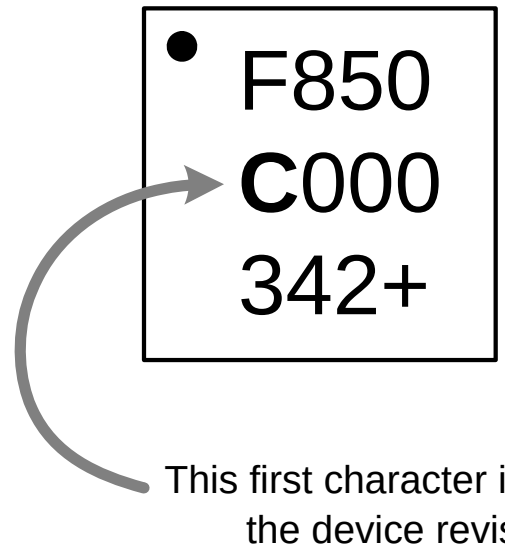


Figure 28.2. QFN-20 Package Revision Marking

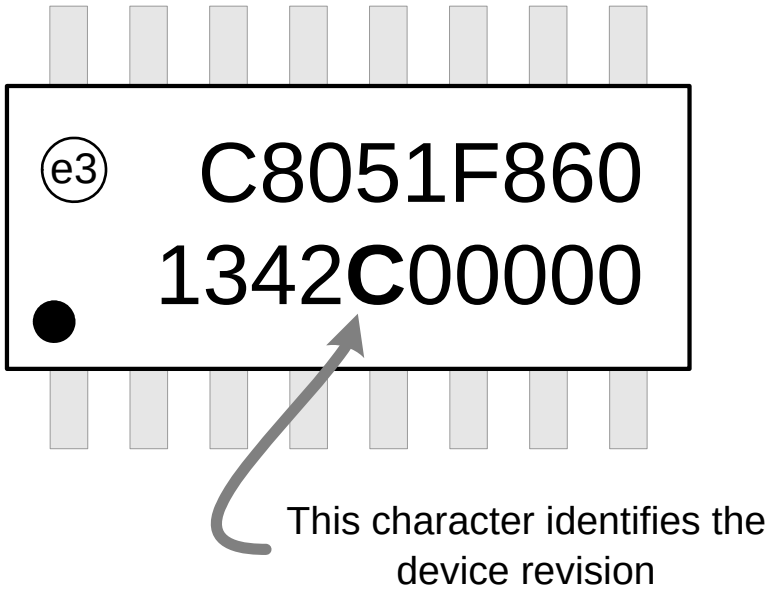


Figure 28.3. SOIC-16 Package Revision Marking

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 0.6

- Updated front page block diagram.
- Updated ADC supply current parameters in Table 1.2, “Power Consumption,” on page 8.
- Corrected flash programming voltage range in "Table 1.4. Flash Memory" on page 11.
- Added ADC Power-On Time specification in Table 1.7, “ADC,” on page 13.
- Added section "1.2. Typical Performance Curves" on page 19.
- Corrected DERIVID Information in Table 11.3, “DERIVID Register Bit Descriptions,” on page 70.
- Updated ADC chapter ("14. Analog-to-Digital Converter (ADC0)" on page 85) and expanded section "14.5. Power Considerations" on page 85 with recommended power configuration settings.
- Updated Figure 21.1, “Port I/O Functional Block Diagram,” on page 184.
- Corrected reset value in Register 24.5, “SMB0ADM: SMBus0 Slave Address Mask,” on page 257.
- Corrected description of IE0 in "Table 25.4. TCON Register Bit Descriptions" on page 259.

Revision 0.6 to Revision 0.7

- Added mention of the UID to the front page.
- Updated some TBD values in the "1. Electrical Specifications" on page 8 section.
- Updated Power-On Reset (POR) Threshold maximum Falling Voltage on V_{DD} specification in Table 1.3.
- Updated Reset Delay from non-POR source typical specification in Table 1.3.
- Removed V_{DD} Ramp Time maximum specification in Table 1.3.
- Updated Flash Memory Erase Time specification and added Note 2 to Table 1.4.
- Updated maximum ADC DC performance specifications in Table 1.7.
- Updated minimum and maximum ADC offset error and slope error specifications in Table 1.7.
- Updated conditions on Internal Fast Settling Reference Output Voltage (Full Temperature and Supply Range) in Table 1.8.
- Added a new section "1.2.3. Port I/O Output Drive" on page 21.
- Updated pinout Figure 3.1, Figure 3.2, Figure 3.3, Table 3.1, Table 3.2, and Table 3.3 titles to the correct part numbers.
- Updated the Ordering Information ("4. Ordering Information" on page 42.) for Revision C devices.
- Added mention of the unique identifier to "8. Memory Organization" on page 52.
- Added unique identifier information to "11. Device Identification and Unique Identifier" on page 68.
- Updated device part numbers listed in Table 11.3, “DERIVID Register Bit Descriptions,” on page 70 to include the revision.
- Added "28. Revision-Specific Behavior" on page 301.

Revision 0.7 to Revision 1.0

- Updated Digital Core, ADC, and Temperature Sensor electrical specifications information for -I devices.
- Updated -I part number information in "4. Ordering Information" on page 42.
- Replaced reference to AMX0P and AMX0N with ADC0MX in Table 21.1, “Port I/O Assignment for Analog Functions,” on page 186.
- Added a note to Table 1.13, “Absolute Maximum Ratings,” on page 22 and added a link to the Quality and Reliability Monitor Report.
- Added Operating Junction Temperature to Table 1.13, “Absolute Maximum Ratings,” on page 22.
- Updated all TBDs in "1. Electrical Specifications" on page 8.