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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	CIP-51™
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f850-c-iur

C8051F85x-86x

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Table 1.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (–Ix Devices, -40°C to +125°C)						
Normal Mode—Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 24.5 MHz ²	—	4.45	5.25	mA
		F _{SYSCLK} = 1.53 MHz ²	—	915	1600	μA
		F _{SYSCLK} = 80 kHz ³ , T _A = 25 °C	—	250	290	μA
		F _{SYSCLK} = 80 kHz ³	—	250	725	μA
Idle Mode—Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 24.5 MHz ²	—	2.05	2.6	mA
		F _{SYSCLK} = 1.53 MHz ²	—	550	1000	μA
		F _{SYSCLK} = 80 kHz ³ , T _A = 25 °C	—	125	130	μA
		F _{SYSCLK} = 80 kHz ³	—	125	550	μA
Stop Mode—Core halted and all clocks stopped, Supply monitor off.	I _{DD}	Internal LDO ON, T _A = 25 °C	—	105	120	μA
		Internal LDO ON	—	105	270	μA
		Internal LDO OFF	—	0.2	—	μA
Analog Peripheral Supply Currents (Both –Gx and –Ix Devices)						
High-Frequency Oscillator	I _{HFOSC}	Operating at 24.5 MHz, T _A = 25 °C	—	155	—	μA
Low-Frequency Oscillator	I _{LFOSC}	Operating at 80 kHz, T _A = 25 °C	—	3.5	—	μA
ADC0 Always-on ⁴	I _{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V _{DD} = 3.0 V	—	845	1200	μA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V _{DD} = 3.0 V	—	425	580	μA
ADC0 Burst Mode, 10-bit single conversions, external reference	I _{ADC}	200 ksps, V _{DD} = 3.0 V	—	370	—	μA
		100 ksps, V _{DD} = 3.0 V	—	185	—	μA
		10 ksps, V _{DD} = 3.0 V	—	19	—	μA
Notes:						
1. Currents are additive. For example, where I _{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.						
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.						
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.						
4. ADC0 always-on power excludes internal reference supply current.						
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.						

2.1. Power

2.1.1. LDO

The C8051F85x/86x devices include an internal regulator to regulate the supply voltage down the core operating voltage of 1.8 V. This LDO consumes little power, but can be shut down in the power-saving Stop mode.

2.1.2. Voltage Supply Monitor (VMON0)

The C8051F85x/86x devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware.

The supply monitor module includes the following features:

- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.

2.1.3. Device Power Modes

The C8051F85x/86x devices feature three low power modes in addition to normal operating mode, allowing the designer to save power when the core is not in use. All power modes are detailed in Table 2.1.

Table 2.1. C8051F85x/86x Power Modes

Mode	Description	Mode Entrance	Mode Exit
Normal	Core and peripherals operating at full speed		
Idle	<ul style="list-style-type: none">■ Core halted■ Peripherals operate at full speed	Set IDLE bit in PCON	Any enabled interrupt or reset source
Stop	<ul style="list-style-type: none">■ All clocks stopped■ Core LDO and (optionally) comparators still running■ Pins retain state	Clear STOPCF in REG0MD and Set STOP bit in PCON	Device reset
Shutdown	<ul style="list-style-type: none">■ All clocks stopped■ Core LDO and all analog circuits shut down■ Pins retain state	Set STOPCF in REG0MD and Set STOP bit in PCON	Device reset

In addition, the user may choose to lower the clock speed in Normal and Idle modes to save power when the CPU requirements allow for lower speed.

C8051F85x/86x

7. SOIC-16 Package Specifications

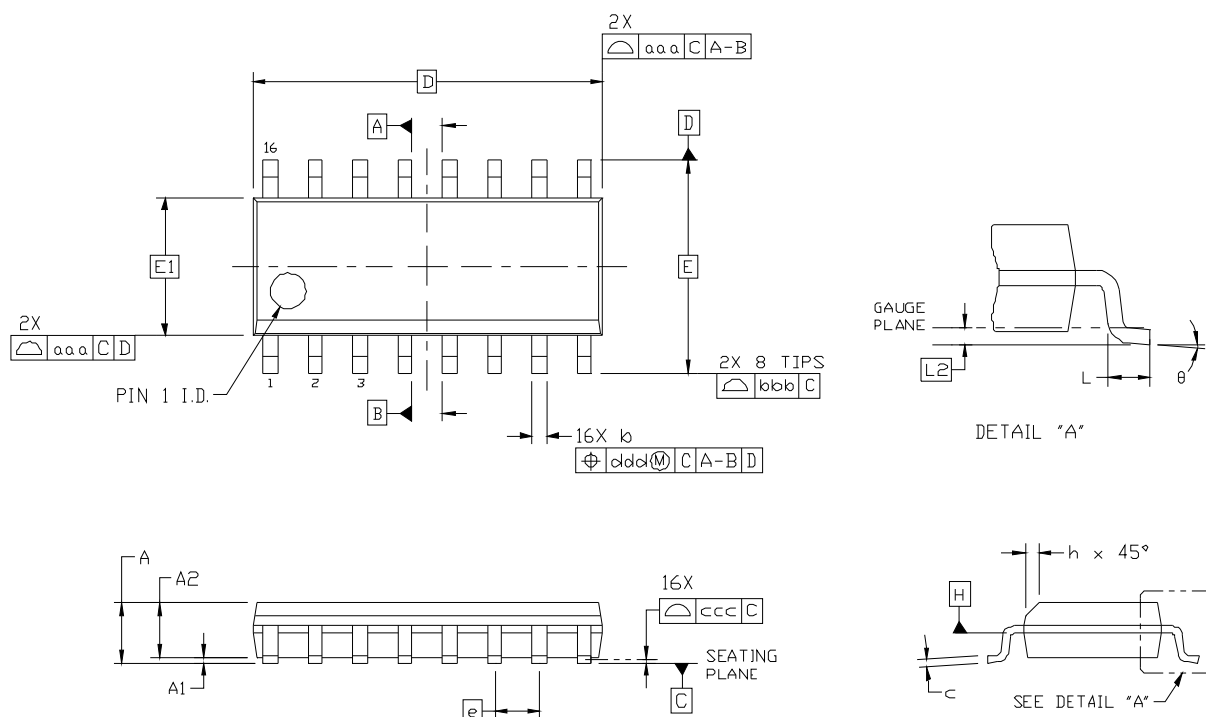


Figure 7.1. SOIC-16 Package Drawing

Table 7.1. SOIC-16 Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—		1.75	L	0.40		1.27
A1	0.10		0.25	L2	0.25 BSC		
A2	1.25		—	h	0.25		0.50
b	0.31		0.51	θ	0°		8°
c	0.17		0.25	aaa	0.10		
D	9.90 BSC			bbb	0.20		
E	6.00 BSC			ccc	0.10		
E1	3.90 BSC			ddd	0.25		
e	1.27 BSC						

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Register 11.3. REVID: Revision Identification

Bit	7	6	5	4	3	2	1	0
Name	REVID							
Type	R							
Reset	X	X	X	X	X	X	X	X
SFR Address: 0xB6								

Table 11.4. REVID Register Bit Descriptions

Bit	Name	Function
7:0	REVID	Revision ID. This read-only register returns the 8-bit revision ID. 00000000: Revision A 00000001: Revision B 00000010: Revision C 00000011-11111111: Reserved.

cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction. If more than one interrupt is pending when the CPU exits an ISR, the CPU will service the next highest priority interrupt that is pending.

14.1. ADC0 Analog Multiplexer

ADC0 on C8051F85x/86x has an analog multiplexer capable of selecting any pin on ports P0 and P1 (up to 16 total), the on-chip temperature sensor, the internal regulated supply, the VDD supply, or GND. ADC0 input channels are selected using the ADC0MX register.

Table 14.1. ADC0 Input Multiplexer Channels

ADC0MX setting	Signal Name	QSOP24 Pin Name	QFN20 Pin Name	SOIC16 Pin Name
00000	ADC0.0	P0.0	P0.0	P0.0
00001	ADC0.1	P0.1	P0.1	P0.1
00010	ADC0.2	P0.2	P0.2	P0.2
00011	ADC0.3	P0.3	P0.3	P0.3
00100	ADC0.4	P0.4	P0.4	P0.4
00101	ADC0.5	P0.5	P0.5	P0.5
00110	ADC0.6	P0.6	P0.6	P0.6
00111	ADC0.7	P0.7	P0.7	P0.7
01000	ADC0.8	P1.0	P1.0	P1.0
01001	ADC0.9	P1.1	P1.1	P1.1
01010	ADC0.10	P1.2	P1.2	P1.2
01011	ADC0.11	P1.3	P1.3	P1.3
01100	ADC0.12	P1.4	P1.4	Reserved
01101	ADC0.13	P1.5	P1.5	Reserved
01110	ADC0.14	P1.6	P1.6	Reserved
01111	ADC0.15	P1.7	Reserved	Reserved
10000	Temp Sensor	Internal Temperature Sensor		
10001	LDO	Internal 1.8 V LDO Output		
10010	VDD	VDD Supply Pin		
10011	GND	GND Supply Pin		
10100-11111	None	No connection		

14.8. Voltage and Ground Reference Options

The voltage reference multiplexer is configurable to use an externally connected voltage reference, the internal voltage reference, or one of two power supply voltages. The ground reference mux allows the ground reference for ADC0 to be selected between the ground pin (GND) or a port pin dedicated to analog ground (AGND).

The voltage and ground reference options are configured using the REF0CN register.

Important Note About the VREF and AGND Inputs: Port pins are used as the external VREF and AGND inputs. When using an external voltage reference, VREF should be configured as an analog input and skipped by the digital crossbar. When using AGND as the ground reference to ADC0, AGND should be configured as an analog input and skipped by the Digital Crossbar.

14.8.1. External Voltage Reference

To use an external voltage reference, REFSL should be set to 00. Bypass capacitors should be added as recommended by the manufacturer of the external voltage reference. If the manufacturer does not provide recommendations, a 4.7uF in parallel with a 0.1uF capacitor is recommended.

14.8.2. Internal Voltage Reference

For applications requiring the maximum number of port I/O pins, or very short VREF turn-on time, the high-speed reference will be the best internal reference option to choose. The internal reference is selected by setting REFSL to 11. When selected, the internal reference will be automatically enabled/disabled on an as-needed basis by the ADC. The reference can be set to one of two voltage values: 1.65 V or 2.4 V, depending on the value of the IREFLVL bit.

For applications with a non-varying power supply voltage, using the power supply as the voltage reference can provide the ADC with added dynamic range at the cost of reduced power supply noise rejection. To use the external supply pin (VDD) or the 1.8 V regulated digital supply voltage as the reference source, REFSL should be set to 01 or 10, respectively.

Internal reference sources are not routed to the VREF pin, and do not require external capacitors. The electrical specifications tables detail SAR clock and throughput limitations for each reference source.

14.8.3. Analog Ground Reference

To prevent ground noise generated by switching digital logic from affecting sensitive analog measurements, a separate analog ground reference option is available. When enabled, the ground reference for the ADC during both the tracking/sampling and the conversion periods is taken from the AGND pin. Any external sensors sampled by the ADC should be referenced to the AGND pin. If an external voltage reference is used, the AGND pin should be connected to the ground of the external reference and its associated decoupling capacitor. The separate analog ground reference option is enabled by setting GNDSL to 1. Note that when sampling the internal temperature sensor, the internal chip ground is always used for the sampling operation, regardless of the setting of the GNDSL bit. Similarly, whenever the internal 1.65 V high-speed reference is selected, the internal chip ground is always used during the conversion period, regardless of the setting of the GNDSL bit.

Register 14.2. ADC0CN1: ADC0 Control 1

Bit	7	6	5	4	3	2	1	0
Name	Reserved							ADCMBE
Type	R							RW
Reset	0	0	0	0	0	0	0	0

SFR Address: 0xB2

Table 14.5. ADC0CN1 Register Bit Descriptions

Bit	Name	Function
7:1	Reserved	Must write reset value.
0	ADCMBE	Common Mode Buffer Enable. 0: Disable the common mode buffer. This setting should be used only if the tracking time of the signal is greater than 1.5 us. 1: Enable the common mode buffer. This setting should be used in most cases, and will give the best dynamic ADC performance. The common mode buffer must be enabled if signal tracking time is less than or equal to 1.5 us.

Register 14.13. ADC0MX: ADC0 Multiplexer Selection

Bit	7	6	5	4	3	2	1	0
Name	Reserved			ADC0MX				
Type	R			RW				
Reset	0	0	0	1	1	1	1	1

SFR Address: 0xBB

Table 14.16. ADC0MX Register Bit Descriptions

Bit	Name	Function
7:5	Reserved	Must write reset value.
4:0	ADC0MX	<p>AMUX0 Positive Input Selection. Selects the positive input channel for ADC0. For reserved bit combinations, no input is selected.</p> <p>00000: ADC0.0 00001: ADC0.1 00010: ADC0.2 00011: ADC0.3 00100: ADC0.4 00101: ADC0.5 00110: ADC0.6 00111: ADC0.7 01000: ADC0.8 01001: ADC0.9 01010: ADC0.10 01011: ADC0.11 01100: ADC0.12 01101: ADC0.13 01110: ADC0.14 01111: ADC0.15 10000: Temperature sensor. 10001: Internal LDO regulator output. 10010: VDD 10011: GND 10100-11111: Reserved.</p>

15. CIP-51 Microcontroller Core

The C8051F85x/86x uses the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The MCU family has a superset of all the peripherals included with a standard 8051. The CIP-51 also includes on-chip debug hardware and interfaces directly with the analog and digital subsystems providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 15.1 for a block diagram). The CIP-51 includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 25 MIPS Peak Throughput with 25 MHz Clock
- 0 to 25 MHz Clock Frequency
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- On-chip Debug Logic
- Program and Data Memory Security

15.1. Performance

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. The CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

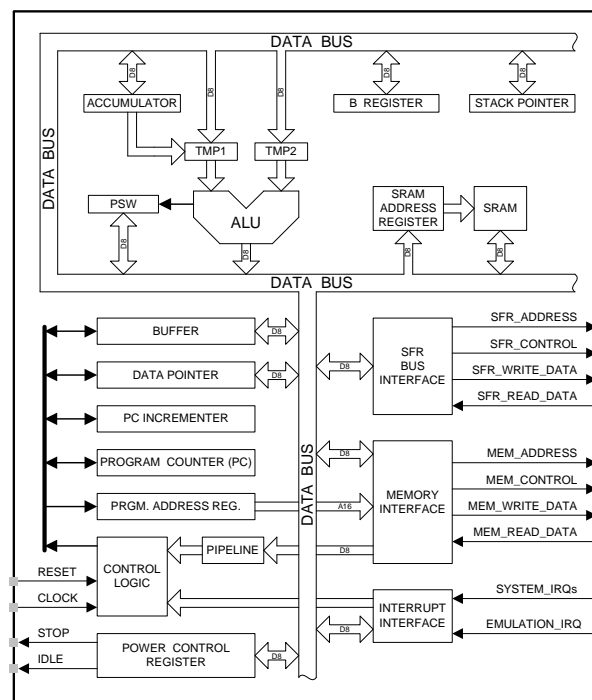


Figure 15.1. CIP-51 Block Diagram

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8

15.4. CPU Core Registers

Register 15.1. DPL: Data Pointer Low

Bit	7	6	5	4	3	2	1	0
Name	DPL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x82								

Table 15.2. DPL Register Bit Descriptions

Bit	Name	Function
7:0	DPL	Data Pointer Low. The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed flash memory or XRAM.

20.5. Comparator Clear Function

In 8/9/10/11/16-bit PWM modes, the comparator clear function utilizes the Comparator0 output synchronized to the system clock to clear CEXn to logic low for the current PWM cycle. This comparator clear function can be enabled for each PWM channel by setting the CPCEn bits to 1 in the PCA0CLR SFR. When the comparator clear function is disabled, CEXn is unaffected.

The asynchronous Comparator 0 output is logic high when the voltage of CP0+ is greater than CP0- and logic low when the voltage of CP0+ is less than CP0-. The polarity of the Comparator 0 output is used to clear CEXn as follows: when CPCPOL = 0, CEXn is cleared on the falling edge of the Comparator0 output (see Figure 20.8); when CPCPOL = 1, CEXn is cleared on the rising edge of the Comparator0 output (see Figure 20.9).

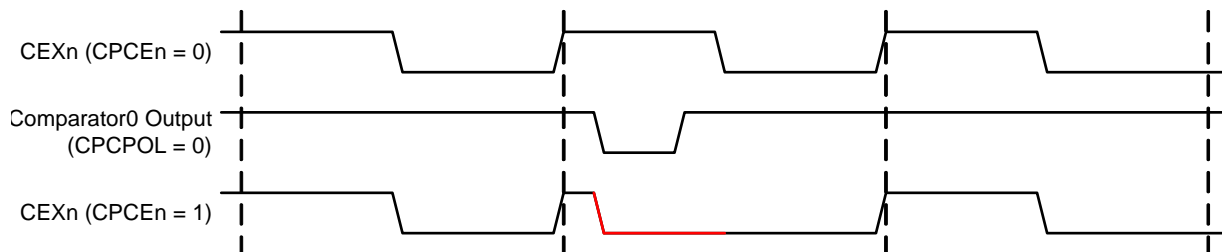


Figure 20.8. CEXn with CPCEn = 1, CPCPOL = 0

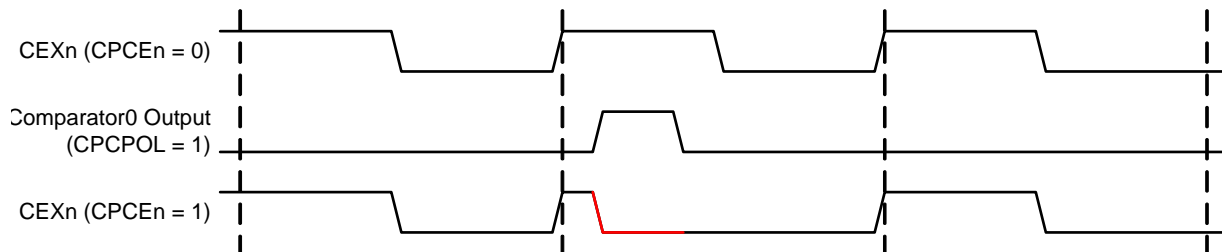


Figure 20.9. CEXn with CPCEn = 1, CPCPOL = 1

In the PWM cycle following the current cycle, should the Comparator 0 output remain logic low when CPCPOL = 0 or logic high when CPCPOL = 1, CEXn will continue to be cleared. See Figure 20.10 and Figure 20.11.

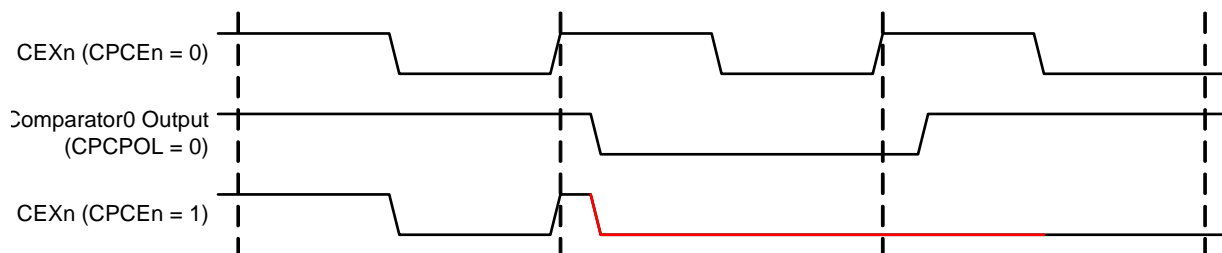


Figure 20.10. CEXn with CPCEn = 1, CPCPOL = 0

21.1. General Port I/O Initialization

Port I/O initialization consists of the following steps:

1. Select the input mode (analog or digital) for all port pins, using the Port Input Mode register (PnMDIN).
2. Select the output mode (open-drain or push-pull) for all port pins, using the Port Output Mode register (PnMDOUT).
3. Select any pins to be skipped by the I/O crossbar using the Port Skip registers (PnSKIP).
4. Assign port pins to desired peripherals.
5. Enable the crossbar (XBARE = '1').

All port pins must be configured as either analog or digital inputs. Any pins to be used as Comparator or ADC inputs should be configured as an analog inputs. When a pin is configured as an analog input, its weak pullup, digital driver, and digital receiver are disabled. This process saves power and reduces noise on the analog input. Pins configured as digital inputs may still be used by analog peripherals; however this practice is not recommended.

Additionally, all analog input pins should be configured to be skipped by the crossbar (accomplished by setting the associated bits in PnSKIP). Port input mode is set in the PnMDIN register, where a '1' indicates a digital input, and a '0' indicates an analog input. All pins default to digital inputs on reset.

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMDOUT). Each port output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is the SMBus (SDA, SCL) pins, which are configured as open-drain regardless of the PnMDOUT settings. When the WEAKPUD bit in XBR1 is '0', a weak pullup is enabled for all Port I/O configured as open-drain. WEAKPUD does not affect the push-pull Port I/O. Furthermore, the weak pullup is turned off on an output that is driving a '0' to avoid unnecessary power dissipation.

Registers XBR0 and XBR1 must be loaded with the appropriate values to select the digital I/O functions required by the design. Setting the XBARE bit in XBR2 to '1' enables the crossbar. Until the crossbar is enabled, the external pins remain as standard port I/O (in input mode), regardless of the XBRn Register settings. For given XBRn Register settings, one can determine the I/O pin-out using the Priority Decode Table; as an alternative, Silicon Labs provides configuration utility software to determine the port I/O pin-assignments based on the crossbar register settings.

The crossbar must be enabled to use port pins as standard port I/O in output mode. Port output drivers of all crossbar pins are disabled whenever the crossbar is disabled.

23.7. SPI Control Registers

Register 23.1. SPI0CFG: SPI0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT
Type	R	RW	RW	RW	R	R	R	R
Reset	0	0	0	0	0	1	1	1
SFR Address: 0xA1								

Table 23.2. SPI0CFG Register Bit Descriptions

Bit	Name	Function
7	SPIBSY	SPI Busy. This bit is set to logic 1 when a SPI transfer is in progress (master or slave mode).
6	MSTEN	Master Mode Enable. 0: Disable master mode. Operate in slave mode. 1: Enable master mode. Operate as a master.
5	CKPHA	SPI0 Clock Phase. 0: Data centered on first edge of SCK period. 1: Data centered on second edge of SCK period.
4	CKPOL	SPI0 Clock Polarity. 0: SCK line low in idle state. 1: SCK line high in idle state.
3	SLVSEL	Slave Selected Flag. This bit is set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.
2	NSSIN	NSS Instantaneous Pin Input. This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.
1	SRMT	Shift Register Empty (valid in slave mode only). This bit will be set to logic 1 when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK. SRMT = 1 when in Master Mode.
Note: In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device.		

24. System Management Bus / I²C (SMBus0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

Reads and writes to the SMBus by the system controller are byte oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/20th of the system clock as a master or slave (this can be faster than allowed by the SMBus specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation. The SMBus peripherals can be fully driven by software (i.e., software accepts/rejects slave addresses, and generates ACKs), or hardware slave address recognition and automatic ACK generation can be enabled to minimize software overhead. A block diagram of the SMBus0 peripheral is shown in Figure 24.1.

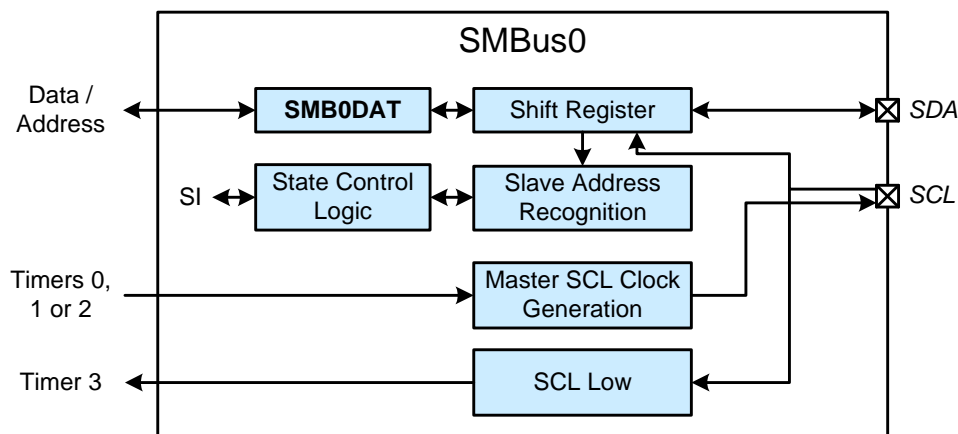


Figure 24.1. SMBus0 Block Diagram

Table 24.5. SMBus Status Decoding: Hardware ACK Disabled (EHACK = 0) (Continued)

Mode	Values Read			Current SMBus State	Typical Response Options	Values to Write			Next Status Vector Expected	
	Status Vector	ACKRQ	ARBLOST			ACK	STA	STO		ACK
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	—
Slave Receiver	0010	1	0	X	A slave address + R/W was received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	—
	0010	1	1	X	Lost arbitration as master; slave address + R/W received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	—
						Reschedule failed transfer; NACK received address.	1	0	0	1110
	0001	0	0	X	A STOP was detected while addressed as a Slave Transmitter or Slave Receiver.	Clear STO.	0	0	X	—
						Lost arbitration while attempting a STOP.	No action required (transfer complete/aborted).	0	0	0
	0000	1	0	X	A slave byte was received; ACK requested.	Acknowledge received byte; Read SMB0DAT.	0	0	1	0000
NACK received byte.						0	0	0	—	

Table 24.5. SMBus Status Decoding: Hardware ACK Disabled (EHACK = 0) (Continued)

Mode	Values Read				Current SMBus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Bus Error Condition	0010	0	1	X	Lost arbitration while attempting a repeated START.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110
	0001	0	1	X	Lost arbitration due to a detected STOP.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110
	0000	1	1	X	Lost arbitration while transmitting a data byte as master.	Abort failed transfer.	0	0	0	—
						Reschedule failed transfer.	1	0	0	1110

Table 24.6. SMBus Status Decoding: Hardware ACK Enabled (EHACK = 1)

Mode	Values Read				Current SMBus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Transmitter	1110	0	0	X	A master START was generated.	Load slave address + R/W into SMB0DAT.	0	0	X	1100
		0	0	0	A master data or address byte was transmitted; NACK received.	Set STA to restart transfer.	1	0	X	1110
						Abort transfer.	0	1	X	—
	1100	0	0	1	A master data or address byte was transmitted; ACK received.	Load next data byte into SMB0-DAT.	0	0	X	1100
						End transfer with STOP.	0	1	X	—
						End transfer with STOP and start another transfer.	1	1	X	—
						Send repeated START.	1	0	X	1110
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT). Set ACK for initial data byte.	0	0	1	1000

Register 25.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH0							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x8C								

Table 25.8. TH0 Register Bit Descriptions

Bit	Name	Function
7:0	TH0	Timer 0 High Byte. The TH0 register is the high byte of the 16-bit Timer 0.

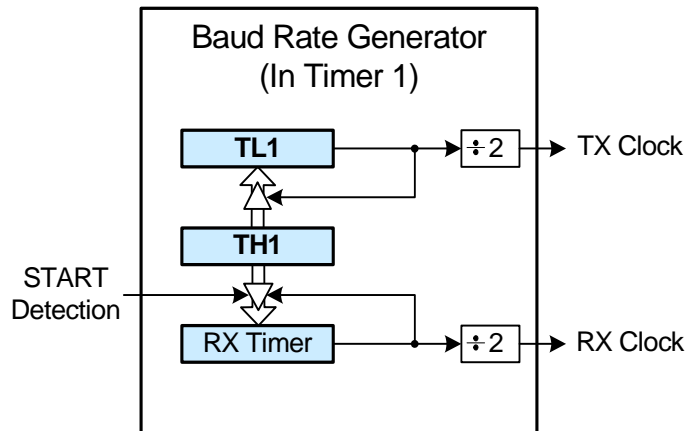


Figure 26.2. UART0 Baud Rate Logic

Timer 1 should be configured for Mode 2, 8-bit auto-reload. The Timer 1 reload value should be set so that overflows will occur at two times the desired UART baud rate frequency. Note that Timer 1 may be clocked by one of six sources: SYSCLK, SYSCLK/4, SYSCLK/12, SYSCLK/48, the external oscillator clock/8, or an external input T1. For any given Timer 1 overflow rate, the UART0 baud rate is determined by Equation 26.1.

$$\text{UartBaudRate} = \frac{1}{2} \times \text{T1_Overflow_Rate}$$

Equation 26.1. UART0 Baud Rate

Timer 1 overflow rate is selected as described in the Timer section. A quick reference for typical baud rates and system clock frequencies is given in Table 26.1.