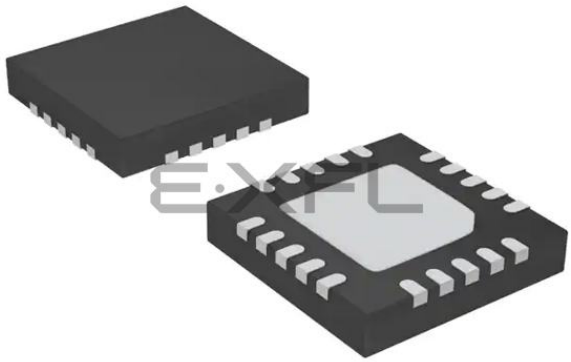

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f852-c-gm

Table 1.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	490	—	µA
		100 ksps, V_{DD} = 3.0 V	—	245	—	µA
		10 ksps, V_{DD} = 3.0 V	—	23	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	530	—	µA
		50 ksps, V_{DD} = 3.0 V	—	265	—	µA
		10 ksps, V_{DD} = 3.0 V	—	53	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	950	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	420	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	85	—	µA
Internal ADC0 Reference, Always-on[5]	I_{IREF}	Normal Power Mode	—	680	790	µA
		Low Power Mode	—	160	210	µA
Temperature Sensor	I_{TSENSE}		—	75	120	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CPnMD = 11	—	0.5	—	µA
		CPnMD = 10	—	3	—	µA
		CPnMD = 01	—	10	—	µA
		CPnMD = 00	—	25	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	µA

Notes:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

Table 1.7. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	200	ksps
		10 Bit Mode	—	—	800	ksps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t_{PWR}		1.2	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode, Reference is 2.4 V internal	—	—	6.25	MHz
		High Speed Mode, Reference is not 2.4 V internal	—	—	12.5	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 12.25 MHz, System Clock = 24.5 MHz.		1.1		µs
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range*	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±2.3	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	–1	±0.7	1.9	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
***Note:** Absolute input pin voltage is limited by the V_{DD} supply.						

1.2.2. ADC Supply Current

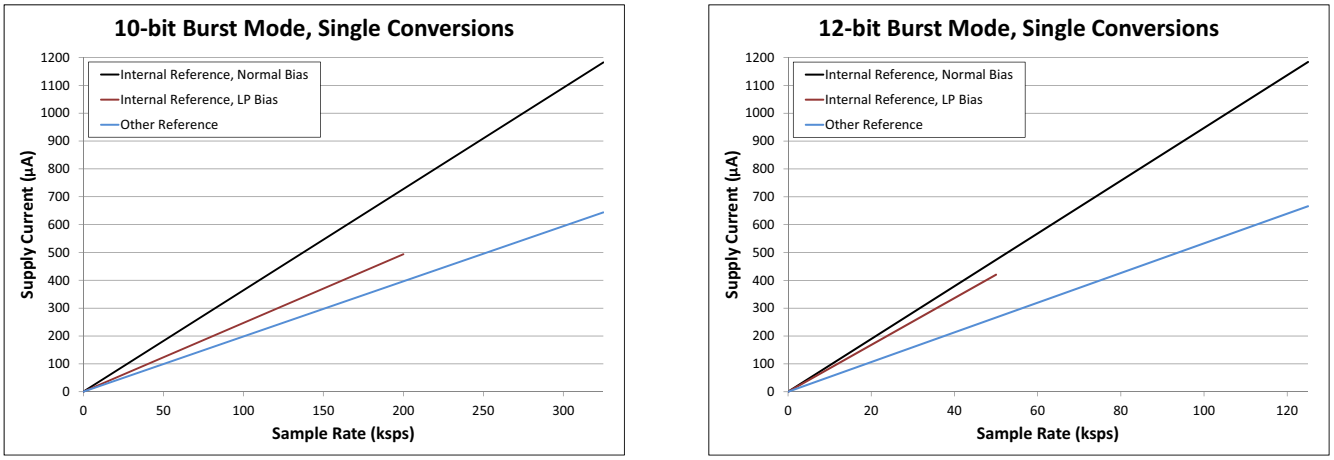

Figure 1.3. Typical ADC and Internal Reference Power Consumption in Burst Mode

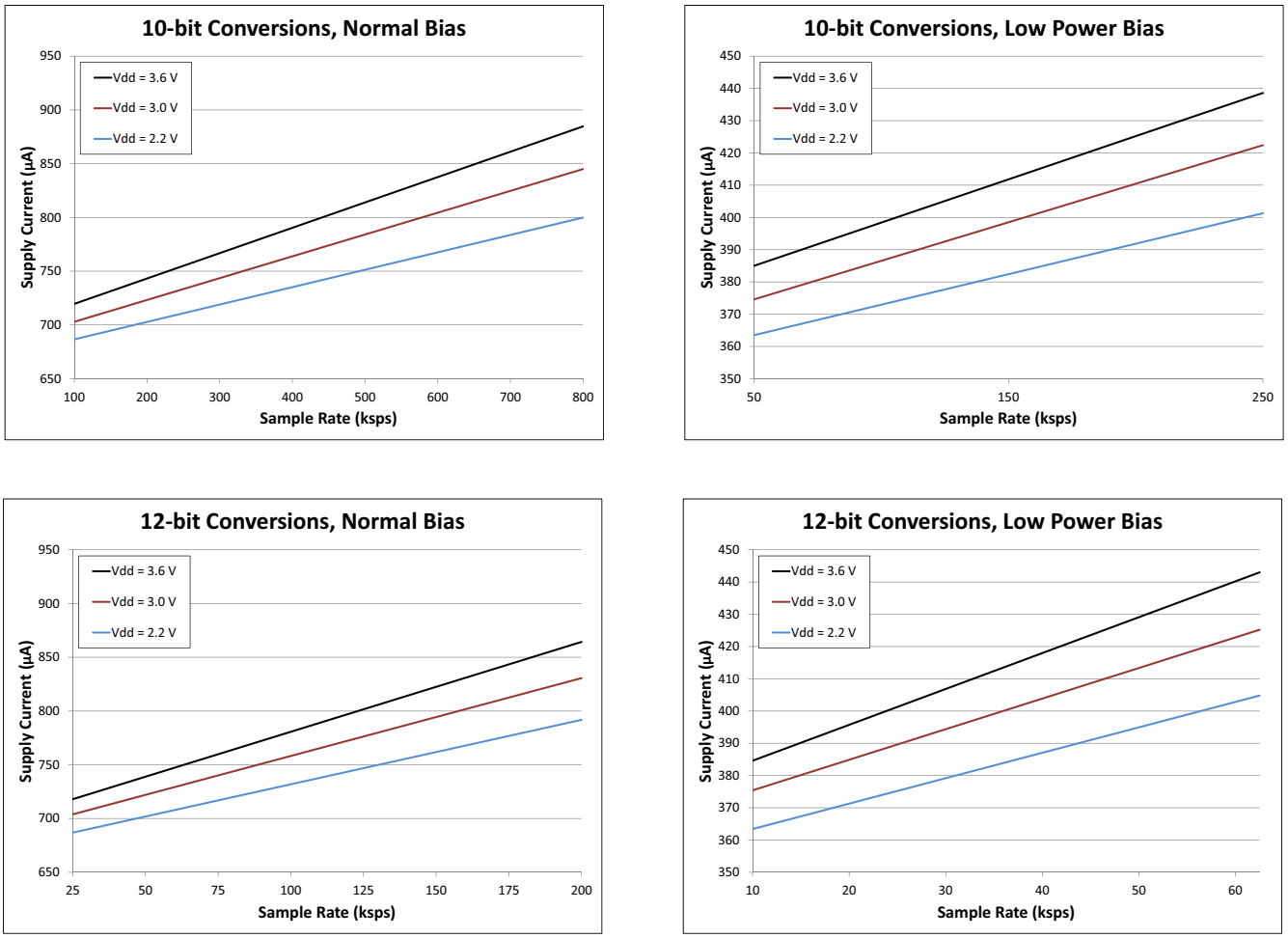

Figure 1.4. Typical ADC Power Consumption in Normal (Always-On) Mode

Table 3.1. Pin Definitions for C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
N/C	No Connection	1 13 24			

Table 4.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of ADC0 Channels	I/O with Comparator 0/1 Inputs	Pb-free (RoHS Compliant)	AEC-Q100 Qualified	Temperature Range	Package
C8051F850-C-GM	8	512	16	15	15	✓	✓	-40 to 85 °C	QFN-20
C8051F850-C-GU	8	512	18	16	16	✓	✓	-40 to 85 °C	QSOP-24
C8051F851-C-GM	4	512	16	15	15	✓	✓	-40 to 85 °C	QFN-20
C8051F851-C-GU	4	512	18	16	16	✓	✓	-40 to 85 °C	QSOP-24
C8051F852-C-GM	2	256	16	15	15	✓	✓	-40 to 85 °C	QFN-20
C8051F852-C-GU	2	256	18	16	16	✓	✓	-40 to 85 °C	QSOP-24
C8051F853-C-GM	8	512	16	—	15	✓	✓	-40 to 85 °C	QFN-20
C8051F853-C-GU	8	512	18	—	16	✓	✓	-40 to 85 °C	QSOP-24
C8051F854-C-GM	4	512	16	—	15	✓	✓	-40 to 85 °C	QFN-20
C8051F854-C-GU	4	512	18	—	16	✓	✓	-40 to 85 °C	QSOP-24
C8051F855-C-GM	2	256	16	—	15	✓	✓	-40 to 85 °C	QFN-20
C8051F855-C-GU	2	256	18	—	16	✓	✓	-40 to 85 °C	QSOP-24
C8051F860-C-GS	8	512	13	12	12	✓	✓	-40 to 85 °C	SOIC-16
C8051F861-C-GS	4	512	13	12	12	✓	✓	-40 to 85 °C	SOIC-16
C8051F862-C-GS	2	256	13	12	12	✓	✓	-40 to 85 °C	SOIC-16
C8051F863-C-GS	8	512	13	—	12	✓	✓	-40 to 85 °C	SOIC-16
C8051F864-C-GS	4	512	13	—	12	✓	✓	-40 to 85 °C	SOIC-16
C8051F865-C-GS	2	256	13	—	12	✓	✓	-40 to 85 °C	SOIC-16

cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction. If more than one interrupt is pending when the CPU exits an ISR, the CPU will service the next highest priority interrupt that is pending.

Register 14.10. ADC0GTL: ADC0 Greater-Than Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTL							
Type	RW							
Reset	1	1	1	1	1	1	1	1
SFR Address: 0xC3								

Table 14.13. ADC0GTL Register Bit Descriptions

Bit	Name	Function
7:0	ADC0GTL	**Greater-Than Low Byte.** Least Significant Byte of the 16-bit Greater-Than window compare register.
Note: In 8-bit mode, this register should be set to 0x00.		

15.4. CPU Core Registers

Register 15.1. DPL: Data Pointer Low

Bit	7	6	5	4	3	2	1	0
Name	DPL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x82								

Table 15.2. DPL Register Bit Descriptions

Bit	Name	Function
7:0	DPL	**Data Pointer Low.** The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed flash memory or XRAM.

Register 15.2. DPH: Data Pointer High

Bit	7	6	5	4	3	2	1	0
Name	DPH							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x83								

Table 15.3. DPH Register Bit Descriptions

Bit	Name	Function
7:0	DPH	**Data Pointer High.** The DPH register is the high byte of the 16-bit DPTR. DPTR is used to access indirectly addressed flash memory or XRAM.

17.2. Functional Description

The comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the port pins: a synchronous “latched” output (CPn), or an asynchronous “raw” output (CPnA). The asynchronous CPnA signal is available even when the system clock is not active. This allows the comparator to operate and generate an output with the device in STOP mode.

When disabled, the comparator output (if assigned to a port I/O pin via the crossbar) defaults to the logic low state, and the power supply to the comparator is turned off.

The comparator response time may be configured in software via the CPTnMD register. Selecting a longer response time reduces the comparator supply current.

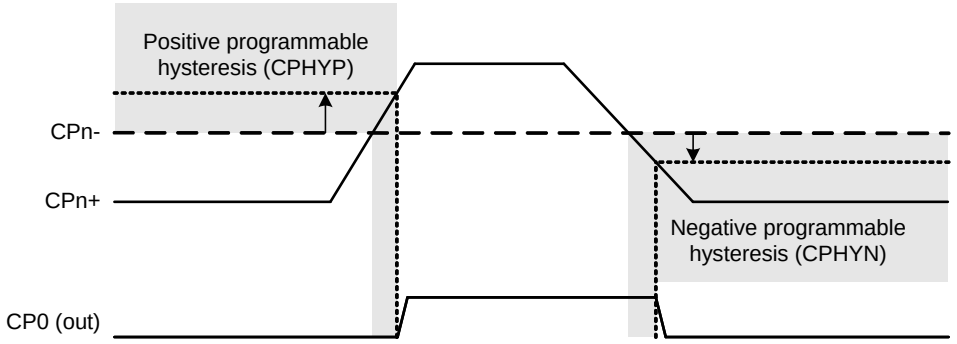

Figure 17.2. Comparator Hysteresis Plot

The comparator hysteresis is software-programmable via its Comparator Control register CPTnCN. The user can program both the amount of hysteresis voltage (referred to the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage.

The comparator hysteresis is programmable using the CPHYN and CPHYP fields in the Comparator Control Register CPTnCN. The amount of negative hysteresis voltage is determined by the settings of the CPHYN bits. As shown in Figure 17.2, settings of 20, 10, or 5 mV (nominal) of negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of positive hysteresis is determined by the setting the CPHYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. The CPFIF flag is set to logic 1 upon a comparator falling-edge occurrence, and the CPRIF flag is set to logic 1 upon the comparator rising-edge occurrence. Once set, these bits remain set until cleared by software. The comparator rising-edge interrupt mask is enabled by setting CPRIE to a logic 1. The comparator falling-edge interrupt mask is enabled by setting CPFIE to a logic 1.

The output state of the comparator can be obtained at any time by reading the CPOUT bit. The comparator is enabled by setting the CPEN bit to logic 1, and is disabled by clearing this bit to logic 0.

Note that false rising edges and falling edges can be detected when the comparator is first powered on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed, before enabling comparator interrupts.

17.3. Comparator Control Registers

Register 17.1. CPT0CN: Comparator 0 Control

Bit	7	6	5	4	3	2	1	0
Name	CPEN	CPOUT	CPRIF	CPFIF	CPHYP		CPHYN	
Type	RW	R	RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x9B								

Table 17.5. CPT0CN Register Bit Descriptions

Bit	Name	Function
7	CPEN	**Comparator 0 Enable Bit.** 0: Comparator Disabled. 1: Comparator Enabled.
6	CPOUT	**Comparator 0 Output State Flag.** 0: Voltage on CP0P < CP0N. 1: Voltage on CP0P > CP0N.
5	CPRIF	**Comparator 0 Rising-Edge Flag. Must be cleared by software.** 0: No Comparator Rising Edge has occurred since this flag was last cleared. 1: Comparator Rising Edge has occurred.
4	CPFIF	**Comparator 0 Falling-Edge Flag. Must be cleared by software.** 0: No Comparator Falling-Edge has occurred since this flag was last cleared. 1: Comparator Falling-Edge has occurred.
3:2	CPHYP	**Comparator 0 Positive Hysteresis Control Bits.** 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = 5 mV. 10: Positive Hysteresis = 10 mV. 11: Positive Hysteresis = 20 mV.
1:0	CPHYN	**Comparator 0 Negative Hysteresis Control Bits.** 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = 5 mV. 10: Negative Hysteresis = 10 mV. 11: Negative Hysteresis = 20 mV.

Register 20.13. PCA0CPM2: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xDC								

Table 20.15. PCA0CPM2 Register Bit Descriptions

Bit	Name	Function
7	PWM16	**16-bit Pulse Width Modulation Enable.** This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected. 1: 16-bit PWM selected.
6	ECOM	**Comparator Function Enable.** This bit enables the comparator function.
5	CAPP	**Capture Positive Function Enable.** This bit enables the positive edge capture capability.
4	CAPN	**Capture Negative Function Enable.** This bit enables the negative edge capture capability.
3	MAT	**Match Function Enable.** This bit enables the match function. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCF2 bit in the PCA0MD register to be set to logic 1.
2	TOG	**Toggle Function Enable.** This bit enables the toggle function. When enabled, matches of the PCA counter with the capture/compare register cause the logic level on the CEX2 pin to toggle. If the PWM bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWM	**Pulse Width Modulation Mode Enable.** This bit enables the PWM function. When enabled, a pulse width modulated signal is output on the CEX2 pin. 8 to 11-bit PWM is used if PWM16 is cleared; 16-bit mode is used if PWM16 is set to logic 1. If the TOG bit is also set, the module operates in Frequency Output Mode.
0	ECCF	**Capture/Compare Flag Interrupt Enable.** This bit sets the masking of the Capture/Compare Flag (CCF2) interrupt. 0: Disable CCF2 interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCF2 is set.

21.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins can be assigned to various analog, digital, and external interrupt functions. The port pins assigned to analog functions should be configured for analog I/O, and port pins assigned to digital or external interrupt functions should be configured for digital I/O.

21.2.1. Assigning Port I/O Pins to Analog Functions

Table 21.1 shows all available analog functions that require port I/O assignments. Table 21.1 shows the potential mapping of port I/O to each analog function.

Table 21.1. Port I/O Assignment for Analog Functions

Analog Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
ADC Input	P0.0 - P1.7	ADC0MX, PnSKIP, PnMDIN
Comparator0 Input	P0.0 - P1.7	CPT0MX, PnSKIP, PnMDIN
Comparator1 Input	P0.0 - P1.7	CPT1MX, PnSKIP, PnMDIN
Voltage Reference (VREF)	P0.0	REF0CN, PnSKIP, PnMDIN
Reference Ground (AGND)	P0.1	REF0CN, PnSKIP, PnMDIN

21.2.2. Assigning Port I/O Pins to Digital Functions

Any port pins not assigned to analog functions may be assigned to digital functions or used as GPIO. Most digital functions rely on the crossbar for pin assignment; however, some digital functions bypass the crossbar in a manner similar to the analog functions listed above. Table 21.2 shows all digital functions available through the crossbar and the potential mapping of port I/O to each function.

Table 21.2. Port I/O Assignment for Digital Functions

Digital Function	Potentially Assignable Port Pins	SFR(s) Used for Assignment
UART0, SPI0, SMBus0, CP0, CP0A, CP1, CP1A, SYSCLK, PCA0 (CEX0-2 and ECI), T0, T1 or T2.	Any port pin available for assignment by the crossbar. This includes P0.0 - P1.7 pins which have their PnSKIP bit set to ‘0’. **Note:** The crossbar will always assign UART0 pins to P0.4 and P0.5.	XBR0, XBR1, XBR2
Any pin used for GPIO	P0.0 - P2.1	P0SKIP, P1SKIP, P2SKIP

Register 21.2. XBR1: Port I/O Crossbar 1

Bit	7	6	5	4	3	2	1	0
Name	Reserved		T2E	T1E	T0E	ECIE	PCA0ME	
Type	R	RW	RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xE2								

Table 21.5. XBR1 Register Bit Descriptions

Bit	Name	Function
7:6	Reserved	Must write reset value.
5	T2E	**T2 Enable.** 0: T2 unavailable at Port pin. 1: T2 routed to Port pin.
4	T1E	**T1 Enable.** 0: T1 unavailable at Port pin. 1: T1 routed to Port pin.
3	T0E	**T0 Enable.** 0: T0 unavailable at Port pin. 1: T0 routed to Port pin.
2	ECIE	**PCA0 External Counter Input Enable.** 0: ECI unavailable at Port pin. 1: ECI routed to Port pin.
1:0	PCA0ME	**PCA Module I/O Enable Bits.** 00: All PCA I/O unavailable at Port pins. 01: CEX0 routed to Port pin. 10: CEX0, CEX1 routed to Port pins. 11: CEX0, CEX1, CEX2 routed to Port pins.

1. Enable the VDD supply monitor (VMONEN = 1).
2. Wait for the VDD supply monitor to stabilize (optional).
3. Enable the VDD monitor as a reset source in the RSTSRC register.

22.4. External Reset

The external $\overline{\text{RST}}$ pin provides a means for external circuitry to force the device into a reset state. Asserting an active-low signal on the $\overline{\text{RST}}$ pin generates a reset; an external pullup and/or decoupling of the $\overline{\text{RST}}$ pin may be necessary to avoid erroneous noise-induced resets. The PINRSF flag is set on exit from an external reset.

22.5. Missing Clock Detector Reset

The Missing Clock Detector (MCD) is a one-shot circuit that is triggered by the system clock. If the system clock remains high or low for more than the MCD time window, the one-shot will time out and generate a reset. After a MCD reset, the MCDRSF flag will read 1, signifying the MCD as the reset source; otherwise, this bit reads 0. Writing a 1 to the MCDRSF bit enables the Missing Clock Detector; writing a 0 disables it. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

22.6. Comparator0 Reset

Comparator0 can be configured as a reset source by writing a 1 to the C0RSEF flag. Comparator0 should be enabled and allowed to settle prior to writing to C0RSEF to prevent any turn-on chatter on the output from generating an unwanted reset. The Comparator0 reset is active-low: if the non-inverting input voltage (on CP0+) is less than the inverting input voltage (on CP0-), the device is put into the reset state. After a Comparator0 reset, the C0RSEF flag will read 1 signifying Comparator0 as the reset source; otherwise, this bit reads ‘0’. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

22.7. Watchdog Timer Reset

The programmable Watchdog Timer (WDT) can be used to prevent software from running out of control during a system malfunction. The WDT function can be enabled or disabled by software as described in the watchdog timer section. If a system malfunction prevents user software from updating the WDT, a reset is generated and the WDTRSF bit is set to ‘1’. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

22.8. Flash Error Reset

If a flash read/write/erase or program read targets an illegal address, a system reset is generated. This may occur due to any of the following:

- A flash write or erase is attempted above user code space.
- A flash read is attempted above user code space.
- A program read is attempted above user code space (i.e. a branch instruction to the reserved area).
- A flash read, write or erase attempt is restricted due to a flash security setting.

The FERROR bit is set following a flash error reset. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

22.9. Software Reset

Software may force a reset by writing a 1 to the SWRSF bit. The SWRSF bit will read 1 following a software forced reset. The state of the $\overline{\text{RST}}$ pin is unaffected by this reset.

Table 23.3. SPI0CN Register Bit Descriptions

Bit	Name	Function
0	SPIEN	**SPI0 Enable.** 0: SPI disabled. 1: SPI enabled.

24.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses an arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames. The position of the ACK interrupt when operating as a receiver depends on whether hardware ACK generation is enabled. As a receiver, the interrupt for an ACK occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled. As a transmitter, interrupts occur **after** the ACK, regardless of whether hardware ACK generation is enabled or not.

24.5.1. Write Sequence (Master)

During a write sequence, an SMBus master writes data to a slave device. The master in this transfer will be a transmitter during the address byte, and a transmitter during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. The interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 24.5 shows a typical master write sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that all of the “data byte transferred” interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.

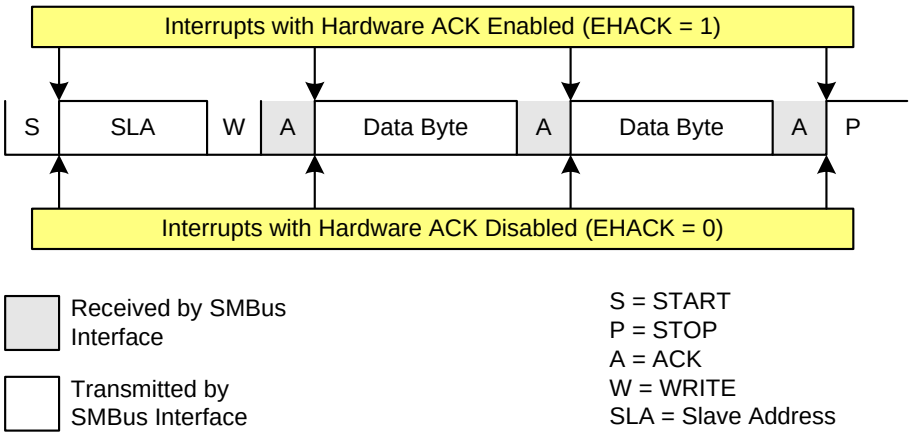

Figure 24.5. Typical Master Write Sequence

24.5.4. Read Sequence (Slave)

During a read sequence, an SMBus master reads data from a slave device. The slave in this transfer will be a receiver during the address byte, and a transmitter during all data bytes. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode (to receive the slave address) when a START followed by a slave address and direction bit (READ in this case) is received. If hardware ACK generation is disabled, upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. The software must respond to the received slave address with an ACK, or ignore the received slave address with a NACK. If hardware ACK generation is enabled, the hardware will apply the ACK for a slave address which matches the criteria set up by SMB0ADR and SMB0ADM. The interrupt will occur after the ACK cycle.

If the received slave address is ignored (by software or hardware), slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are transmitted. If the received slave address is acknowledged, data should be written to SMB0DAT to be transmitted. The interface enters slave transmitter mode, and transmits one or more bytes of data. After each byte is transmitted, the master sends an acknowledge bit; if the acknowledge bit is an ACK, SMB0DAT should be written with the next data byte. If the acknowledge bit is a NACK, SMB0DAT should not be written to before SI is cleared (an error condition may be generated if SMB0DAT is written following a received NACK while in slave transmitter mode). The interface exits slave transmitter mode after receiving a STOP. The interface will switch to slave receiver mode if SMB0DAT is not written following a Slave Transmitter interrupt. Figure 24.8 shows a typical slave read sequence. Two transmitted data bytes are shown, though any number of bytes may be transmitted. Notice that all of the “data byte transferred” interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.

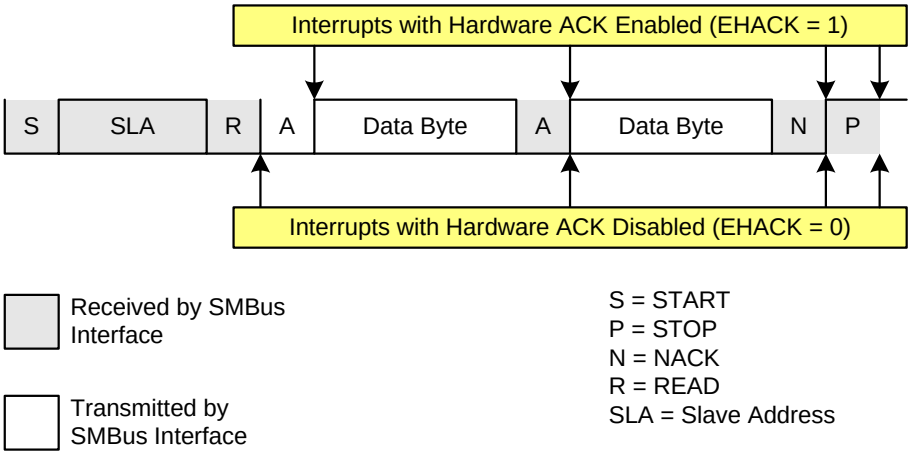

Figure 24.8. Typical Slave Read Sequence

24.6. SMBus Status Decoding

The current SMBus status can be easily decoded using the SMB0CN register. The appropriate actions to take in response to an SMBus event depend on whether hardware slave address recognition and ACK generation is enabled or disabled. Table 24.5 describes the typical actions when hardware slave address recognition and ACK generation is disabled. Table 24.6 describes the typical actions when hardware slave address recognition and ACK generation is enabled. In the tables, STATUS VECTOR refers to the four upper bits of SMB0CN: MASTER, TXMODE, STA, and STO. The shown response options are only the typical responses; application-specific procedures are allowed as long as they conform to the SMBus specification. Highlighted responses are allowed by hardware but do not conform to the SMBus specification.

25.2.2. 8-bit Timers with Auto-Reload

When TnSPLIT is set, the timer operates as two 8-bit timers (TMRnH and TMRnL). Both 8-bit timers operate in auto-reload mode as shown in Figure 25.5. TMRnRLL holds the reload value for TMRnL; TMRnRLH holds the reload value for TMRnH. The TRn bit in TMRnCN handles the run control for TMRnH. TMRnL is always running when configured for 8-bit auto-reload mode.

Each 8-bit timer may be configured to clock from SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. The Clock Select bits (TnMH and TnML in CKCON) select either SYSCLK or the clock defined by the External Clock Select bit (TnXCLK in TMRnCN), as follows:

TnMH	TnXCLK	TMRnH Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

TnML	TnXCLK	TMRnL Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

The TFnH bit is set when TMRnH overflows from 0xFF to 0x00; the TFnL bit is set when TMRnL overflows from 0xFF to 0x00. When timer interrupts are enabled, an interrupt is generated each time TMRnH overflows. If timer interrupts are enabled and TFnLEN is set, an interrupt is generated each time either TMRnL or TMRnH overflows. When TFnLEN is enabled, software must check the TFnH and TFnL flags to determine the source of the timer interrupt. The TFnH and TFnL interrupt flags are not cleared by hardware and must be manually cleared by software.

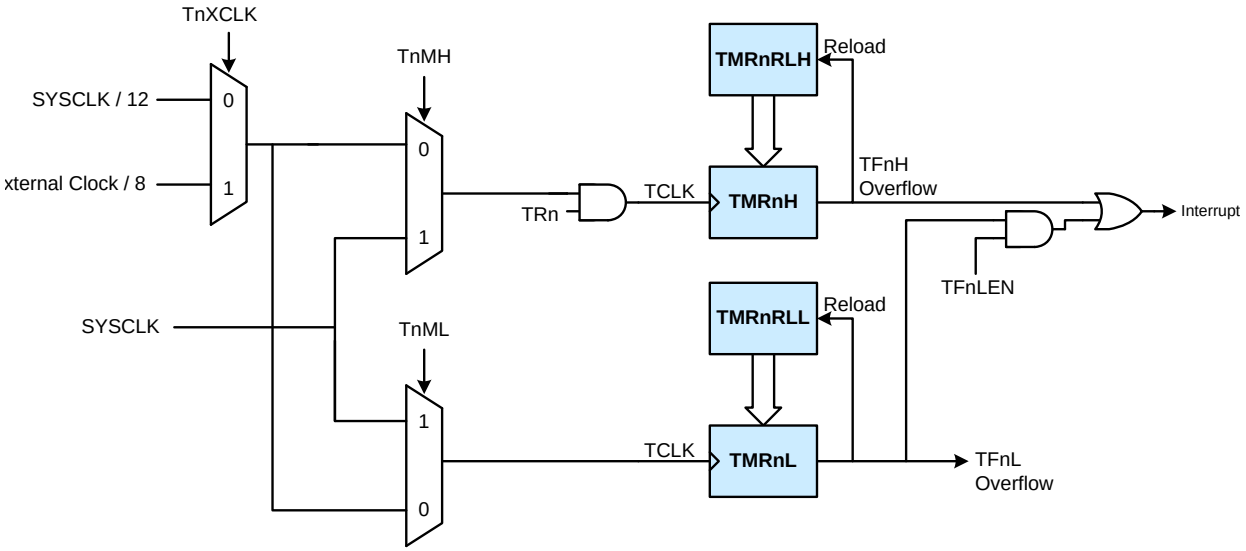

Figure 25.5. 8-Bit Mode Block Diagram

29.2. C2 Interface Registers

The following describes the C2 registers necessary to perform flash programming through the C2 interface. All C2 registers are accessed through the C2 interface, and are not available in the SFR map for firmware access.

Register 29.1. C2ADD: C2 Address

Bit	7	6	5	4	3	2	1	0
Name	C2ADD							
Type	RW							
Reset	0	0	0	0	0	0	0	0
This register is part of the C2 protocol.								

Table 29.1. C2ADD Register Bit Descriptions

Bit	Name	Function
7:0	C2ADD	**C2 Address.** The C2ADD register is accessed via the C2 interface. The value written to C2ADD selects the target data register for C2 Data Read and Data Write commands. 0x00: C2DEVID 0x01: C2REVID 0x02: C2FPCTL 0xB4: C2FPDAT