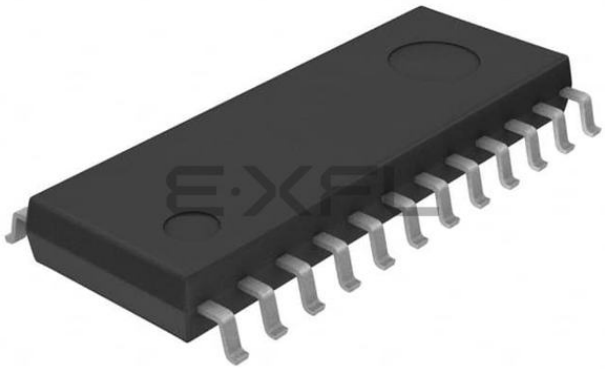

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f852-c-gu

1. Electrical Specifications

1.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 1.1, unless stated otherwise.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.2	—	3.6	V
System Clock Frequency	f_{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T_A	Commercial Grade Devices (-GM, -GS, -GU)	–40	—	85	°C
		Industrial Grade Devices (-IM, -IS, -IU)	–40	—	125	°C
Note: All voltages with respect to GND						

Table 1.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (–Gx Devices, -40°C to +85°C)						
Normal Mode—Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 24.5 MHz[2]	—	4.45	4.85	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	915	1150	µA
		F_{SYSCLK} = 80 kHz[3], T_A = 25 °C	—	250	290	µA
		F_{SYSCLK} = 80 kHz[3]	—	250	380	µA
Idle Mode—Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 24.5 MHz[2]	—	2.05	2.3	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	550	700	µA
		F_{SYSCLK} = 80 kHz[3], T_A = 25 °C	—	125	130	µA
		F_{SYSCLK} = 80 kHz[3]	—	125	200	µA
Stop Mode—Core halted and all clocks stopped, Supply monitor off.	I_{DD}	Internal LDO ON, T_A = 25 °C	—	105	120	µA
		Internal LDO ON	—	105	170	µA
		Internal LDO OFF	—	0.2	—	µA

Notes:
1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

1.2.3. Port I/O Output Drive

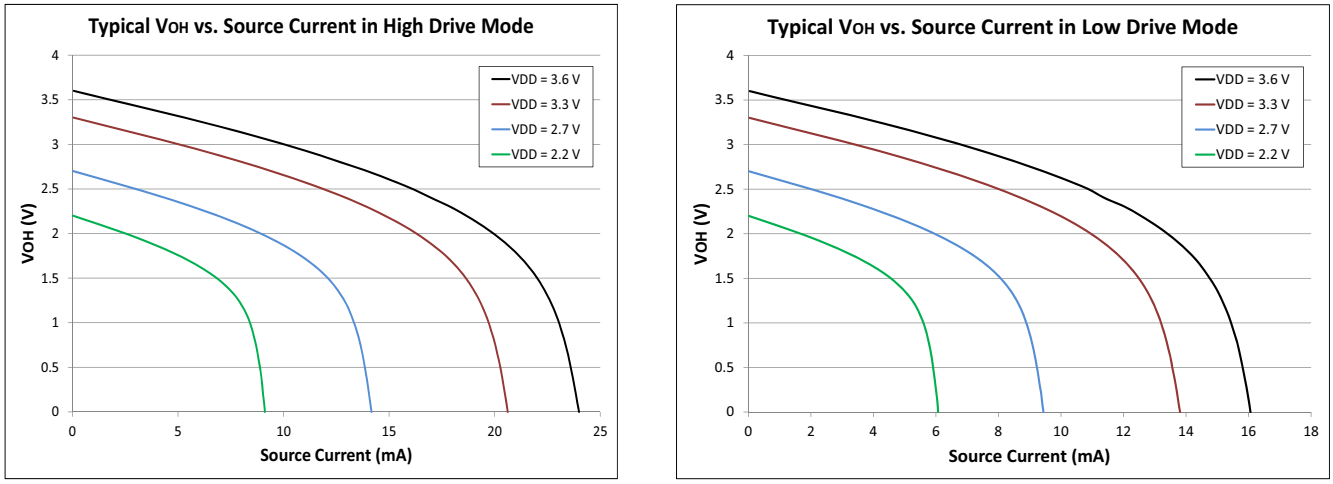

Figure 1.5. Typical V_{OH} vs. Source Current

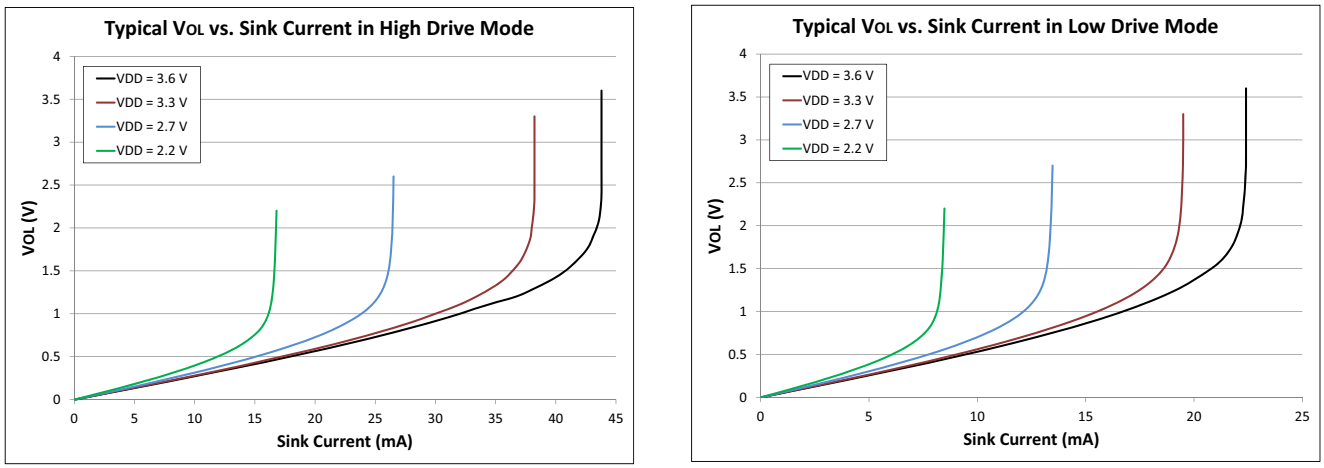

Figure 1.6. Typical V_{OL} vs. Sink Current

1.3. Thermal Conditions

Table 1.12. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	SOIC-16 Packages	—	70	—	°C/W
		QFN-20 Packages	—	60	—	°C/W
		QSOP-24 Packages	—	65	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

3.3. C8051F860/1/2/3/4/5 SOIC16 Pin Definitions

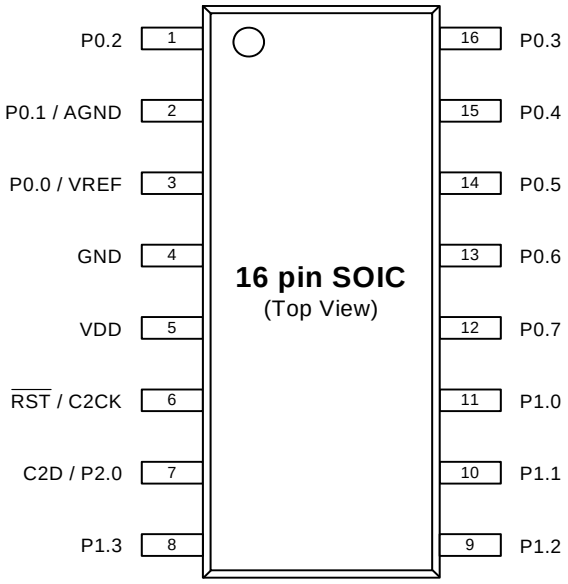

Figure 3.3. C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS Pinout

Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	4			
VDD	Power	5			
RST / C2CK	Active-low Reset / C2 Debug Clock	6			
P0.0	Standard I/O	3	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0

Table 17.3. CMP1 Positive Input Multiplexer Channels

CMXP Setting in Register CPT1MX	Signal Name	QSOP24 Pin Name	QFN20 Pin Name	SOIC16 Pin Name
0000	CP1P.0	P1.0	P1.0	P0.6
0001	CP1P.1	P1.1	P1.1	P0.7
0010	CP1P.2	P1.2	P1.2	P1.0
0011	CP1P.3	P1.3	P1.3	P1.1
0100	CP1P.4	P1.4	P1.4	P1.2
0101	CP1P.5	P1.5	P1.5	P1.3
0110	CP1P.6	P1.6	P1.6	Reserved
0111	CP1P.7	P1.7	Reserved	Reserved
1000	LDO	Internal 1.8 V LDO Output		
1001-1111	None	No connection		

Table 17.4. CMP1 Negative Input Multiplexer Channels

CMXN Setting in Register CPT1MX	Signal Name	QSOP24 Pin Name	QFN20 Pin Name	SOIC16 Pin Name
0000	CP1N.0	P1.0	P1.0	P0.6
0001	CP1N.1	P1.1	P1.1	P0.7
0010	CP1N.2	P1.2	P1.2	P1.0
0011	CP1N.3	P1.3	P1.3	P1.1
0100	CP1N.4	P1.4	P1.4	P1.2
0101	CP1N.5	P1.5	P1.5	P1.3
0110	CP1N.6	P1.6	P1.6	Reserved
0111	CP1N.7	P1.7	Reserved	Reserved
1000	GND	GND		
1001-1111	None	No connection		

17.2. Functional Description

The comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the port pins: a synchronous “latched” output (CPn), or an asynchronous “raw” output (CPnA). The asynchronous CPnA signal is available even when the system clock is not active. This allows the comparator to operate and generate an output with the device in STOP mode.

When disabled, the comparator output (if assigned to a port I/O pin via the crossbar) defaults to the logic low state, and the power supply to the comparator is turned off.

The comparator response time may be configured in software via the CPTnMD register. Selecting a longer response time reduces the comparator supply current.

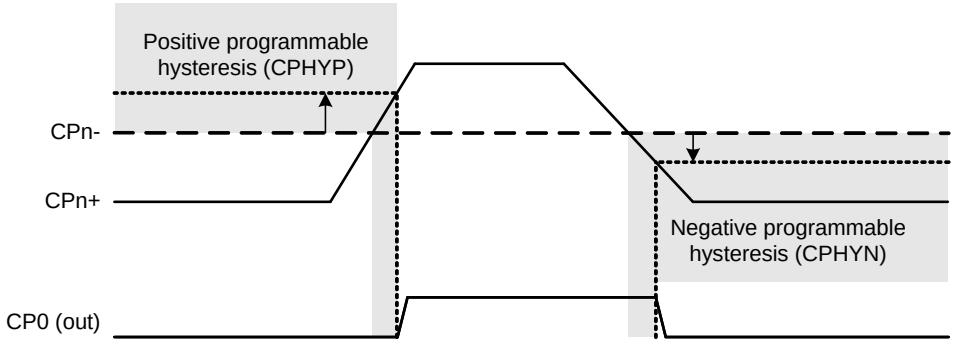

Figure 17.2. Comparator Hysteresis Plot

The comparator hysteresis is software-programmable via its Comparator Control register CPTnCN. The user can program both the amount of hysteresis voltage (referred to the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage.

The comparator hysteresis is programmable using the CPHYN and CPHYP fields in the Comparator Control Register CPTnCN. The amount of negative hysteresis voltage is determined by the settings of the CPHYN bits. As shown in Figure 17.2, settings of 20, 10, or 5 mV (nominal) of negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of positive hysteresis is determined by the setting the CPHYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. The CPFIF flag is set to logic 1 upon a comparator falling-edge occurrence, and the CPRIF flag is set to logic 1 upon the comparator rising-edge occurrence. Once set, these bits remain set until cleared by software. The comparator rising-edge interrupt mask is enabled by setting CPRIE to a logic 1. The comparator falling-edge interrupt mask is enabled by setting CPFIE to a logic 1.

The output state of the comparator can be obtained at any time by reading the CPOUT bit. The comparator is enabled by setting the CPEN bit to logic 1, and is disabled by clearing this bit to logic 0.

Note that false rising edges and falling edges can be detected when the comparator is first powered on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed, before enabling comparator interrupts.

Register 17.2. CPT0MD: Comparator 0 Mode

Bit	7	6	5	4	3	2	1	0
Name	CPLOUT	Reserved	CPRIE	CPFIE	Reserved		CPMD	
Type	RW	R	RW	RW	R		RW	
Reset	0	0	0	0	0	0	1	0
SFR Address: 0x9D								

Table 17.6. CPT0MD Register Bit Descriptions

Bit	Name	Function
7	CPLOUT	**Comparator 0 Latched Output Flag.** This bit represents the comparator output value at the most recent PCA counter overflow. 0: Comparator output was logic low at last PCA overflow. 1: Comparator output was logic high at last PCA overflow.
6	Reserved	Must write reset value.
5	CPRIE	**Comparator 0 Rising-Edge Interrupt Enable.** 0: Comparator Rising-Edge interrupt disabled. 1: Comparator Rising-Edge interrupt enabled.
4	CPFIE	**Comparator 0 Falling-Edge Interrupt Enable.** 0: Comparator Falling-Edge interrupt disabled. 1: Comparator Falling-Edge interrupt enabled.
3:2	Reserved	Must write reset value.
1:0	CPMD	**Comparator 0 Mode Select.** These bits affect the response time and power consumption of the comparator. 00: Mode 0 (Fastest Response Time, Highest Power Consumption) 01: Mode 1 10: Mode 2 11: Mode 3 (Slowest Response Time, Lowest Power Consumption)

18.6. CRC Control Registers

Register 18.1. CRC0CN: CRC0 Control

Bit	7	6	5	4	3	2	1	0
Name	Reserved				CRCINIT	CRCVAL	Reserved	CRCPNT
Type	R				RW	RW	R	RW
Reset	0	0	0	1	0	0	0	0
SFR Address: 0xCE								

Table 18.2. CRC0CN Register Bit Descriptions

Bit	Name	Function
7:4	Reserved	Must write reset value.
3	CRCINIT	**CRC Result Initialization Bit.** Writing a 1 to this bit initializes the entire CRC result based on CRCVAL.
2	CRCVAL	**CRC Set Value Initialization Bit.** This bit selects the set value of the CRC result. 0: CRC result is set to 0x0000 on write of 1 to CRCINIT. 1: CRC result is set to 0xFFFF on write of 1 to CRCINIT.
1	Reserved	Must write reset value.
0	CRCPNT	**CRC Result Pointer.** Specifies the byte of the CRC result to be read/written on the next access to CRC0DAT. This bit will automatically toggle upon each read or write. 0: CRC0DAT accesses bits 7-0 of the 16-bit CRC result. 1: CRC0DAT accesses bits 15-8 of the 16-bit CRC result.
Note: Upon initiation of an automatic CRC calculation, the three cycles following a write to CRC0CN that initiate a CRC operation must only contain instructions which execute in the same number of cycles as the number of bytes in the instruction. An example of such an instruction is a 3-byte MOV that targets the CRC0FLIP register. When programming in C, the dummy value written to CRC0FLIP should be a non-zero value to prevent the compiler from generating a 2-byte MOV instruction.		

20.3.2. Edge-Triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

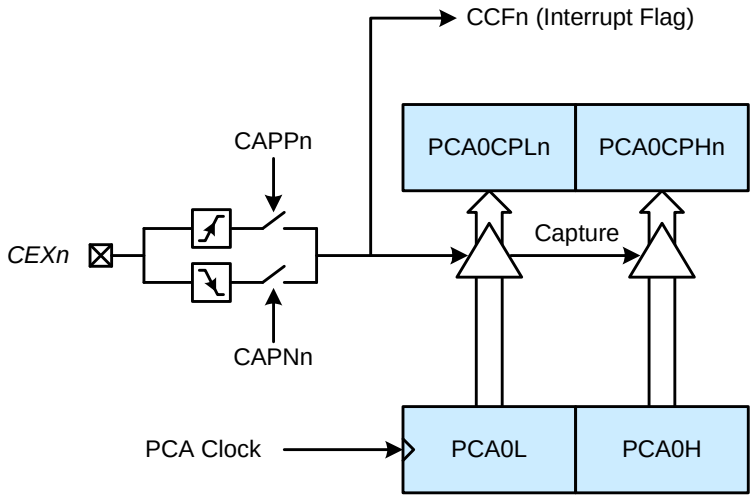

Figure 20.2. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

Register 20.5. PCA0CPM0: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xDA								

Table 20.7. PCA0CPM0 Register Bit Descriptions

Bit	Name	Function
7	PWM16	**16-bit Pulse Width Modulation Enable.** This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected. 1: 16-bit PWM selected.
6	ECOM	**Comparator Function Enable.** This bit enables the comparator function.
5	CAPP	**Capture Positive Function Enable.** This bit enables the positive edge capture capability.
4	CAPN	**Capture Negative Function Enable.** This bit enables the negative edge capture capability.
3	MAT	**Match Function Enable.** This bit enables the match function. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCF0 bit in the PCA0MD register to be set to logic 1.
2	TOG	**Toggle Function Enable.** This bit enables the toggle function. When enabled, matches of the PCA counter with the capture/compare register cause the logic level on the CEX0 pin to toggle. If the PWM bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWM	**Pulse Width Modulation Mode Enable.** This bit enables the PWM function. When enabled, a pulse width modulated signal is output on the CEX0 pin. 8 to 11-bit PWM is used if PWM16 is cleared; 16-bit mode is used if PWM16 is set to logic 1. If the TOG bit is also set, the module operates in Frequency Output Mode.
0	ECCF	**Capture/Compare Flag Interrupt Enable.** This bit sets the masking of the Capture/Compare Flag (CCF0) interrupt. 0: Disable CCF0 interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCF0 is set.

21.4.3. Port Drive Strength

Port drive strength can be controlled on a port-by-port basis using the PRTDRV register. Each port has a bit in PRTDRV to select the high or low drive strength setting for all pins on that port. By default, all ports are configured for high drive strength.

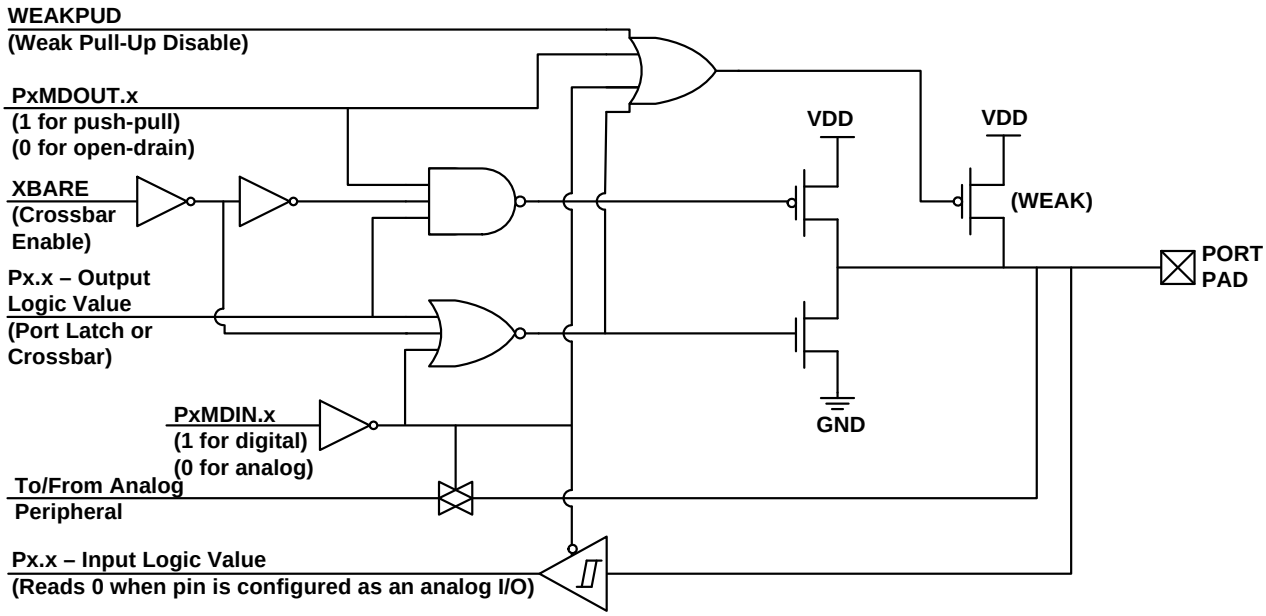

Figure 21.4. Port I/O Cell Block Diagram

21.5. Port Match

Port match functionality allows system events to be triggered by a logic value change on one or more port I/O pins. A software controlled value stored in the PnMATCH registers specifies the expected or normal logic values of the associated port pins (for example, P0MATCH.0 would correspond to P0.0). A port mismatch event occurs if the logic levels of the port's input pins no longer match the software controlled value. This allows software to be notified if a certain change or pattern occurs on the input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which pins should be compared against the PnMATCH registers. A port mismatch event is generated if (Pn & PnMASK) does not equal (PnMATCH & PnMASK) for all ports with a PnMAT and PnMASK register.

A port mismatch event may be used to generate an interrupt or wake the device from idle mode. See the interrupts and power options chapters for more details on interrupt and wake-up sources.

21.6. Direct Read/Write Access to Port I/O Pins

All port I/O are accessed through corresponding special function registers (SFRs) that are both byte addressable and bit addressable. When writing to a port, the value written to the SFR is latched to maintain the output data value at each pin. When reading, the logic levels of the port's input pins are returned regardless of the XBRn settings (i.e., even when the pin is assigned to another signal by the crossbar, the port register can always read its corresponding port I/O pin). The exception to this is the execution of the read-modify-write instructions that target a Port Latch register as the destination. The read-modify-write instructions when operating on a port SFR are the following: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ and MOV, CLR or SETB, when the destination is an individual bit in a port SFR. For these instructions, the value of the latch register (not the pin) is read, modified, and written back to the SFR.

Register 21.7. P0: Port 0 Pin Latch

Bit	7	6	5	4	3	2	1	0
Name	P0							
Type	RW							
Reset	1	1	1	1	1	1	1	1
SFR Address: 0x80 (bit-addressable)								

Table 21.10. P0 Register Bit Descriptions

Bit	Name	Function
7:0	P0	**Port 0 Data.** Writing this register sets the port latch logic value for the associated I/O pins configured as digital I/O. Reading this register returns the logic value at the pin, regardless if it is configured as output or input.

22.2. Power-Fail Reset / Supply Monitor

C8051F85x/86x devices have a supply monitor that is enabled and selected as a reset source after each power-on.

The supply monitor senses the voltage on the device VDD supply and can generate a reset if the supply drops below the corresponding threshold. This monitor is enabled and enabled as a reset source after initial power-on to protect the device until VDD is an adequate and stable voltage.

When enabled and selected as a reset source, any power down transition or power irregularity that causes VDD to drop below the reset threshold will drive the $\overline{\text{RST}}$ pin low and hold the core in a reset state. When VDD returns to a level above the reset threshold, the monitor will release the core from the reset state. The reset status can then be read using the device reset sources module. After a power-fail reset, the PORF flag reads 1 and all of the other reset flags in the RSTSRC Register are indeterminate. The power-on reset delay (t_{POR}) is not incurred after a supply monitor reset. The contents of RAM should be presumed invalid after a VDD monitor reset.

The enable state of the VDD supply monitor and its selection as a reset source is not altered by device resets. For example, if the VDD supply monitor is de-selected as a reset source and disabled by software, and then firmware performs a software reset, the VDD supply monitor will remain disabled and de-selected after the reset.

To protect the integrity of flash contents, the VDD supply monitor must be enabled and selected as a reset source if software contains routines that erase or write flash memory. If the VDD supply monitor is not enabled, any erase or write performed on flash memory will be ignored.

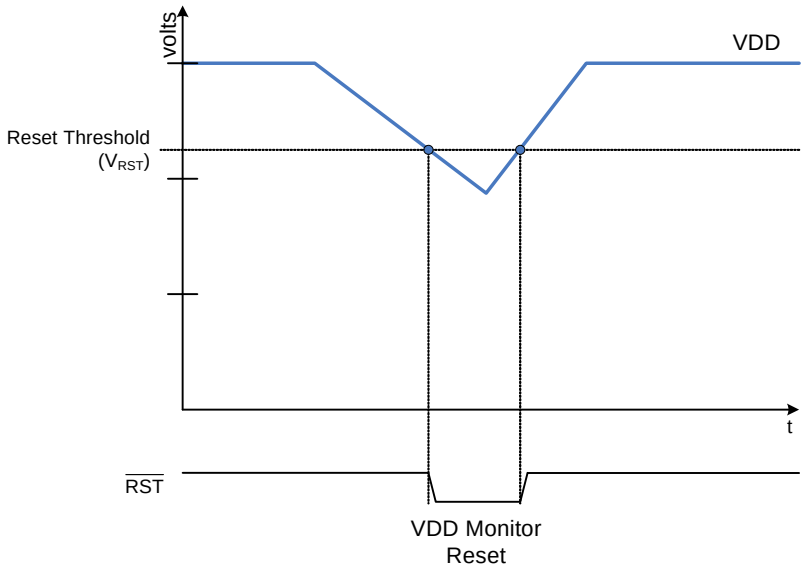

Figure 22.3. VDD Supply Monitor Threshold

22.3. Enabling the VDD Monitor

The VDD supply monitor is enabled by default. However, in systems which disable the supply monitor, it must be enabled before selecting it as a reset source. Selecting the VDD supply monitor as a reset source before it has stabilized may generate a system reset. In systems where this reset would be undesirable, a delay should be introduced between enabling the VDD supply monitor and selecting it as a reset source. No delay should be introduced in systems where software contains routines that erase or write flash memory. The procedure for enabling the VDD supply monitor and selecting it as a reset source is:

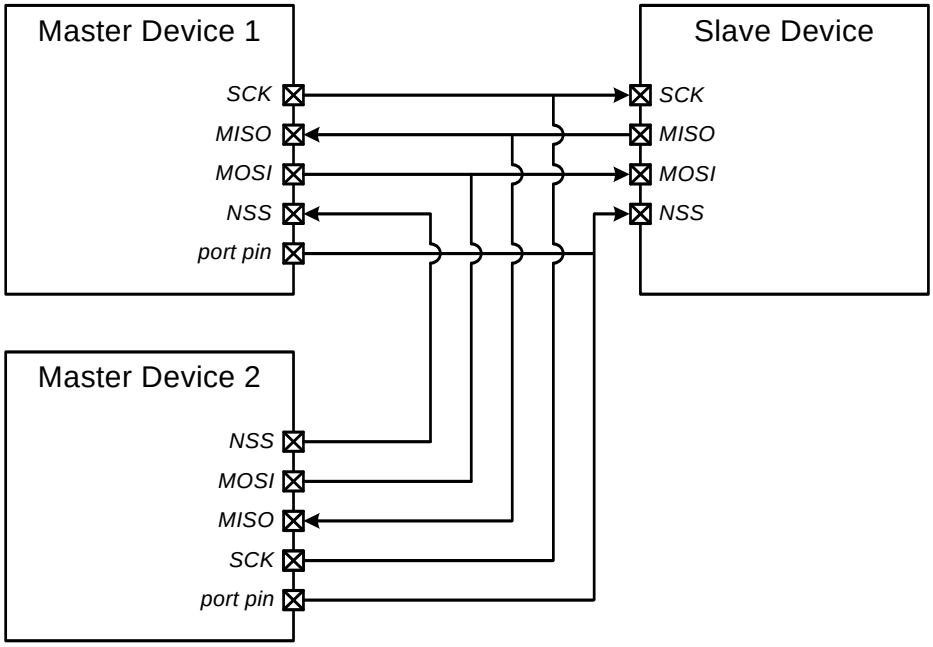

Figure 23.2. Multiple-Master Mode Connection Diagram

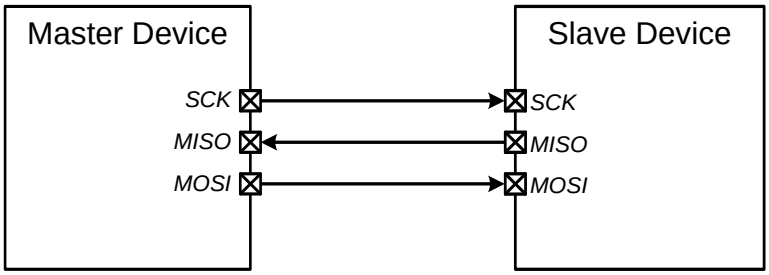

Figure 23.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram

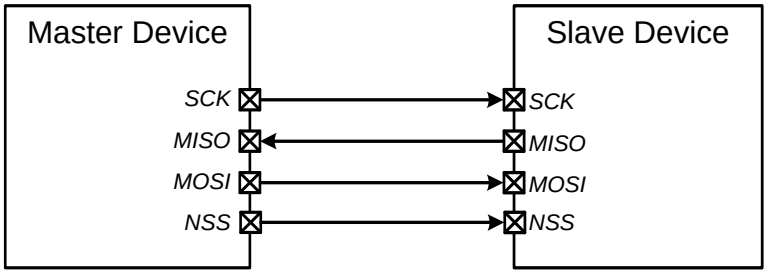

Figure 23.4. 4-Wire Single Master Mode and 4-Wire Slave Mode Connection Diagram

24.5.2. Read Sequence (Master)

During a read sequence, an SMBus master reads data from a slave device. The master in this transfer will be a transmitter during the address byte, and a receiver during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 1 (READ). Serial data is then received from the slave on SDA while the SMBus outputs the serial clock. The slave transmits one or more bytes of serial data.

If hardware ACK generation is disabled, the ACKRQ is set to 1 and an interrupt is generated after each received byte. Software must write the ACK bit at that time to ACK or NACK the received byte.

With hardware ACK generation enabled, the SMBus hardware will automatically generate the ACK/NACK, and then post the interrupt. **It is important to note that the appropriate ACK or NACK value should be set up by the software prior to receiving the byte when hardware ACK generation is enabled.**

Writing a 1 to the ACK bit generates an ACK; writing a 0 generates a NACK. Software should write a 0 to the ACK bit for the last data transfer, to transmit a NACK. The interface exits Master Receiver Mode after the STO bit is set and a STOP is generated. The interface will switch to Master Transmitter Mode if SMB0DAT is written while an active Master Receiver. Figure 24.6 shows a typical master read sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the ‘data byte transferred’ interrupts occur at different places in the sequence, depending on whether hardware ACK generation is enabled. The interrupt occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled.

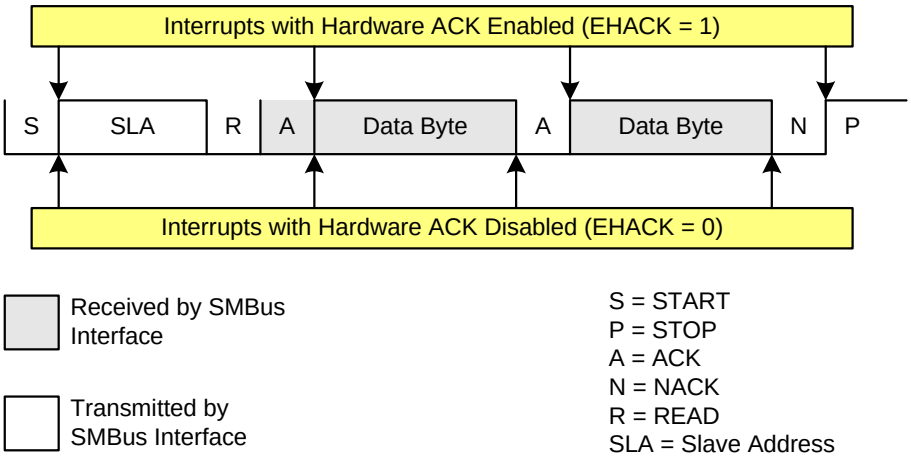

Figure 24.6. Typical Master Read Sequence

Table 24.6. SMBus Status Decoding: Hardware ACK Enabled (EHACK = 1) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Receiver	1000	0	0	1	A master data byte was received; ACK sent.	Set ACK for next data byte; Read SMB0DAT.	0	0	1	1000
						Set NACK to indicate next data byte as the last data byte; Read SMB0DAT.	0	0	0	1000
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100
		0	0	0	A master data byte was received; NACK sent (last byte).	Read SMB0DAT; send STOP.	0	1	0	—
						Read SMB0DAT; Send STOP followed by START.	1	1	0	1110
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	—

Table 24.6. SMBus Status Decoding: Hardware ACK Enabled (EHACK = 1) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Slave Receiver	0010	0	0	X	A slave address + R/W was received; ACK sent.	If Write, Set ACK for first data byte.	0	0	1	0000
						If Read, Load SMB0DAT with data byte	0	0	X	0100
		0	1	X	Lost arbitration as master; slave address + R/W received; ACK sent.	If Write, Set ACK for first data byte.	0	0	1	0000
						If Read, Load SMB0DAT with data byte	0	0	X	0100
						Reschedule failed transfer	1	0	X	1110
	0001	0	0	X	A STOP was detected while addressed as a Slave Transmitter or Slave Receiver.	Clear STO.	0	0	X	—
		0	1	X	Lost arbitration while attempting a STOP.	No action required (transfer complete/aborted).	0	0	0	—
	0000	0	0	X	A slave byte was received.	Set ACK for next data byte; Read SMB0DAT.	0	0	1	0000
						Set NACK for next data byte; Read SMB0DAT.	0	0	0	0000
Bus Error Condition	0010	0	1	X	Lost arbitration while attempting a repeated START.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110
	0001	0	1	X	Lost arbitration due to a detected STOP.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110
	0000	0	1	X	Lost arbitration while transmitting a data byte as master.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110

25.2.3. Capture Mode

Capture mode allows an external input (Timer 2) or the low-frequency oscillator clock (Timer 3) to be measured against the system clock or an external oscillator source. The timer can be clocked from the system clock, the system clock divided by 12, or the external oscillator divided by 8, depending on the TnML, and TnXCLK settings.

Setting TFnCEN to 1 enables Capture Mode. In this mode, TnSPLIT should be set to 0, as the full 16-bit timer is used. Upon a falling edge of the input capture signal, the contents of the timer register (TMRnH:TMRnL) are loaded into the reload registers (TMRnRLH:TMRnRLL) and the TFnH flag is set. By recording the difference between two successive timer capture values, the period of the captured signal can be determined with respect to the selected timer clock.

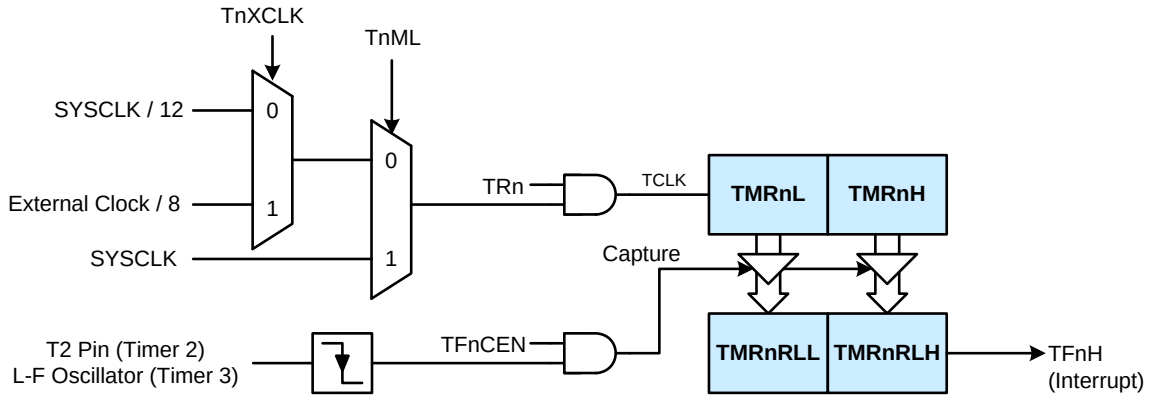

Figure 25.6. Capture Mode Block Diagram

26.4. UART Control Registers

Register 26.1. SCON0: UART0 Serial Port Control

Bit	7	6	5	4	3	2	1	0
Name	SMODE	Reserved	MCE	REN	TB8	RB8	TI	RI
Type	RW	R	RW	RW	RW	RW	RW	RW
Reset	0	1	0	0	0	0	0	0
SFR Address: 0x98 (bit-addressable)								

Table 26.2. SCON0 Register Bit Descriptions

Bit	Name	Function
7	SMODE	**Serial Port 0 Operation Mode.** Selects the UART0 Operation Mode. 0: 8-bit UART with Variable Baud Rate (Mode 0). 1: 9-bit UART with Variable Baud Rate (Mode 1).
6	Reserved	Must write reset value.
5	MCE	**Multiprocessor Communication Enable.** This bit enables checking of the stop bit or the 9th bit in multi-drop communication buses. The function of this bit is dependent on the UART0 operation mode selected by the SMODE bit. In Mode 0 (8-bits), the peripheral will check that the stop bit is logic 1. In Mode 1 (9-bits) the peripheral will check for a logic 1 on the 9th bit. 0: Ignore level of 9th bit / Stop bit. 1: RI is set and an interrupt is generated only when the stop bit is logic 1 (Mode 0) or when the 9th bit is logic 1 (Mode 1).
4	REN	**Receive Enable.** 0: UART0 reception disabled. 1: UART0 reception enabled.
3	TB8	**Ninth Transmission Bit.** The logic level of this bit will be sent as the ninth transmission bit in 9-bit UART Mode (Mode 1). Unused in 8-bit mode (Mode 0).
2	RB8	**Ninth Receive Bit.** RB8 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.
1	TI	**Transmit Interrupt Flag.** Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

28. Revision-Specific Behavior

C8051F85x/86x Revision B devices have differences from Revision C devices:

- Temperature Sensor offset and slope
- Flash endurance
- Latch-up performance
- Unique Identifier

28.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figure 28.1, Figure 28.2, and Figure 28.3 show how to find the Lot ID Code on the top side of the device package.

Firmware can distinguish between a Revision B and Revision C device using the value of the REVID register described in “Device Identification and Unique Identifier” on page 68.

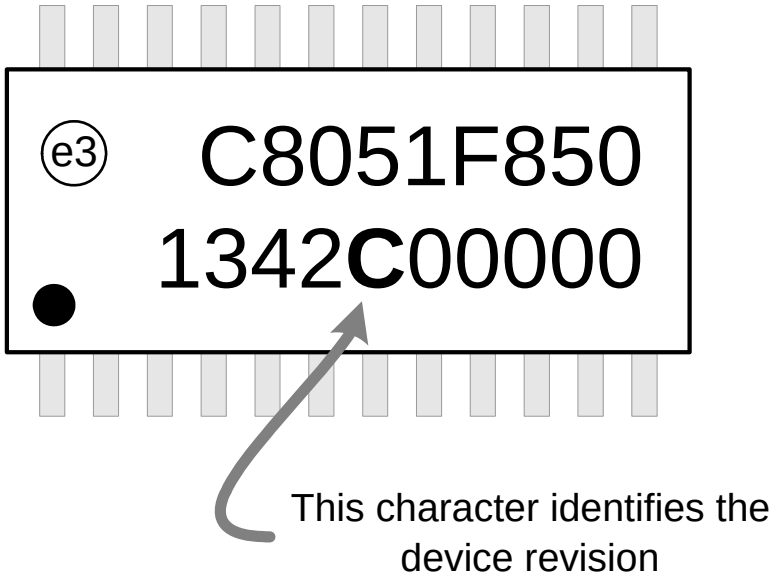

Figure 28.1. QSOP-24 Package Revision Marking

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 0.6

- Updated front page block diagram.
- Updated ADC supply current parameters in Table 1.2, “Power Consumption,” on page 8.
- Corrected flash programming voltage range in "Table 1.4. Flash Memory" on page 11.
- Added ADC Power-On Time specification in Table 1.7, “ADC,” on page 13.
- Added section "1.2. Typical Performance Curves" on page 19.
- Corrected DERIVID Information in Table 11.3, “DERIVID Register Bit Descriptions,” on page 70.
- Updated ADC chapter ("14. Analog-to-Digital Converter (ADC0)" on page 85) and expanded section "14.5. Power Considerations" on page 85 with recommended power configuration settings.
- Updated Figure 21.1, “Port I/O Functional Block Diagram,” on page 184.
- Corrected reset value in Register 24.5, “SMB0ADM: SMBus0 Slave Address Mask,” on page 257.
- Corrected description of IE0 in "Table 25.4. TCON Register Bit Descriptions" on page 259.

Revision 0.6 to Revision 0.7

- Added mention of the UID to the front page.
- Updated some TBD values in the "1. Electrical Specifications" on page 8 section.
- Updated Power-On Reset (POR) Threshold maximum Falling Voltage on V_{DD} specification in Table 1.3.
- Updated Reset Delay from non-POR source typical specification in Table 1.3.
- Removed V_{DD} Ramp Time maximum specification in Table 1.3.
- Updated Flash Memory Erase Time specification and added Note 2 to Table 1.4.
- Updated maximum ADC DC performance specifications in Table 1.7.
- Updated minimum and maximum ADC offset error and slope error specifications in Table 1.7.
- Updated conditions on Internal Fast Settling Reference Output Voltage (Full Temperature and Supply Range) in Table 1.8.
- Added a new section "1.2.3. Port I/O Output Drive" on page 21.
- Updated pinout Figure 3.1, Figure 3.2, Figure 3.3, Table 3.1, Table 3.2, and Table 3.3 titles to the correct part numbers.
- Updated the Ordering Information ("4. Ordering Information" on page 42.) for Revision C devices.
- Added mention of the unique identifier to "8. Memory Organization" on page 52.
- Added unique identifier information to "11. Device Identification and Unique Identifier" on page 68.
- Updated device part numbers listed in Table 11.3, “DERIVID Register Bit Descriptions,” on page 70 to include the revision.
- Added "28. Revision-Specific Behavior" on page 301.

Revision 0.7 to Revision 1.0

- Updated Digital Core, ADC, and Temperature Sensor electrical specifications information for -I devices.
- Updated -I part number information in "4. Ordering Information" on page 42.
- Replaced reference to AMX0P and AMX0N with ADC0MX in Table 21.1, “Port I/O Assignment for Analog Functions,” on page 186.
- Added a note to Table 1.13, “Absolute Maximum Ratings,” on page 22 and added a link to the Quality and Reliability Monitor Report.
- Added Operating Junction Temperature to Table 1.13, “Absolute Maximum Ratings,” on page 22.
- Updated all TBDs in "1. Electrical Specifications" on page 8.