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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f852-c-iur

Table 1.8. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, $V_{DD} \geq 2.6$ V	2.35	2.4	2.45	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 800 ksps; VREF = 3.0 V	—	5	—	µA

Table 1.9. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	757	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	17	—	mV
Slope	M		—	2.85	—	mV/°C
Slope Error*	E_M		—	70	—	µV/°C
Linearity			—	0.5	—	°C
Turn-on Time			—	1.8	—	µs
***Note:** Represents one standard deviation from the mean.						

3.3. C8051F860/1/2/3/4/5 SOIC16 Pin Definitions

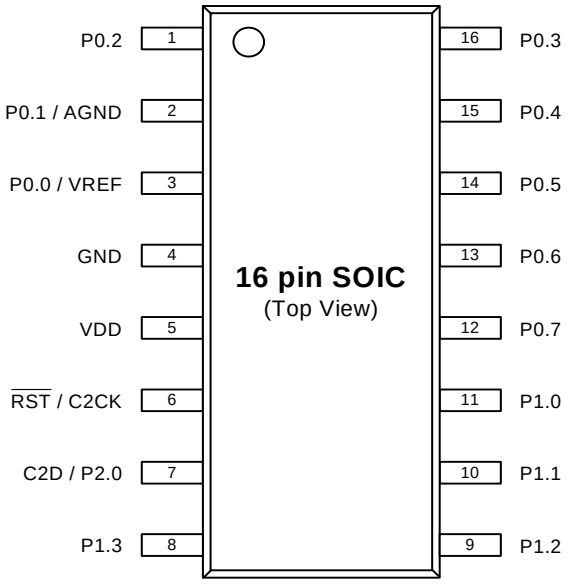


Figure 3.3. C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS Pinout

Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	4			
VDD	Power	5			
RST / C2CK	Active-low Reset / C2 Debug Clock	6			
P0.0	Standard I/O	3	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0

8.1. Program Memory

The CIP-51 core has a 64 kB program memory space. The C8051F85x/86x family implements 8 kB, 4 kB or 2 kB of this program memory space as in-system, re-programmable flash memory. The last address in the flash block (0x1FFF on 8 kB devices, 0x0FFF on 4 kB devices and 0x07FF on 2 kB devices) serves as a security lock byte for the device, and provides read, write and erase protection. Addresses above the lock byte within the 64 kB address space are reserved.

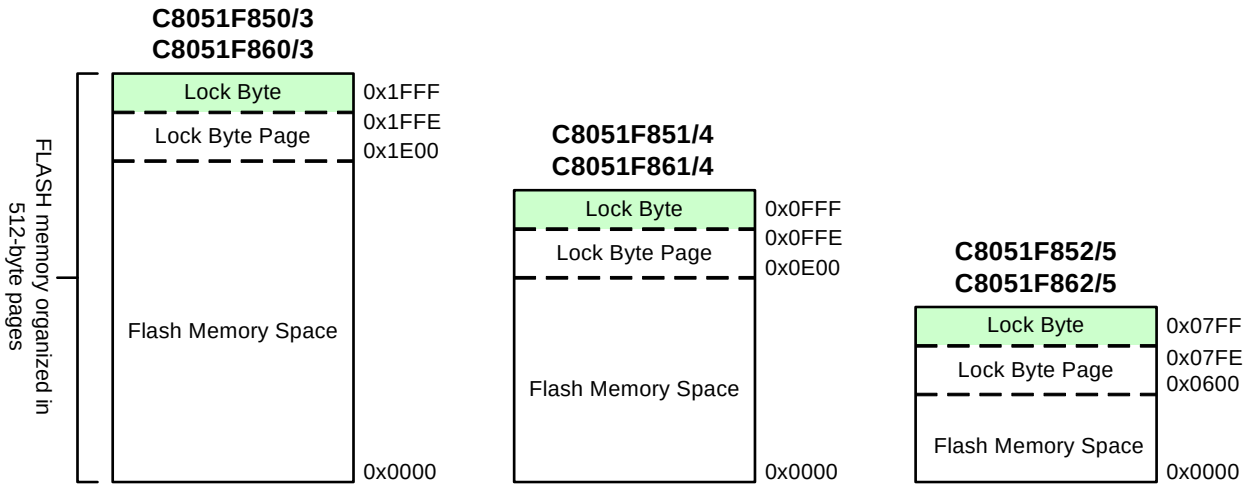


Figure 8.2. Flash Program Memory Map

8.1.1. MOVX Instruction and Program Memory

The MOVX instruction in an 8051 device is typically used to access external data memory. On the C8051F85x/86x devices, the MOVX instruction is normally used to read and write on-chip XRAM, but can be re-configured to write and erase on-chip flash memory space. MOVC instructions are always used to read flash memory, while MOVX write instructions are used to erase and write flash. This flash access feature provides a mechanism for the C8051F85x/86x to update program code and use the program memory space for non-volatile data storage. Refer to Section “10. Flash Memory” on page 61 for further details.

8.2. Data Memory

The C8051F85x/86x device family includes up to 512 bytes of RAM data memory. 256 bytes of this memory is mapped into the internal RAM space of the 8051. On devices with 512 bytes total RAM, 256 additional bytes of memory are available as on-chip “external” memory. The data memory map is shown in Figure 8.1 for reference.

8.2.1. Internal RAM

There are 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

8.2.3. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the CIP-51's resources and peripherals. The CIP-51 duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided.

Table 9.2. Special Function Registers (Continued)

Register	Address	Register Description	Page
ADC0L	0xBD	ADC0 Data Word Low Byte	106
ADC0LTH	0xC6	ADC0 Less-Than High Byte	109
ADC0LTL	0xC5	ADC0 Less-Than Low Byte	110
ADC0MX	0xBB	ADC0 Multiplexer Selection	111
ADC0PWR	0xDF	ADC0 Power Control	103
ADC0TK	0xB9	ADC0 Burst Mode Track Time	104
B	0xF0	B Register	123
CKCON	0x8E	Clock Control	269
CLKSEL	0xA9	Clock Selection	129
CPT0CN	0x9B	Comparator 0 Control	134
CPT0MD	0x9D	Comparator 0 Mode	135
CPT0MX	0x9F	Comparator 0 Multiplexer Selection	136
CPT1CN	0xBF	Comparator 1 Control	137
CPT1MD	0xAB	Comparator 1 Mode	138
CPT1MX	0xAA	Comparator 1 Multiplexer Selection	139
CRC0AUTO	0xD2	CRC0 Automatic Control	146
CRC0CN	0xCE	CRC0 Control	143
CRC0CNT	0xD3	CRC0 Automatic Flash Sector Count	147
CRC0DAT	0xDE	CRC0 Data Output	145
CRC0FLIP	0xCF	CRC0 Bit Flip	148
CRC0IN	0xDD	CRC0 Data Input	144
DERIVID	0xAD	Derivative Identification	70
DEVICEID	0xB5	Device Identification	69
DPH	0x83	Data Pointer Low	120
DPL	0x82	Data Pointer High	119
EIE1	0xE6	Extended Interrupt Enable 1	78
EIP1	0xF3	Extended Interrupt Priority 1	80
FLKEY	0xB7	Flash Lock and Key	67

cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction. If more than one interrupt is pending when the CPU exits an ISR, the CPU will service the next highest priority interrupt that is pending.

12.2. Interrupt Control Registers

Register 12.1. IE: Interrupt Enable

Bit	7	6	5	4	3	2	1	0
Name	EA	ESPI0	ET2	ES0	ET1	EX1	ET0	EX0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xA8 (bit-addressable)								

Table 12.2. IE Register Bit Descriptions

Bit	Name	Function
7	EA	**Enable All Interrupts.** Globally enables/disables all interrupts and overrides individual interrupt mask settings. 0: Disable all interrupt sources. 1: Enable each interrupt according to its individual mask setting.
6	ESPI0	**Enable SPI0 Interrupt.** This bit sets the masking of the SPI0 interrupts. 0: Disable all SPI0 interrupts. 1: Enable interrupt requests generated by SPI0.
5	ET2	**Enable Timer 2 Interrupt.** This bit sets the masking of the Timer 2 interrupt. 0: Disable Timer 2 interrupt. 1: Enable interrupt requests generated by the TF2L or TF2H flags.
4	ES0	**Enable UART0 Interrupt.** This bit sets the masking of the UART0 interrupt. 0: Disable UART0 interrupt. 1: Enable UART0 interrupt.
3	ET1	**Enable Timer 1 Interrupt.** This bit sets the masking of the Timer 1 interrupt. 0: Disable all Timer 1 interrupt. 1: Enable interrupt requests generated by the TF1 flag.
2	EX1	**Enable External Interrupt 1.** This bit sets the masking of External Interrupt 1. 0: Disable external interrupt 1. 1: Enable interrupt requests generated by the INT1 input.
1	ET0	**Enable Timer 0 Interrupt.** This bit sets the masking of the Timer 0 interrupt. 0: Disable all Timer 0 interrupt. 1: Enable interrupt requests generated by the TF0 flag.

13.1.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the controller core to enter stop mode as soon as the instruction that sets the bit completes execution. Before entering stop mode, the system clock must be sourced by the internal high-frequency oscillator. In stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering stop mode. Stop mode can only be terminated by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout.

13.2. LDO Regulator

C8051F85x/86x devices include an internal regulator that regulates the internal core and logic supply. Under default conditions, the internal regulator will remain on when the device enters STOP mode. This allows any enabled reset source to generate a reset for the device and bring the device out of STOP mode. For additional power savings, the STOPCF bit can be used to shut down the regulator and the internal power network of the device when the part enters STOP mode. When STOPCF is set to 1, the $\overline{\text{RST}}$ pin and a full power cycle of the device are the only methods of generating a reset.

13.3. Power Control Registers

Register 13.1. PCON: Power Control

Bit	7	6	5	4	3	2	1	0
Name	GF						STOP	IDLE
Type	RW						RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x87								

Table 13.1. PCON Register Bit Descriptions

Bit	Name	Function
7:2	GF	**General Purpose Flags 5-0.** These are general purpose flags for use under software control.
1	STOP	**Stop Mode Select.** Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0.
0	IDLE	**Idle Mode Select.** Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0.

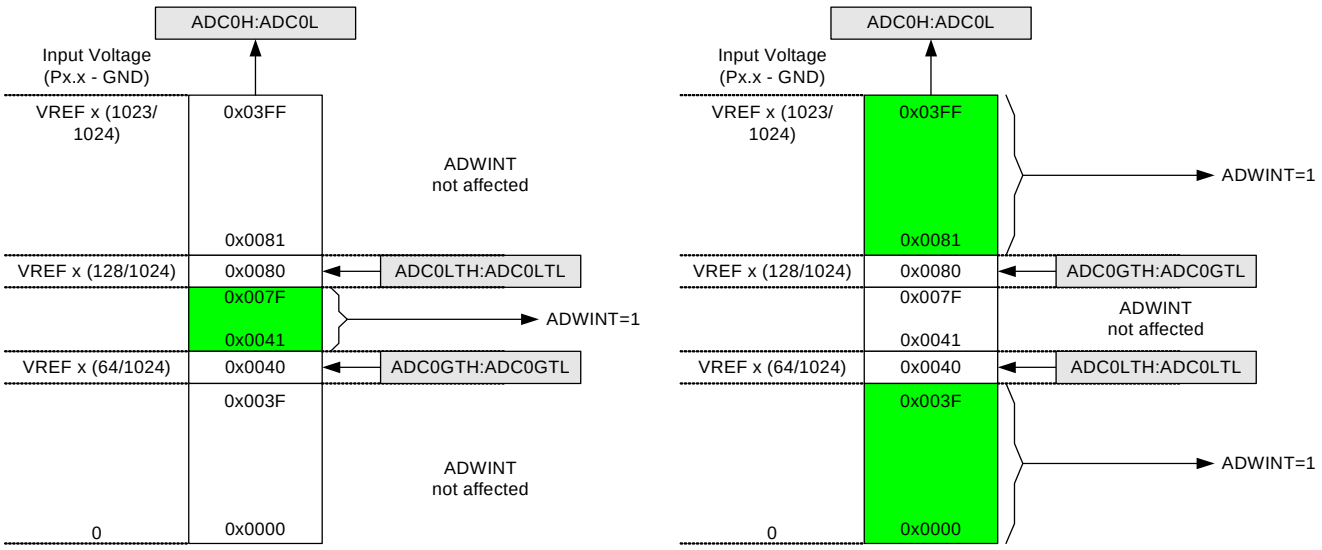


Figure 14.6. ADC Window Compare Example: Right-Justified Single-Ended Data

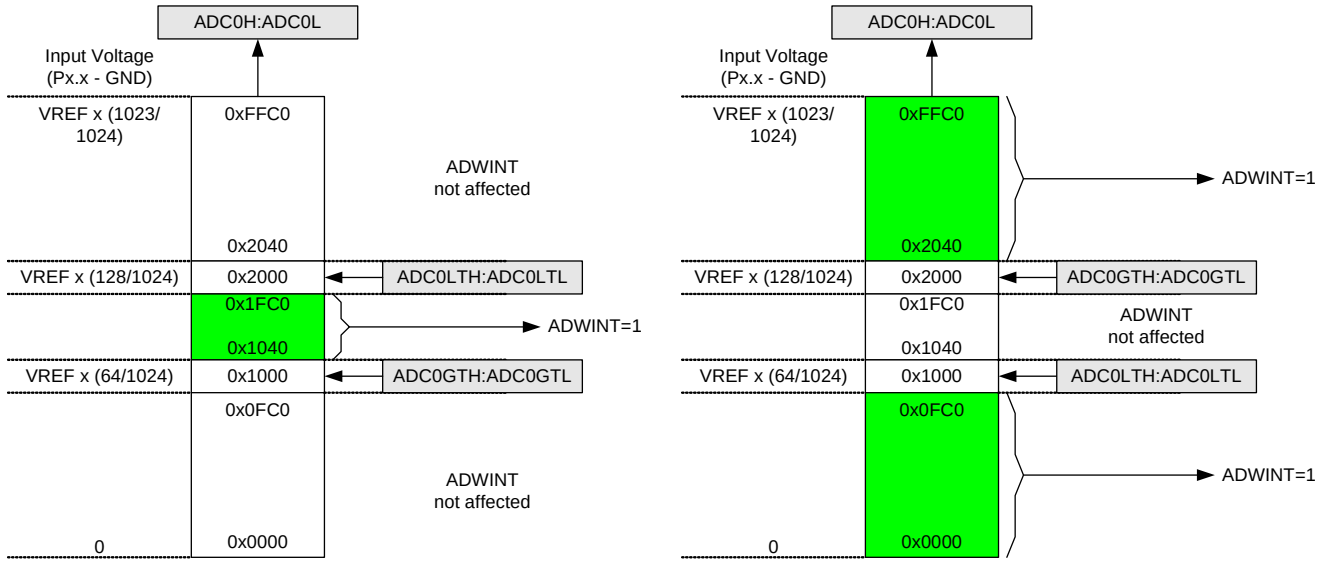


Figure 14.7. ADC Window Compare Example: Left-Justified Single-Ended Data

Register 15.5. B: B Register

Bit	7	6	5	4	3	2	1	0
Name	B							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xF0 (bit-addressable)								

Table 15.6. B Register Bit Descriptions

Bit	Name	Function
7:0	B	**B Register.** This register serves as a second accumulator for certain arithmetic operations.

Register 18.2. CRC0IN: CRC0 Data Input

Bit	7	6	5	4	3	2	1	0
Name	CRC0IN							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xDD								

Table 18.3. CRC0IN Register Bit Descriptions

Bit	Name	Function
7:0	CRC0IN	**CRC Data Input.** Each write to CRCIN results in the written data being computed into the existing CRC result according to the CRC algorithm.

20.3.3. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

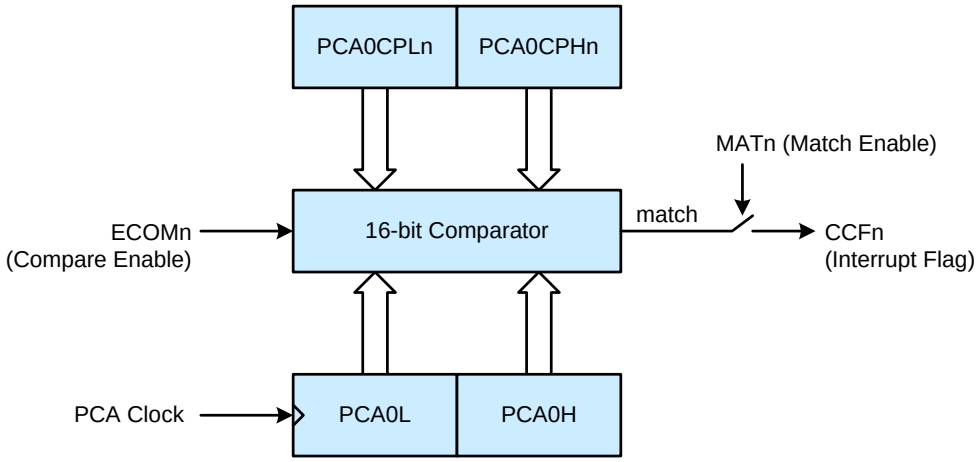


Figure 20.3. PCA Software Timer Mode Diagram

20.4.4. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. 16-bit PWM mode is independent of the other (8 through 11-bit) PWM modes. The entire PCA0CP register is used to determine the duty cycle in 16-bit PWM mode.

To output a varying duty cycle, new value writes should be synchronized with the PCA CCFn match flag to ensure seamless updates.

16-Bit PWM mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, the match interrupt flag should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. If the MATn bit is set to 1, the CCFn flag for the module will be set each time a match edge or up edge occurs. The CF flag in PCA0CN can be used to detect the overflow or down edge.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

Register 20.14. PCA0CPL1: PCA Capture Module Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPL1							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xE9								

Table 20.16. PCA0CPL1 Register Bit Descriptions

Bit	Name	Function
7:0	PCA0CPL1	**PCA Capture Module Low Byte.** The PCA0CPL1 register holds the low byte (LSB) of the 16-bit capture module.This register address also allows access to the low byte of the corresponding PCA channels auto-reload value for 9 to 11-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.
Note: A write to this register will clear the modules ECOM bit to a 0.		

Register 21.10. P0SKIP: Port 0 Skip

Bit	7	6	5	4	3	2	1	0
Name	P0SKIP							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xD4								

Table 21.13. P0SKIP Register Bit Descriptions

Bit	Name	Function
7:0	P0SKIP	**Port 0 Skip.** These bits select port pins to be skipped by the crossbar decoder. Port pins used for analog, special functions or GPIO should be skipped. 0: Corresponding P0.x pin is not skipped by the crossbar. 1: Corresponding P0.x pin is skipped by the crossbar.

22. Reset Sources and Supply Monitor

Reset circuitry allows the controller to be easily placed in a predefined default condition. Upon entering this reset state, the following events occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External port pins are placed in a known state
- Interrupts and timers are disabled.

All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain, low-drive mode. Weak pullups are enabled during and after the reset. For V_{DD} Monitor and power-on resets, the $\overline{RST}$ pin is driven low until the device exits the reset state. Note that during a power-on event, there may be a short delay before the POR circuitry fires and the $\overline{RST}$ pin is driven low. During that time, the $\overline{RST}$ pin will be weakly pulled to the V_{DD} supply pin.

On exit from the reset state, the program counter (PC) is reset, the Watchdog Timer is enabled and the system clock defaults to the internal oscillator. Program execution begins at location 0x0000.

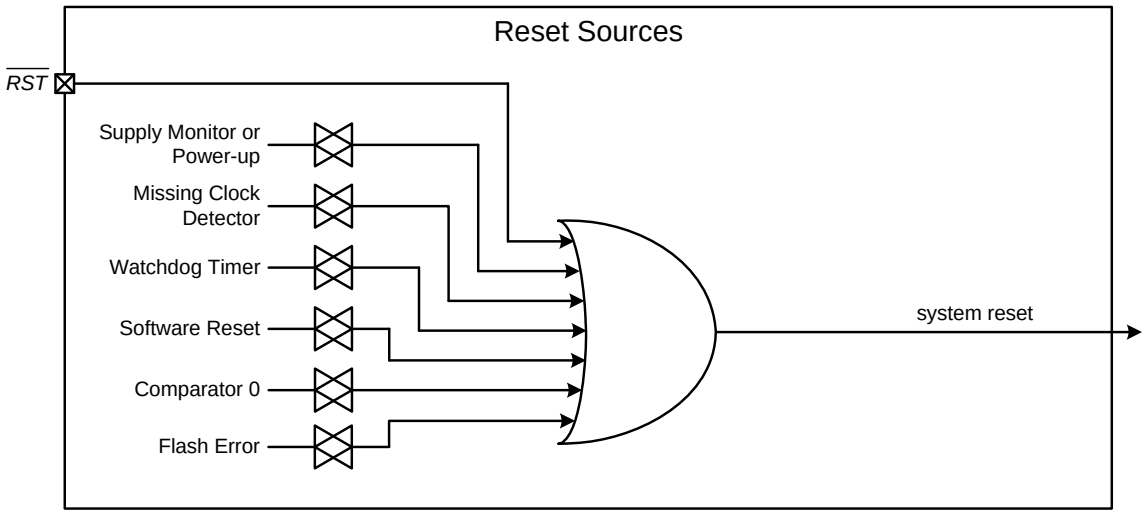
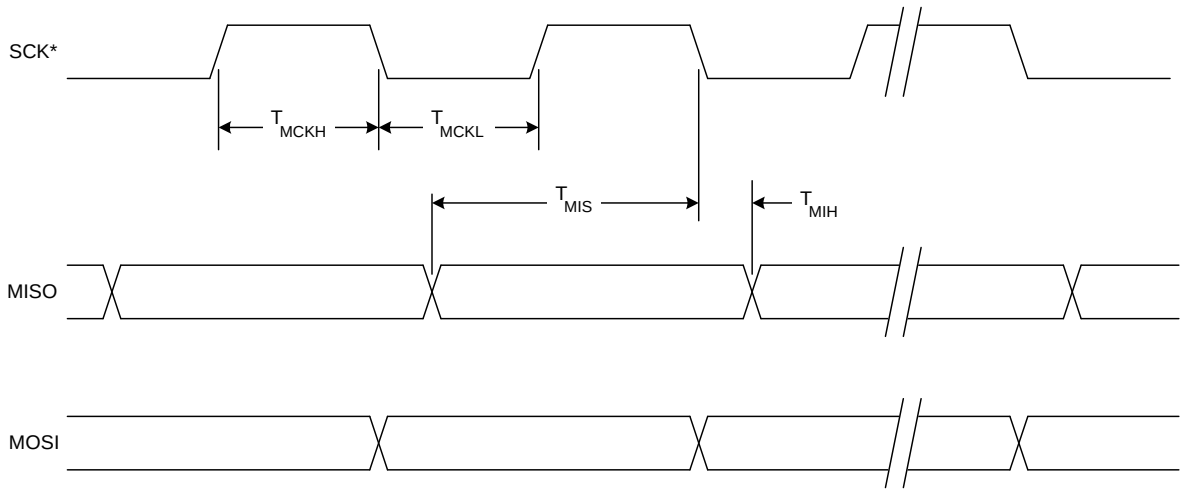
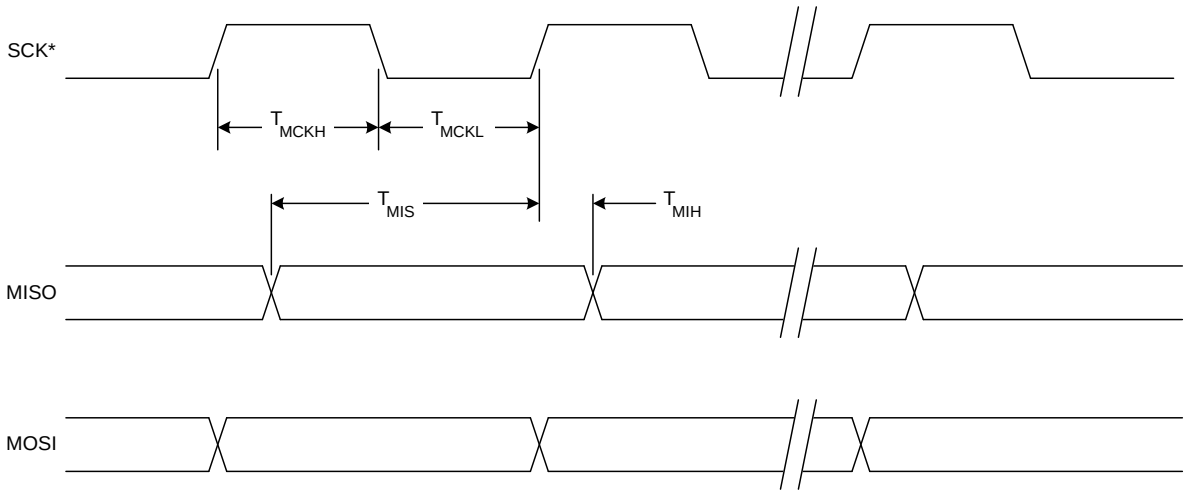


Figure 22.1. Reset Sources



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 23.8. SPI Master Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 23.9. SPI Master Timing (CKPHA = 1)

24.5.3. Write Sequence (Slave)

During a write sequence, an SMBus master writes data to a slave device. The slave in this transfer will be a receiver during the address byte, and a receiver during all data bytes. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode when a START followed by a slave address and direction bit (WRITE in this case) is received. If hardware ACK generation is disabled, upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. The software must respond to the received slave address with an ACK, or ignore the received slave address with a NACK. If hardware ACK generation is enabled, the hardware will apply the ACK for a slave address which matches the criteria set up by SMB0ADR and SMB0ADM. The interrupt will occur after the ACK cycle.

If the received slave address is ignored (by software or hardware), slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are received.

If hardware ACK generation is disabled, the ACKRQ is set to 1 and an interrupt is generated after each received byte. Software must write the ACK bit at that time to ACK or NACK the received byte.

With hardware ACK generation enabled, the SMBus hardware will automatically generate the ACK/NACK, and then post the interrupt. **It is important to note that the appropriate ACK or NACK value should be set up by the software prior to receiving the byte when hardware ACK generation is enabled.**

The interface exits Slave Receiver Mode after receiving a STOP. The interface will switch to Slave Transmitter Mode if SMB0DAT is written while an active Slave Receiver. Figure 24.7 shows a typical slave write sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the ‘data byte transferred’ interrupts occur at different places in the sequence, depending on whether hardware ACK generation is enabled. The interrupt occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled.

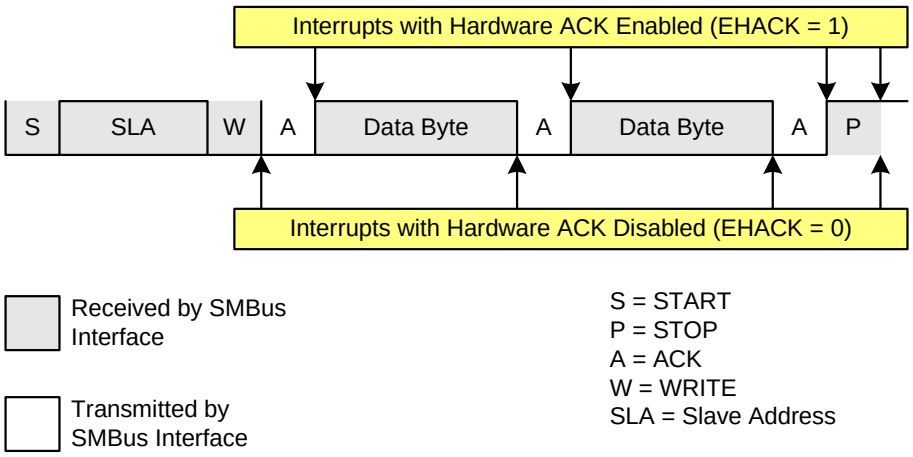


Figure 24.7. Typical Slave Write Sequence

Register 25.11. TMR2L: Timer 2 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2L							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xCC								

Table 25.13. TMR2L Register Bit Descriptions

Bit	Name	Function
7:0	TMR2L	**Timer 2 Low Byte.** In 16-bit mode, the TMR2L register contains the low byte of the 16-bit Timer 2. In 8-bit mode, TMR2L contains the 8-bit low byte timer value.

Register 29.3. C2REVID: C2 Revision ID

Bit	7	6	5	4	3	2	1	0
Name	C2REVID							
Type	R							
Reset	X	X	X	X	X	X	X	X
C2 Address: 0x01								

Table 29.3. C2REVID Register Bit Descriptions

Bit	Name	Function
7:0	C2REVID	**Revision ID.** This read-only register returns the 8-bit revision ID. For example: 0x00 = Revision A, 0x01 = Revision B and 0x02 = Revision C.