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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f854-c-iu

1. Electrical Specifications

1.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 1.1, unless stated otherwise.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.2	—	3.6	V
System Clock Frequency	f_{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T_A	Commercial Grade Devices (-GM, -GS, -GU)	–40	—	85	°C
		Industrial Grade Devices (-IM, -IS, -IU)	–40	—	125	°C
Note: All voltages with respect to GND						

Table 1.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (–Gx Devices, -40°C to +85°C)						
Normal Mode—Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 24.5 MHz[2]	—	4.45	4.85	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	915	1150	µA
		F_{SYSCLK} = 80 kHz[3], T_A = 25 °C	—	250	290	µA
		F_{SYSCLK} = 80 kHz[3]	—	250	380	µA
Idle Mode—Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 24.5 MHz[2]	—	2.05	2.3	mA
		F_{SYSCLK} = 1.53 MHz[2]	—	550	700	µA
		F_{SYSCLK} = 80 kHz[3], T_A = 25 °C	—	125	130	µA
		F_{SYSCLK} = 80 kHz[3]	—	125	200	µA
Stop Mode—Core halted and all clocks stopped, Supply monitor off.	I_{DD}	Internal LDO ON, T_A = 25 °C	—	105	120	µA
		Internal LDO ON	—	105	170	µA
		Internal LDO OFF	—	0.2	—	µA

Notes:
1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

1.2.3. Port I/O Output Drive

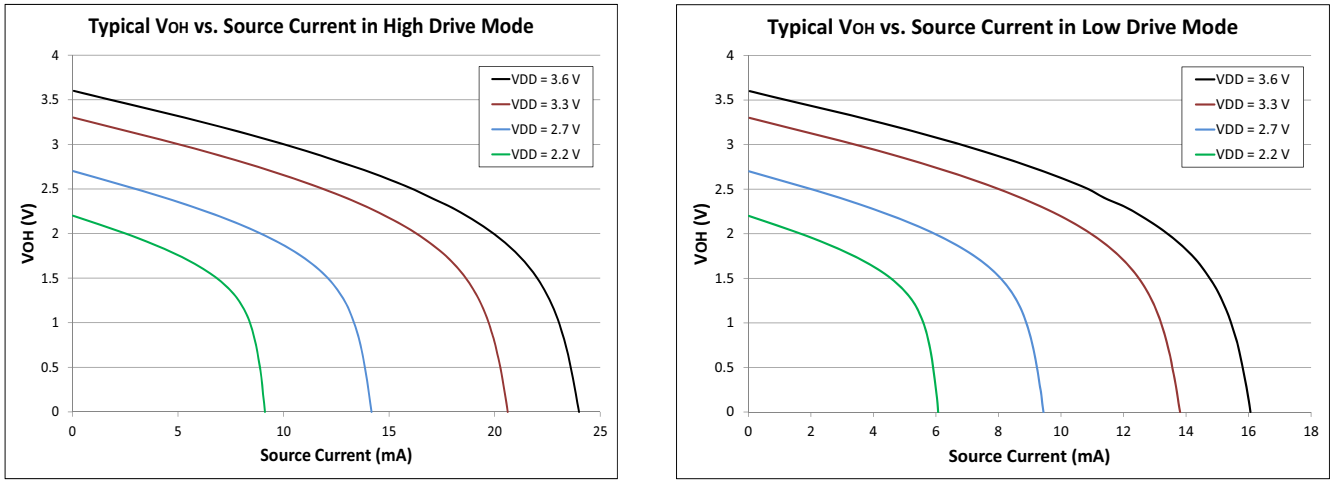


Figure 1.5. Typical V_{OH} vs. Source Current

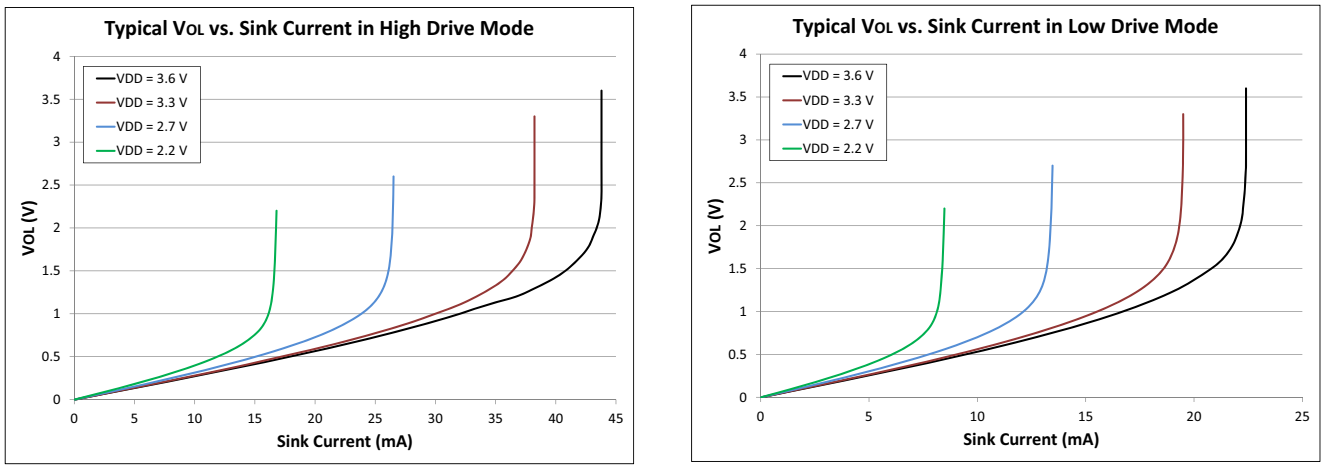


Figure 1.6. Typical V_{OL} vs. Sink Current

1.3. Thermal Conditions

Table 1.12. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	SOIC-16 Packages	—	70	—	°C/W
		QFN-20 Packages	—	60	—	°C/W
		QSOP-24 Packages	—	65	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

3.3. C8051F860/1/2/3/4/5 SOIC16 Pin Definitions

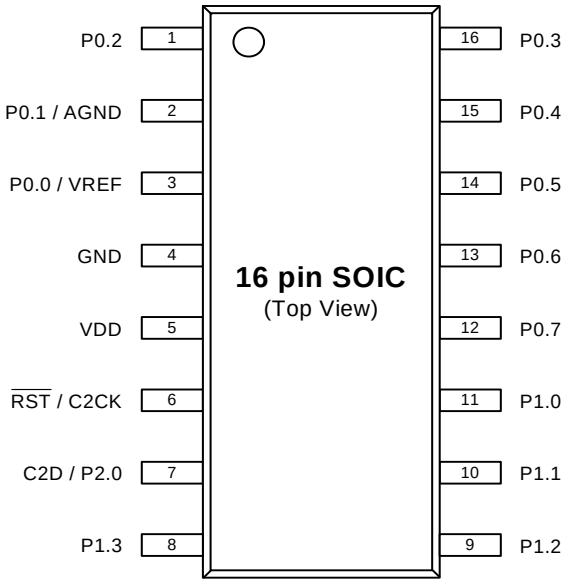


Figure 3.3. C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS Pinout

Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	4			
VDD	Power	5			
RST / C2CK	Active-low Reset / C2 Debug Clock	6			
P0.0	Standard I/O	3	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0

13.4. LDO Control Registers

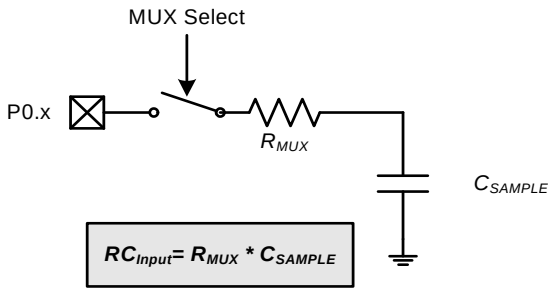
Register 13.2. REG0CN: Voltage Regulator Control

Bit	7	6	5	4	3	2	1	0
Name	Reserved				STOPCF	Reserved		
Type	R				RW	R		
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xC9								

Table 13.2. REG0CN Register Bit Descriptions

Bit	Name	Function
7:4	Reserved	Must write reset value.
3	STOPCF	**Stop Mode Configuration.** This bit configures the regulator's behavior when the device enters stop mode. 0: Regulator is still active in stop mode. Any enabled reset source will reset the device. 1: Regulator is shut down in stop mode. Only the $\overline{\text{RST}}$ pin or power cycle can reset the device.
2:0	Reserved	Must write reset value.

n is the ADC resolution in bits (8/10/12).



Note: The value of CSAMPLE depends on the PGA Gain. See electrical specifications for details.

Figure 14.4. ADC0 Equivalent Input Circuits

14.2.5. Gain Setting

The ADC has gain settings of 1x and 0.5x. In 1x mode, the full scale reading of the ADC is determined directly by VREF. In 0.5x mode, the full-scale reading of the ADC occurs when the input voltage is VREF x 2. The 0.5x gain setting can be useful to obtain a higher input voltage range when using a small VREF voltage, or to measure input voltages that are between VREF and VDD. Gain settings for the ADC are controlled by the ADGN bit in register ADC0CF. Note that even with a gain setting of 0.5, voltages above the supply rail cannot be measured directly by the ADC.

14.3. 8-Bit Mode

Setting the ADC08BE bit in register ADC0CF to 1 will put the ADC in 8-bit mode. In 8-bit mode, only the 8 MSBs of data are converted, allowing the conversion to be completed in fewer SAR clock cycles than a 10-bit conversion. The two LSBs of a conversion are always 00 in this mode, and the ADC0L register will always read back 0x00.

14.4. 12-Bit Mode

When configured for 12-bit conversions, the ADC performs four 10-bit conversions using four different reference voltages and combines the results into a single 12-bit value. Unlike simple averaging techniques, this method provides true 12-bit resolution of AC or DC input signals without depending on noise to provide dithering. The converter also employs a hardware dynamic element matching algorithm that reconfigures the largest elements of the internal DAC for each of the four 10-bit conversions. This reconfiguration cancels any matching errors and enables the converter to achieve 12-bit linearity performance to go along with its 12-bit resolution.

The 12-bit mode is enabled by setting the AD12BE bit in register ADC0AC to logic 1 and configuring the ADC in burst mode (ADBMEN = 1) for four or more conversions. The conversion can be initiated using any of the conversion start sources, and the 12-bit result will appear in the ADC0H and ADC0L registers. Since the 12-bit result is formed from a combination of four 10-bit results, the maximum output value is 4 x (1023) = 4092, rather than the max value of (2^12 – 1) = 4095 that is produced by a traditional 12-bit converter. To further increase resolution, the burst mode repeat value may be configured to any multiple of four conversions. For example, if a repeat value of 16 is selected, the ADC0 output will be a 14-bit number (sum of four 12-bit numbers) with 13 effective bits of resolution.

The AD12SM bit in register ADC0TK controls when the ADC will track and sample the input signal. When AD12SM is set to 1, the selected input signal will be tracked before the first conversion of a set and held internally during all four conversions. When AD12SM is cleared to 0, the ADC will track and sample the selected input before each of the four conversions in a set. When maximum throughput (180-200 ksps) is

Register 14.8. ADC0L: ADC0 Data Word Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0L							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xBD								

Table 14.11. ADC0L Register Bit Descriptions

Bit	Name	Function
7:0	ADC0L	**Data Word Low Byte.** When read, this register returns the least significant byte of the 16-bit ADC0 accumulator, formatted according to the settings in ADSJST. The register may also be written, to set the lower byte of the 16-bit ADC0 accumulator.
Note: If Accumulator shifting is enabled, the most significant bits of the value read will be zeros. This register should not be written when the SYNC bit is set to 1.		

Register 17.3. CPT0MX: Comparator 0 Multiplexer Selection

Bit	7	6	5	4	3	2	1	0
Name	CMXN				CMXP			
Type	RW				RW			
Reset	1	1	1	1	1	1	1	1
SFR Address: 0x9F								

Table 17.7. CPT0MX Register Bit Descriptions

Bit	Name	Function
7:4	CMXN	**Comparator 0 Negative Input MUX Selection.** 0000: External pin CP0N.0 0001: External pin CP0N.1 0010: External pin CP0N.2 0011: External pin CP0N.3 0100: External pin CP0N.4 0101: External pin CP0N.5 0110: External pin CP0N.6 0111: External pin CP0N.7 1000: GND 1001-1111: Reserved.
3:0	CMXP	**Comparator 0 Positive Input MUX Selection.** 0000: External pin CP0P.0 0001: External pin CP0P.1 0010: External pin CP0P.2 0011: External pin CP0P.3 0100: External pin CP0P.4 0101: External pin CP0P.5 0110: External pin CP0P.6 0111: External pin CP0P.7 1000: Internal LDO output 1001-1111: Reserved.

Register 18.6. CRC0FLIP: CRC0 Bit Flip

Bit	7	6	5	4	3	2	1	0
Name	CRC0FLIP							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xCF								

Table 18.7. CRC0FLIP Register Bit Descriptions

Bit	Name	Function
7:0	CRC0FLIP	**CRC0 Bit Flip.** Any byte written to CRC0FLIP is read back in a bit-reversed order, i.e., the written LSB becomes the MSB. For example: If 0xC0 is written to CRC0FLIP, the data read back will be 0x03. If 0x05 is written to CRC0FLIP, the data read back will be 0xA0.

19. External Interrupts ($\overline{INT0}$ and $\overline{INT1}$)

The C8051F85x/86x device family includes two external digital interrupt sources ($\overline{INT0}$ and $\overline{INT1}$), with dedicated interrupt sources (up to 16 additional I/O interrupts are available through the port match function). As is the case on a standard 8051 architecture, certain controls for these two interrupt sources are available in the Timer0/1 registers. Extensions to these controls which provide additional functionality on C8051F85x/86x devices are available in the IT01CF register. $\overline{INT0}$ and $\overline{INT1}$ are configurable as active high or low, edge- or level-sensitive. The IN0PL and IN1PL bits in the IT01CF register select active high or active low; the IT0 and IT1 bits in TCON select level- or edge-sensitive. The table below lists the possible configurations.

IT0	IN0PL	$\overline{INT0}$ Interrupt
1	0	Active low, edge-sensitive
1	1	Active high, edge-sensitive
0	0	Active low, level-sensitive
0	1	Active high, level-sensitive

IT1	IN1PL	$\overline{INT1}$ Interrupt
1	0	Active low, edge-sensitive
1	1	Active high, edge-sensitive
0	0	Active low, level-sensitive
0	1	Active high, level-sensitive

$\overline{INT0}$ and $\overline{INT1}$ are assigned to port pins as defined in the IT01CF register. Note that $\overline{INT0}$ and $\overline{INT1}$ port pin assignments are independent of any crossbar assignments. $\overline{INT0}$ and $\overline{INT1}$ will monitor their assigned port pins without disturbing the peripheral that was assigned the port pin via the crossbar. To assign a port pin only to $\overline{INT0}$ and/or $\overline{INT1}$, configure the crossbar to skip the selected pin(s).

IE0 and IE1 in the TCON register serve as the interrupt-pending flags for the $\overline{INT0}$ and $\overline{INT1}$ external interrupts, respectively. If an $\overline{INT0}$ or $\overline{INT1}$ external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by the hardware when the CPU vectors to the ISR. When configured as level sensitive, the interrupt-pending flag remains logic 1 while the input is active as defined by the corresponding polarity bit (IN0PL or IN1PL); the flag remains logic 0 while the input is inactive. The external interrupt source must hold the input active until the interrupt request is recognized. It must then deactivate the interrupt request before execution of the ISR completes or another interrupt request will be generated.

21.4. Port I/O Modes of Operation

Port pins are configured by firmware as digital or analog I/O using the PnMDIN registers. On reset, all port I/O cells default to a high impedance state with weak pull-ups enabled. Until the crossbar is enabled, both the high and low port I/O drive circuits are explicitly disabled on all crossbar pins. Port pins configured as digital I/O may still be used by analog peripherals; however, this practice is not recommended and may result in measurement errors.

21.4.1. Configuring Port Pins For Analog Modes

Any pins to be used for analog functions should be configured for analog mode. When a pin is configured for analog I/O, its weak pullup, digital driver, and digital receiver are disabled. Port pins configured for analog functions will always read back a value of ‘0’ in the corresponding Pn Port Latch register. To configure a pin as analog, the following steps should be taken:

1. Clear the bit associated with the pin in the PnMDIN register to ‘0’. This selects analog mode for the pin.
2. Set the bit associated with the pin in the Pn register to ‘1’.
3. Skip the bit associated with the pin in the PnSKIP register to ensure the crossbar does not attempt to assign a function to the pin.

21.4.2. Configuring Port Pins For Digital Modes

Any pins to be used by digital peripherals or as GPIO should be configured as digital I/O (PnMDIN.n = ‘1’). For digital I/O pins, one of two output modes (push-pull or open-drain) must be selected using the PnMDOUT registers.

Push-pull outputs (PnMDOUT.n = ‘1’) drive the port pad to the supply rails based on the output logic value of the port pin. Open-drain outputs have the high side driver disabled; therefore, they only drive the port pad to the low-side rail when the output logic value is ‘0’ and become high impedance inputs (both high low drivers turned off) when the output logic value is ‘1’.

When a digital I/O cell is placed in the high impedance state, a weak pull-up transistor pulls the port pad to the high-side rail to ensure the digital input is at a defined logic state. Weak pull-ups are disabled when the I/O cell is driven low to minimize power consumption, and they may be globally disabled by setting WEAKPUD to ‘1’. The user should ensure that digital I/O are always internally or externally pulled or driven to a valid logic state to minimize power consumption. Port pins configured for digital I/O always read back the logic state of the port pad, regardless of the output logic value of the port pin.

To configure a pin as digital input:

1. Set the bit associated with the pin in the PnMDIN register to ‘1’. This selects digital mode for the pin.
2. Clear the bit associated with the pin in the PnMDOUT register to ‘0’. This configures the pin as open-drain.
3. Set the bit associated with the pin in the Pn register to ‘1’. This tells the output driver to “drive” logic high. Because the pin is configured as open-drain, the high-side driver is not active, and the pin may be used as an input.

Open-drain outputs are configured exactly as digital inputs. However, the pin may be driven low by an assigned peripheral, or by writing ‘0’ to the associated bit in the Pn register if the signal is a GPIO.

To configure a pin as a digital, push-pull output:

1. Set the bit associated with the pin in the PnMDIN register to ‘1’. This selects digital mode for the pin.
2. Set the bit associated with the pin in the PnMDOUT register to ‘1’. This configures the pin as push-pull.

If a digital pin is to be used as a general-purpose I/O, or with a digital function that is not part of the crossbar, the bit associated with the pin in the PnSKIP register can be set to ‘1’ to ensure the crossbar does not attempt to assign a function to the pin.

Register 21.12. P1MAT: Port 1 Match

Bit	7	6	5	4	3	2	1	0
Name	P1MAT							
Type	RW							
Reset	1	1	1	1	1	1	1	1
SFR Address: 0xED								

Table 21.15. P1MAT Register Bit Descriptions

Bit	Name	Function
7:0	P1MAT	**Port 1 Match Value.** Match comparison value used on P1 pins for bits in P1MASK which are set to 1. 0: P1.x pin logic value is compared with logic LOW. 1: P1.x pin logic value is compared with logic HIGH.
Note: Port 1 consists of 8 bits (P1.0-P1.7) on QSOP24 packages and 7 bits (P1.0-P1.6) on QFN20 packages and 4 bits (P1.0-P1.3) on SOIC16 packages.		

Register 21.15. P1MDOUT: Port 1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xA5								

Table 21.18. P1MDOUT Register Bit Descriptions

Bit	Name	Function
7:0	P1MDOUT	**Port 1 Output Mode.** These bits are only applicable when the pin is configured for digital mode using the P1MDIN register. 0: Corresponding P1.n Output is open-drain. 1: Corresponding P1.n Output is push-pull.
Note: Port 1 consists of 8 bits (P1.0-P1.7) on QSOP24 packages and 7 bits (P1.0-P1.6) on QFN20 packages and 4 bits (P1.0-P1.3) on SOIC16 packages.		

22.10. Reset Sources Control Registers

Register 22.1. RSTSRC: Reset Source

Bit	7	6	5	4	3	2	1	0
Name	Reserved	FERROR	C0RSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF
Type	R	R	RW	RW	R	RW	RW	R
Reset	0	X	X	X	X	X	X	X
SFR Address: 0xEF								

Table 22.1. RSTSRC Register Bit Descriptions

Bit	Name	Function
7	Reserved	Must write reset value.
6	FERROR	**Flash Error Reset Flag.** This read-only bit is set to 1 if a flash read/write/erase error caused the last reset.
5	C0RSEF	**Comparator0 Reset Enable and Flag.** Read: This bit reads 1 if Comparator0 caused the last reset. Write: Writing a 1 to this bit enables Comparator0 (active-low) as a reset source.
4	SWRSF	**Software Reset Force and Flag.** Read: This bit reads 1 if last reset was caused by a write to SWRSF. Write: Writing a 1 to this bit forces a system reset.
3	WDTRSF	**Watchdog Timer Reset Flag.** This read-only bit is set to 1 if a watchdog timer overflow caused the last reset.
2	MCDRSF	**Missing Clock Detector Enable and Flag.** Read: This bit reads 1 if a missing clock detector timeout caused the last reset. Write: Writing a 1 to this bit enables the missing clock detector. The MCD triggers a reset if a missing clock condition is detected.
1	PORSF	**Power-On / Supply Monitor Reset Flag, and Supply Monitor Reset Enable.** Read: This bit reads 1 anytime a power-on or supply monitor reset has occurred. Write: Writing a 1 to this bit enables the supply monitor as a reset source.
0	PINRSF	**HW Pin Reset Flag.** This read-only bit is set to 1 if the RST pin caused the last reset.

Notes:
1. Reads and writes of the RSTSRC register access different logic in the device. Reading the register always returns status information to indicate the source of the most recent reset. Writing to the register activates certain options as reset sources. It is recommended to not use any kind of read-modify-write operation on this register.
2. When the PORSF bit reads back 1 all other RSTSRC flags are indeterminate.
3. Writing 1 to the PORSF bit when the supply monitor is not enabled and stabilized may cause a system reset.

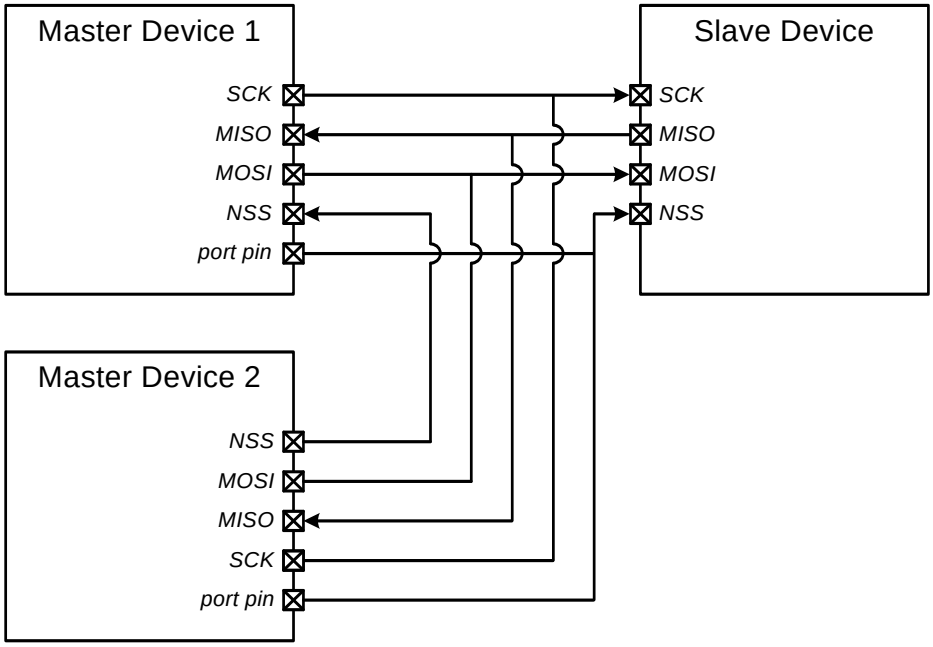


Figure 23.2. Multiple-Master Mode Connection Diagram

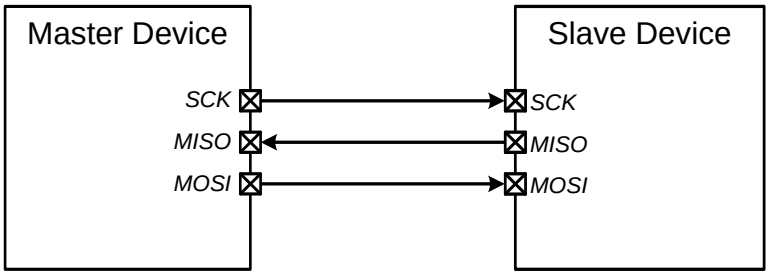


Figure 23.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram

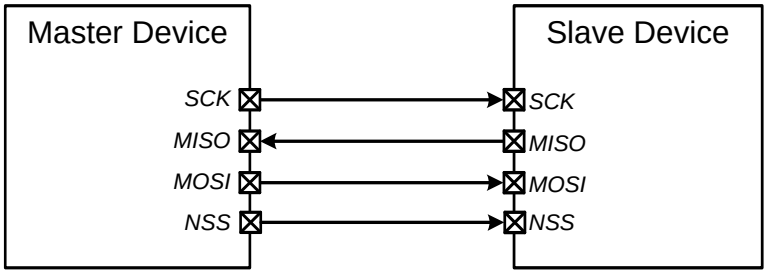


Figure 23.4. 4-Wire Single Master Mode and 4-Wire Slave Mode Connection Diagram

Table 23.1. SPI Slave Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode Timing (See Figure 23.8 and Figure 23.9)				
T_{MCKH}	SCK High Time	1 x T_{SYSCLK}	—	ns
T_{MCKL}	SCK Low Time	1 x T_{SYSCLK}	—	ns
T_{MIS}	MISO Valid to SCK Shift Edge	1 x T_{SYSCLK} + 20	—	ns
T_{MIH}	SCK Shift Edge to MISO Change	0	—	ns
Slave Mode Timing (See Figure 23.10 and Figure 23.11)				
T_{SE}	NSS Falling to First SCK Edge	2 x T_{SYSCLK}	—	ns
T_{SD}	Last SCK Edge to NSS Rising	2 x T_{SYSCLK}	—	ns
T_{SEZ}	NSS Falling to MISO Valid	—	4 x T_{SYSCLK}	ns
T_{SDZ}	NSS Rising to MISO High-Z	—	4 x T_{SYSCLK}	ns
T_{CKH}	SCK High Time	5 x T_{SYSCLK}	—	ns
T_{CKL}	SCK Low Time	5 x T_{SYSCLK}	—	ns
T_{SIS}	MOSI Valid to SCK Sample Edge	2 x T_{SYSCLK}	—	ns
T_{SIH}	SCK Sample Edge to MOSI Change	2 x T_{SYSCLK}	—	ns
T_{SOH}	SCK Shift Edge to MISO Change	—	4 x T_{SYSCLK}	ns
T_{SLH}	Last SCK Edge to MISO Change (CKPHA = 1 ONLY)	6 x T_{SYSCLK}	8 x T_{SYSCLK}	ns
Note: T_{SYSCLK} is equal to one period of the device system clock (SYSCLK).				

Register 23.4. SPI0DAT: SPI0 Data

Bit	7	6	5	4	3	2	1	0
Name	SPI0DAT							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xA3								

Table 23.5. SPI0DAT Register Bit Descriptions

Bit	Name	Function
7:0	SPI0DAT	**SPI0 Transmit and Receive Data.** The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0-DAT places the data into the transmit buffer and initiates a transfer when in master mode. A read of SPI0DAT returns the contents of the receive buffer.

24.5.2. Read Sequence (Master)

During a read sequence, an SMBus master reads data from a slave device. The master in this transfer will be a transmitter during the address byte, and a receiver during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 1 (READ). Serial data is then received from the slave on SDA while the SMBus outputs the serial clock. The slave transmits one or more bytes of serial data.

If hardware ACK generation is disabled, the ACKRQ is set to 1 and an interrupt is generated after each received byte. Software must write the ACK bit at that time to ACK or NACK the received byte.

With hardware ACK generation enabled, the SMBus hardware will automatically generate the ACK/NACK, and then post the interrupt. **It is important to note that the appropriate ACK or NACK value should be set up by the software prior to receiving the byte when hardware ACK generation is enabled.**

Writing a 1 to the ACK bit generates an ACK; writing a 0 generates a NACK. Software should write a 0 to the ACK bit for the last data transfer, to transmit a NACK. The interface exits Master Receiver Mode after the STO bit is set and a STOP is generated. The interface will switch to Master Transmitter Mode if SMB0DAT is written while an active Master Receiver. Figure 24.6 shows a typical master read sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the ‘data byte transferred’ interrupts occur at different places in the sequence, depending on whether hardware ACK generation is enabled. The interrupt occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled.

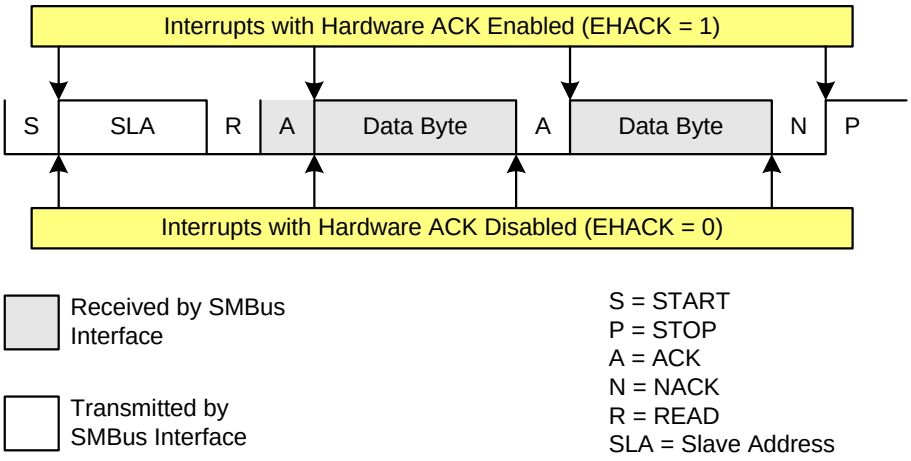


Figure 24.6. Typical Master Read Sequence

24.5.4. Read Sequence (Slave)

During a read sequence, an SMBus master reads data from a slave device. The slave in this transfer will be a receiver during the address byte, and a transmitter during all data bytes. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode (to receive the slave address) when a START followed by a slave address and direction bit (READ in this case) is received. If hardware ACK generation is disabled, upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. The software must respond to the received slave address with an ACK, or ignore the received slave address with a NACK. If hardware ACK generation is enabled, the hardware will apply the ACK for a slave address which matches the criteria set up by SMB0ADR and SMB0ADM. The interrupt will occur after the ACK cycle.

If the received slave address is ignored (by software or hardware), slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are transmitted. If the received slave address is acknowledged, data should be written to SMB0DAT to be transmitted. The interface enters slave transmitter mode, and transmits one or more bytes of data. After each byte is transmitted, the master sends an acknowledge bit; if the acknowledge bit is an ACK, SMB0DAT should be written with the next data byte. If the acknowledge bit is a NACK, SMB0DAT should not be written to before SI is cleared (an error condition may be generated if SMB0DAT is written following a received NACK while in slave transmitter mode). The interface exits slave transmitter mode after receiving a STOP. The interface will switch to slave receiver mode if SMB0DAT is not written following a Slave Transmitter interrupt. Figure 24.8 shows a typical slave read sequence. Two transmitted data bytes are shown, though any number of bytes may be transmitted. Notice that all of the “data byte transferred” interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.

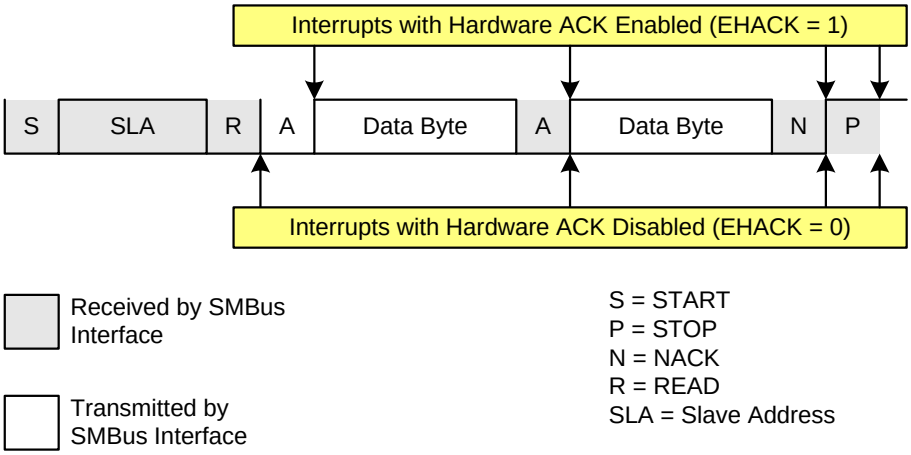


Figure 24.8. Typical Slave Read Sequence

24.6. SMBus Status Decoding

The current SMBus status can be easily decoded using the SMB0CN register. The appropriate actions to take in response to an SMBus event depend on whether hardware slave address recognition and ACK generation is enabled or disabled. Table 24.5 describes the typical actions when hardware slave address recognition and ACK generation is disabled. Table 24.6 describes the typical actions when hardware slave address recognition and ACK generation is enabled. In the tables, STATUS VECTOR refers to the four upper bits of SMB0CN: MASTER, TXMODE, STA, and STO. The shown response options are only the typical responses; application-specific procedures are allowed as long as they conform to the SMBus specification. Highlighted responses are allowed by hardware but do not conform to the SMBus specification.

Register 24.2. SMB0TC: SMBus0 Timing and Pin Control

Bit	7	6	5	4	3	2	1	0
Name	SWAP	Reserved					SDD	
Type	RW	R					RW	
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xAC								

Table 24.8. SMB0TC Register Bit Descriptions

Bit	Name	Function
7	SWAP	**SMBus0 Swap Pins.** This bit swaps the order of the SMBus0 pins on the crossbar. 0: SDA is mapped to the lower-numbered port pin, and SCL is mapped to the higher-numbered port pin. 1: SCL is mapped to the lower-numbered port pin, and SDA is mapped to the higher-numbered port pin.
6:2	Reserved	Must write reset value.
1:0	SDD	**SMBus0 Start Detection Window.** These bits increase the hold time requirement between SDA falling and SCL falling for START detection. 00: No additional hold time window (0-1 SYSCLK). 01: Increase hold time window to 2-3 SYSCLKs. 10: Increase hold time window to 4-5 SYSCLKs. 11: Increase hold time window to 8-9 SYSCLKs.

Table 25.15. TMR3CN Register Bit Descriptions

Bit	Name	Function
0	T3XCLK	**Timer 3 External Clock Select.** This bit selects the external clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 3 clock is the system clock divided by 12. 1: Timer 3 clock is the external clock divided by 8 (synchronized with SYSCLK).