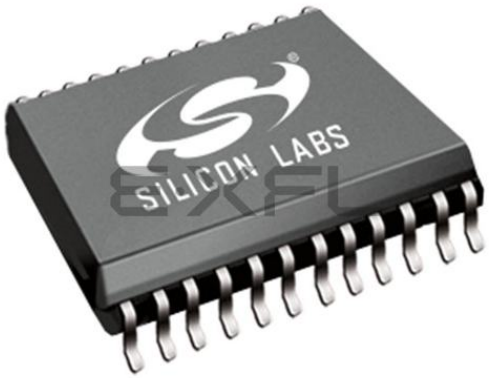

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f855-c-gu

3.3. C8051F860/1/2/3/4/5 SOIC16 Pin Definitions

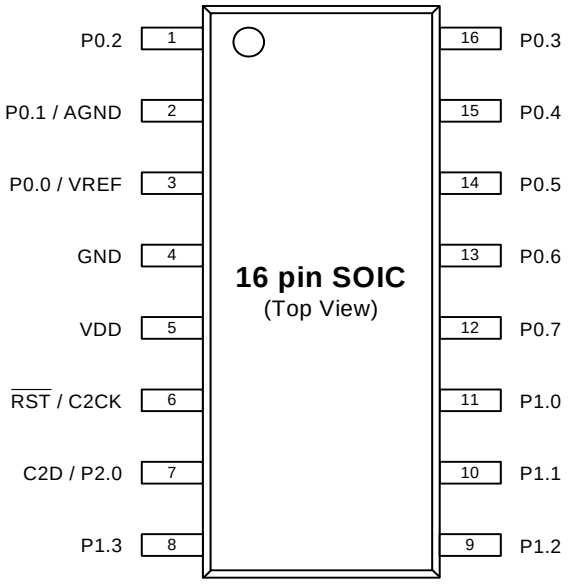

Figure 3.3. C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS Pinout

Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	4			
VDD	Power	5			
RST / C2CK	Active-low Reset / C2 Debug Clock	6			
P0.0	Standard I/O	3	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0

7. SOIC-16 Package Specifications

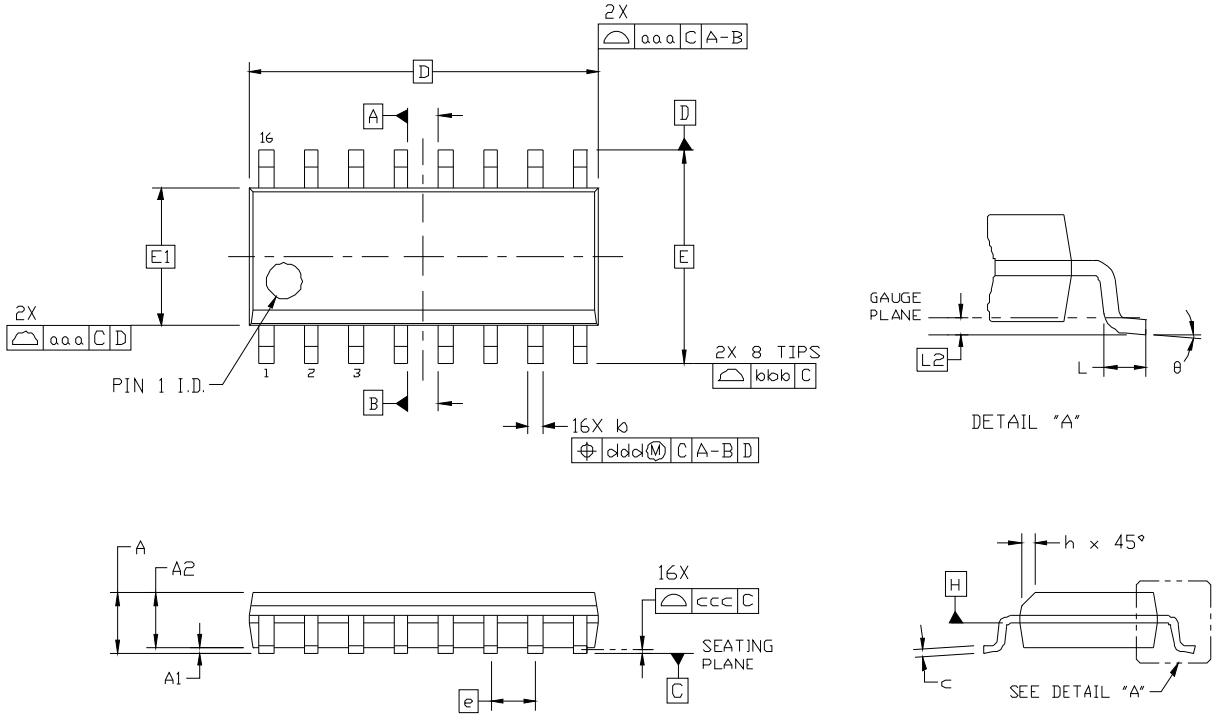

Figure 7.1. SOIC-16 Package Drawing

Table 7.1. SOIC-16 Package Dimensions

Dimension	Min	Nom	Max
A	—		1.75
A1	0.10		0.25
A2	1.25		—
b	0.31		0.51
c	0.17		0.25
D		9.90 BSC	
E		6.00 BSC	
E1		3.90 BSC	
e		1.27 BSC	

Dimension	Min	Nom	Max
L	0.40		1.27
L2		0.25 BSC	
h	0.25		0.50
θ	0º		8º
aaa		0.10	
bbb		0.20	
ccc		0.10	
ddd		0.25	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Memory Organization

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory organization of the C8051F85x/86x device family is shown in Figure 8.1.

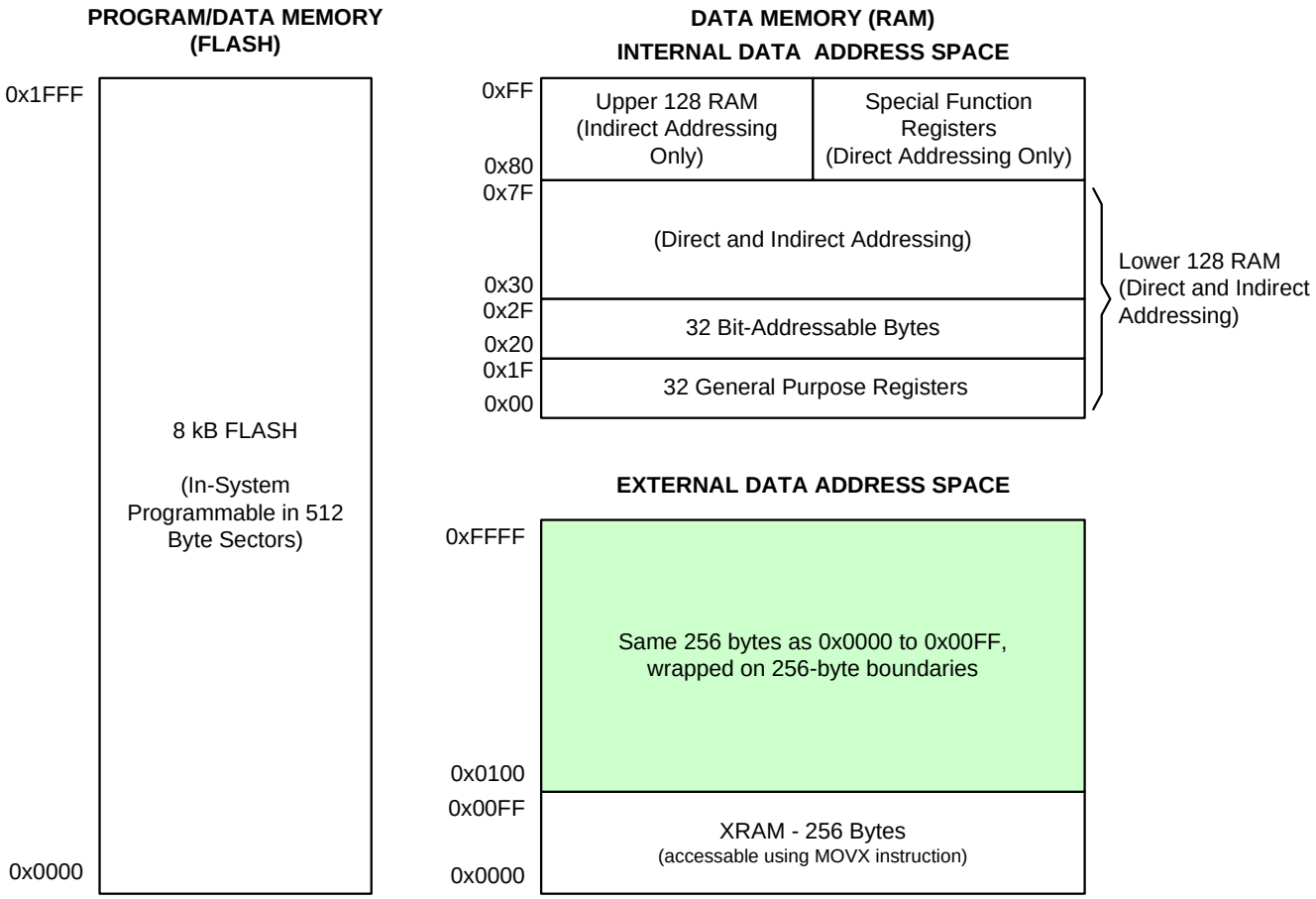

Figure 8.1. C8051F85x/86x Memory Map (8 kB flash version shown)

8.1. Program Memory

The CIP-51 core has a 64 kB program memory space. The C8051F85x/86x family implements 8 kB, 4 kB or 2 kB of this program memory space as in-system, re-programmable flash memory. The last address in the flash block (0x1FFF on 8 kB devices, 0x0FFF on 4 kB devices and 0x07FF on 2 kB devices) serves as a security lock byte for the device, and provides read, write and erase protection. Addresses above the lock byte within the 64 kB address space are reserved.

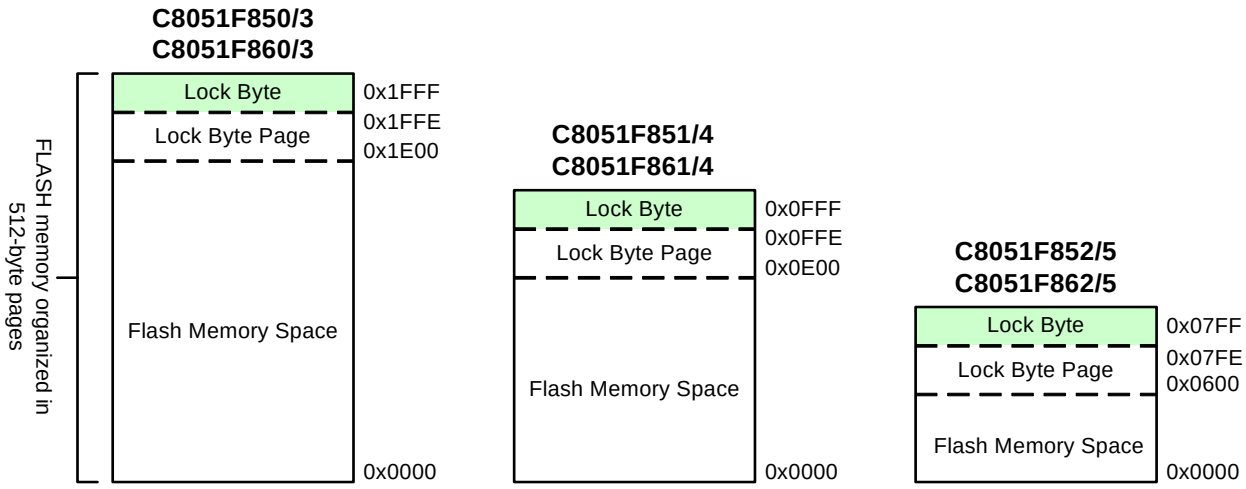

Figure 8.2. Flash Program Memory Map

8.1.1. MOVX Instruction and Program Memory

The MOVX instruction in an 8051 device is typically used to access external data memory. On the C8051F85x/86x devices, the MOVX instruction is normally used to read and write on-chip XRAM, but can be re-configured to write and erase on-chip flash memory space. MOVC instructions are always used to read flash memory, while MOVX write instructions are used to erase and write flash. This flash access feature provides a mechanism for the C8051F85x/86x to update program code and use the program memory space for non-volatile data storage. Refer to Section “10. Flash Memory” on page 61 for further details.

8.2. Data Memory

The C8051F85x/86x device family includes up to 512 bytes of RAM data memory. 256 bytes of this memory is mapped into the internal RAM space of the 8051. On devices with 512 bytes total RAM, 256 additional bytes of memory are available as on-chip “external” memory. The data memory map is shown in Figure 8.1 for reference.

8.2.1. Internal RAM

There are 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

Table 9.2. Special Function Registers (Continued)

Register	Address	Register Description	Page
SPI0DAT	0xA3	SPI0 Data	232
TCON	0x88	Timer 0/1 Control	271
TH0	0x8C	Timer 0 High Byte	275
TH1	0x8D	Timer 1 High Byte	276
TL0	0x8A	Timer 0 Low Byte	273
TL1	0x8B	Timer 1 Low Byte	274
TMOD	0x89	Timer 0/1 Mode	272
TMR2CN	0xC8	Timer 2 Control	277
TMR2H	0xCD	Timer 2 High Byte	282
TMR2L	0xCC	Timer 2 Low Byte	281
TMR2RLH	0xCB	Timer 2 Reload High Byte	280
TMR2RLL	0xCA	Timer 2 Reload Low Byte	279
TMR3CN	0x91	Timer 3 Control	283
TMR3H	0x95	Timer 3 High Byte	288
TMR3L	0x94	Timer 3 Low Byte	287
TMR3RLH	0x93	Timer 3 Reload High Byte	286
TMR3RLL	0x92	Timer 3 Reload Low Byte	285
VDM0CN	0xFF	Supply Monitor Control	216
WDTCN	0x97	Watchdog Timer Control	300
XBR0	0xE1	Port I/O Crossbar 0	193
XBR1	0xE2	Port I/O Crossbar 1	194
XBR2	0xE3	Port I/O Crossbar 2	195

Register 11.3. REVID: Revision Identifcation

Bit	7	6	5	4	3	2	1	0
Name	REVID							
Type	R							
Reset	X	X	X	X	X	X	X	X
SFR Address: 0xB6								

Table 11.4. REVID Register Bit Descriptions

Bit	Name	Function
7:0	REVID	**Revision ID.** This read-only register returns the 8-bit revision ID. 00000000: Revision A 00000001: Revision B 00000010: Revision C 00000011-11111111: Reserved.

Table 12.4. EIE1 Register Bit Descriptions

Bit	Name	Function
0	ESMB0	**Enable SMBus (SMB0) Interrupt.** This bit sets the masking of the SMB0 interrupt. 0: Disable all SMB0 interrupts. 1: Enable interrupt requests generated by SMB0.

13. Power Management and Internal Regulator

All internal circuitry on the C8051F85x/86x devices draws power from the VDD supply pin. Circuits with external connections (I/O pins, analog muxes) are powered directly from the VDD supply voltage, while most of the internal circuitry is supplied by an on-chip LDO regulator. The regulator output is fully internal to the device, and is available also as an ADC input or reference source for the comparators and ADC.

The devices support the standard 8051 power modes: idle and stop. For further power savings in stop mode, the internal LDO regulator may be disabled, shutting down the majority of the power nets on the device.

Although the C8051F85x/86x has idle and stop modes available, more control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

13.1. Power Modes

Idle mode halts the CPU while leaving the peripherals and clocks active. In stop mode, the CPU is halted, all interrupts and timers are inactive, and the internal oscillator is stopped (analog peripherals remain in their selected states; the external oscillator is not affected). Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode consumes the least power because the majority of the device is shut down with no clocks active. The Power Control Register (PCON) is used to control the C8051F85x/86x's Stop and Idle power management modes.

13.1.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the hardware to halt the CPU and enter idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

Note: If the instruction following the write of the IDLE bit is a single-byte instruction and an interrupt occurs during the execution phase of the instruction that sets the IDLE bit, the CPU may not wake from Idle mode when a future interrupt occurs. Therefore, instructions that set the IDLE bit should be followed by an instruction that has two or more opcode bytes, for example:

```
// in 'C':
PCON |= 0x01;                  // set IDLE bit
PCON = PCON;                   // ... followed by a 3-cycle dummy instruction

; in assembly:
ORL PCON, #01h                 ; set IDLE bit
MOV PCON, PCON                 ; ... followed by a 3-cycle dummy instruction
```

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system.

Register 14.12. ADC0LTL: ADC0 Less-Than Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0LTL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xC5								

Table 14.15. ADC0LTL Register Bit Descriptions

Bit	Name	Function
7:0	ADC0LTL	**Less-Than Low Byte.** Least Significant Byte of the 16-bit Less-Than window compare register.
Note: In 8-bit mode, this register should be set to 0x00.		

Register 15.4. ACC: Accumulator

Bit	7	6	5	4	3	2	1	0
Name	ACC							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xE0 (bit-addressable)								

Table 15.5. ACC Register Bit Descriptions

Bit	Name	Function
7:0	ACC	**Accumulator.** This register is the accumulator for arithmetic operations.

20.3.4. High-Speed Output Mode

In High-Speed Output mode, a module's associated CEXn pin is toggled each time a match occurs between the PCA Counter and the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode. If ECOMn is cleared, the associated pin will retain its state, and not toggle on the next match event.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

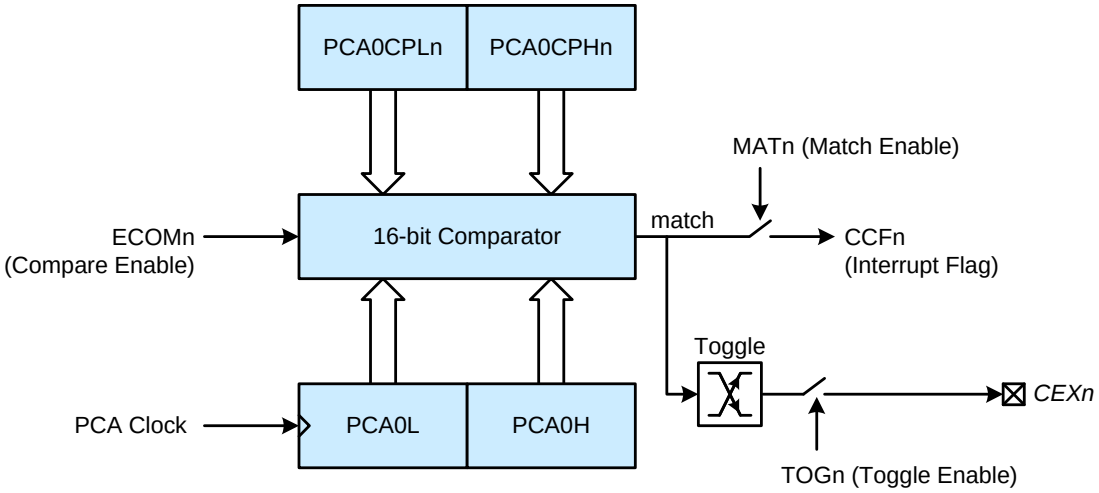

Figure 20.4. PCA High-Speed Output Mode Diagram

Register 20.10. PCA0POL: PCA Output Polarity

Bit	7	6	5	4	3	2	1	0
Name	Reserved					CEX2POL	CEX1POL	CEX0POL
Type	R					RW	RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x96								

Table 20.12. PCA0POL Register Bit Descriptions

Bit	Name	Function
7:3	Reserved	Must write reset value.
2	CEX2POL	**CEX2 Output Polarity.** Selects the polarity of the CEX2 output channel. When this bit is modified, the change takes effect at the pin immediately. 0: Use default polarity. 1: Invert polarity.
1	CEX1POL	**CEX1 Output Polarity.** Selects the polarity of the CEX1 output channel. When this bit is modified, the change takes effect at the pin immediately. 0: Use default polarity. 1: Invert polarity.
0	CEX0POL	**CEX0 Output Polarity.** Selects the polarity of the CEX0 output channel. When this bit is modified, the change takes effect at the pin immediately. 0: Use default polarity. 1: Invert polarity.

Register 20.13. PCA0CPM2: PCA Capture/Compare Mode

Bit	7	6	5	4	3	2	1	0
Name	PWM16	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xDC								

Table 20.15. PCA0CPM2 Register Bit Descriptions

Bit	Name	Function
7	PWM16	**16-bit Pulse Width Modulation Enable.** This bit enables 16-bit mode when Pulse Width Modulation mode is enabled. 0: 8 to 11-bit PWM selected. 1: 16-bit PWM selected.
6	ECOM	**Comparator Function Enable.** This bit enables the comparator function.
5	CAPP	**Capture Positive Function Enable.** This bit enables the positive edge capture capability.
4	CAPN	**Capture Negative Function Enable.** This bit enables the negative edge capture capability.
3	MAT	**Match Function Enable.** This bit enables the match function. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCF2 bit in the PCA0MD register to be set to logic 1.
2	TOG	**Toggle Function Enable.** This bit enables the toggle function. When enabled, matches of the PCA counter with the capture/compare register cause the logic level on the CEX2 pin to toggle. If the PWM bit is also set to logic 1, the module operates in Frequency Output Mode.
1	PWM	**Pulse Width Modulation Mode Enable.** This bit enables the PWM function. When enabled, a pulse width modulated signal is output on the CEX2 pin. 8 to 11-bit PWM is used if PWM16 is cleared; 16-bit mode is used if PWM16 is set to logic 1. If the TOG bit is also set, the module operates in Frequency Output Mode.
0	ECCF	**Capture/Compare Flag Interrupt Enable.** This bit sets the masking of the Capture/Compare Flag (CCF2) interrupt. 0: Disable CCF2 interrupts. 1: Enable a Capture/Compare Flag interrupt request when CCF2 is set.

Register 20.14. PCA0CPL1: PCA Capture Module Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPL1							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xE9								

Table 20.16. PCA0CPL1 Register Bit Descriptions

Bit	Name	Function
7:0	PCA0CPL1	**PCA Capture Module Low Byte.** The PCA0CPL1 register holds the low byte (LSB) of the 16-bit capture module.This register address also allows access to the low byte of the corresponding PCA channels auto-reload value for 9 to 11-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.
Note: A write to this register will clear the modules ECOM bit to a 0.		

21.7. Port I/O and Pin Configuration Control Registers

Register 21.1. XBR0: Port I/O Crossbar 0

Bit	7	6	5	4	3	2	1	0
Name	SYSCKE	CP1AE	CP1E	CP0AE	CP0E	SMB0E	SPI0E	URT0E
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xE1								

Table 21.4. XBR0 Register Bit Descriptions

Bit	Name	Function
7	SYSCKE	**SYSCLK Output Enable.** 0: SYSCLK unavailable at Port pin. 1: SYSCLK output routed to Port pin.
6	CP1AE	**Comparator1 Asynchronous Output Enable.** 0: Asynchronous CP1 unavailable at Port pin. 1: Asynchronous CP1 routed to Port pin.
5	CP1E	**Comparator1 Output Enable.** 0: CP1 unavailable at Port pin. 1: CP1 routed to Port pin.
4	CP0AE	**Comparator0 Asynchronous Output Enable.** 0: Asynchronous CP0 unavailable at Port pin. 1: Asynchronous CP0 routed to Port pin.
3	CP0E	**Comparator0 Output Enable.** 0: CP0 unavailable at Port pin. 1: CP0 routed to Port pin.
2	SMB0E	**SMBus0 I/O Enable.** 0: SMBus0 I/O unavailable at Port pins. 1: SMBus0 I/O routed to Port pins.
1	SPI0E	**SPI I/O Enable.** 0: SPI I/O unavailable at Port pins. 1: SPI I/O routed to Port pins. The SPI can be assigned either 3 or 4 GPIO pins.
0	URT0E	**UART I/O Output Enable.** 0: UART I/O unavailable at Port pin. 1: UART TX, RX routed to Port pins P0.4 and P0.5.

Register 21.12. P1MAT: Port 1 Match

Bit	7	6	5	4	3	2	1	0
Name	P1MAT							
Type	RW							
Reset	1	1	1	1	1	1	1	1
SFR Address: 0xED								

Table 21.15. P1MAT Register Bit Descriptions

Bit	Name	Function
7:0	P1MAT	**Port 1 Match Value.** Match comparison value used on P1 pins for bits in P1MASK which are set to 1. 0: P1.x pin logic value is compared with logic LOW. 1: P1.x pin logic value is compared with logic HIGH.
Note: Port 1 consists of 8 bits (P1.0-P1.7) on QSOP24 packages and 7 bits (P1.0-P1.6) on QFN20 packages and 4 bits (P1.0-P1.3) on SOIC16 packages.		

Table 24.7. SMB0CF Register Bit Descriptions

Bit	Name	Function
1:0	SMBCS	**SMBus0 Clock Source Selection.** These two bits select the SMBus0 clock source, which is used to generate the SMBus0 bit rate. See the SMBus clock timing section for additional details. 00: Timer 0 Overflow 01: Timer 1 Overflow 10: Timer 2 High Byte Overflow 11: Timer 2 Low Byte Overflow

Register 25.14. TMR3RLL: Timer 3 Reload Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x92								

Table 25.16. TMR3RLL Register Bit Descriptions

Bit	Name	Function
7:0	TMR3RLL	**Timer 3 Reload Low Byte.** When operating in one of the auto-reload modes, TMR3RLL holds the reload value for the low byte of Timer 3 (TMR3L). When operating in capture mode, TMR3RLL is the captured value of TMR3L.

26.3. Multiprocessor Communications

9-Bit UART mode supports multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the MCE bit of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic 1 (RB8 = 1) signifying an address byte has been received. In the UART interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its MCE bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their MCE bits set and do not generate interrupts on the reception of the following data bytes, thereby ignoring the data. Once the entire message is received, the addressed slave resets its MCE bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).

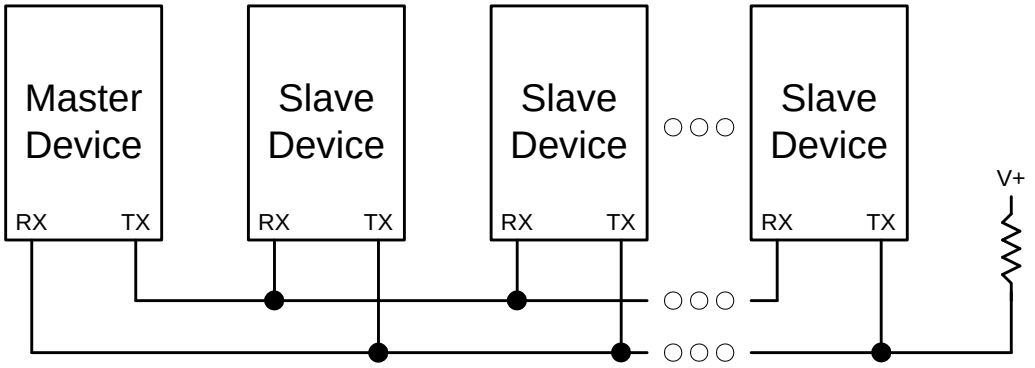

Figure 26.5. UART Multi-Processor Mode Interconnect Diagram

Register 29.4. C2FPCTL: C2 Flash Programming Control

Bit	7	6	5	4	3	2	1	0
Name	C2FPCTL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
C2 Address: 0x02								

Table 29.4. C2FPCTL Register Bit Descriptions

Bit	Name	Function
7:0	C2FPCTL	**Flash Programming Control Register.** This register is used to enable flash programming via the C2 interface. To enable C2 flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 flash programming is enabled, a system reset must be issued to resume normal operation.