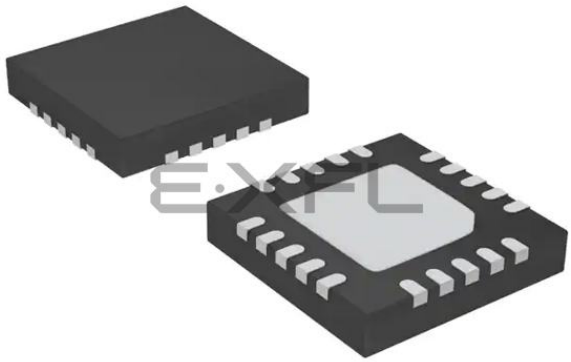

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What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f855-c-im

3.2. C8051F850/1/2/3/4/5 QFN20 Pin Definitions

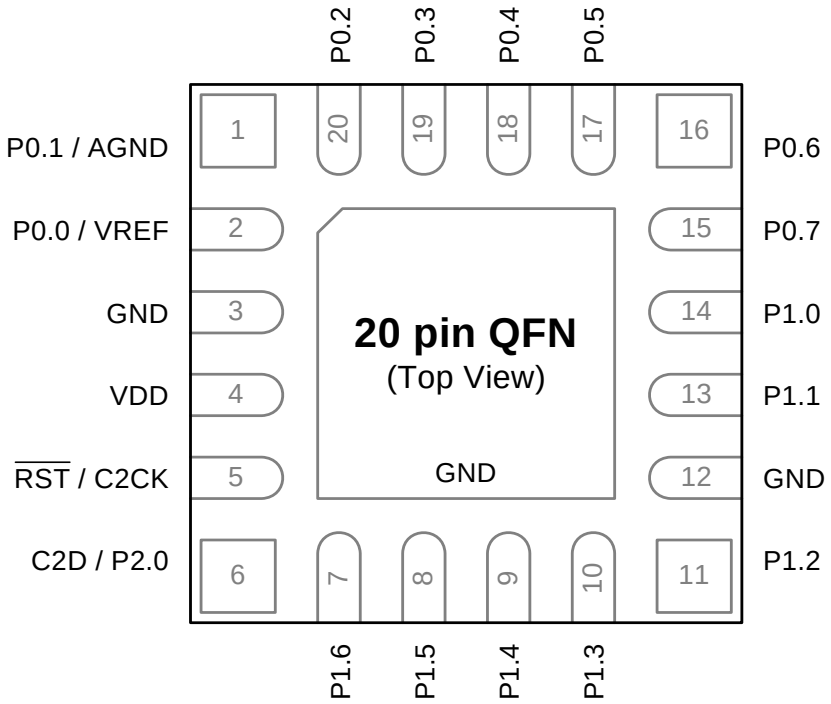

Figure 3.2. C8051F850/1/2/3/4/5-GM and C8051F850/1/2/3/4/5-IM Pinout

Table 3.2. Pin Definitions for C8051F850/1/2/3/4/5-GM and C8051F850/1/2/3/4/5-IM

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	Center 3 12			
VDD	Power	4			
$\overline{\text{RST}}$ / C2CK	Active-low Reset / C2 Debug Clock	5			

3.3. C8051F860/1/2/3/4/5 SOIC16 Pin Definitions

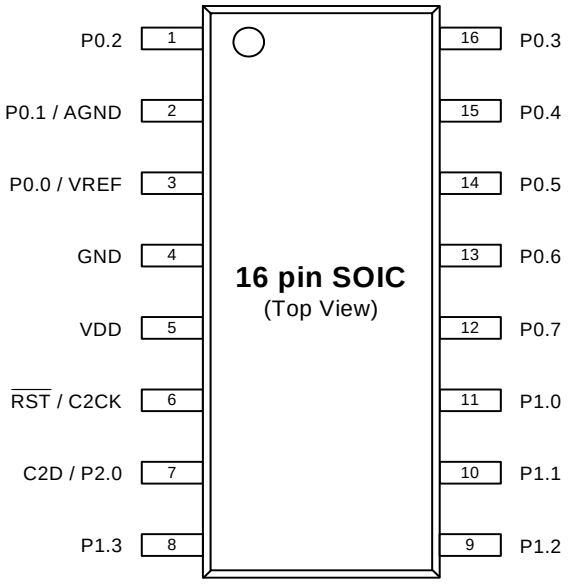

Figure 3.3. C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS Pinout

Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	4			
VDD	Power	5			
RST / C2CK	Active-low Reset / C2 Debug Clock	6			
P0.0	Standard I/O	3	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0

Table 4.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of ADC0 Channels	I/O with Comparator 0/1 Inputs	Pb-free (RoHS Compliant)	AEC-Q100 Qualified	Temperature Range	Package
-IM, -IU and -IS extended temperature range devices (-40 to 125 °C) are also available.									

Table 9.2. Special Function Registers (Continued)

Register	Address	Register Description	Page
IE	0xA8	Interrupt Enable	75
IP	0xB8	Interrupt Priority	77
IT01CF	0xE4	INT0 / INT1 Configuration	150
OSCICL	0xC7	High Frequency Oscillator Calibration	127
OSCLCN	0xB1	Low Frequency Oscillator Control	128
P0	0x80	Port 0 Pin Latch	199
P0MASK	0xFE	Port 0 Mask	197
P0MAT	0xFD	Port 0 Match	198
P0MDIN	0xF1	Port 0 Input Mode	200
P0MDOUT	0xA4	Port 0 Output Mode	201
P0SKIP	0xD4	Port 0 Skip	202
P1	0x90	Port 1 Pin Latch	205
P1MASK	0xEE	Port 1 Mask	203
P1MAT	0xED	Port 1 Match	204
P1MDIN	0xF2	Port 1 Input Mode	206
P1MDOUT	0xA5	Port 1 Output Mode	207
P1SKIP	0xD5	Port 1 Skip	208
P2	0xA0	Port 2 Pin Latch	209
P2MDOUT	0xA6	Port 2 Output Mode	210
PCA0CENT	0x9E	PCA Center Alignment Enable	177
PCA0CLR	0x9C	PCA Comparator Clear Control	170
PCA0CN	0xD8	PCA Control	167
PCA0CPH0	0xFC	PCA Capture Module High Byte 0	175
PCA0CPH1	0xEA	PCA Capture Module High Byte 1	181
PCA0CPH2	0xEC	PCA Capture Module High Byte 2	183
PCA0CPL0	0xFB	PCA Capture Module Low Byte 0	174
PCA0CPL1	0xE9	PCA Capture Module Low Byte 1	180
PCA0CPL2	0xEB	PCA Capture Module Low Byte 2	182

Table 9.2. Special Function Registers (Continued)

Register	Address	Register Description	Page
PCA0CPM0	0xDA	PCA Capture/Compare Mode 0	171
PCA0CPM1	0xDB	PCA Capture/Compare Mode 1	178
PCA0CPM2	0xDC	PCA Capture/Compare Mode 1	179
PCA0H	0xFA	PCA Counter/Timer Low Byte	173
PCA0L	0xF9	PCA Counter/Timer High Byte	172
PCA0MD	0xD9	PCA Mode	168
PCA0POL	0x96	PCA Output Polarity	176
PCA0PWM	0xF7	PCA PWM Configuration	169
PCON	0x87	Power Control	83
PRTDRV	0xF6	Port Drive Strength	196
PSCTL	0x8F	Program Store Control	66
PSW	0xD0	Program Status Word	124
REF0CN	0xD1	Voltage Reference Control	112
REG0CN	0xC9	Voltage Regulator Control	84
REVID	0xB6	Revision Identification	71
RSTSRC	0xEF	Reset Source	215
SBUF0	0x99	UART0 Serial Port Data Buffer	297
SCON0	0x98	UART0 Serial Port Control	295
SMB0ADM	0xD6	SMBus0 Slave Address Mask	257
SMB0ADR	0xD7	SMBus0 Slave Address	256
SMB0CF	0xC1	SMBus0 Configuration	251
SMB0CN	0xC0	SMBus0 Control	254
SMB0DAT	0xC2	SMBus0 Data	258
SMB0TC	0xAC	SMBus0 Timing and Pin Control	253
SP	0x81	Stack Pointer	121
SPI0CFG	0xA1	SPI0 Configuration	227
SPI0CKR	0xA2	SPI0 Clock Control	231
SPI0CN	0xF8	SPI0 Control	229

10. Flash Memory

On-chip, re-programmable flash memory is included for program code and non-volatile data storage. The flash memory is organized in 512-byte pages. It can be erased and written through the C2 interface or from firmware by overloading the MOVX instruction. Any individual byte in flash memory must only be written once between page erase operations.

10.1. Security Options

The CIP-51 provides security options to protect the flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the flash memory from accidental modification by software. PSWE must be explicitly set to '1' before software can modify the flash memory; both PSWE and PSEE must be set to '1' before software can erase flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located in flash user space offers protection of the flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. See Section "8. Memory Organization" on page 52 for the location of the security byte. The flash security mechanism allows the user to lock *n* 512-byte flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where *n* is the 1's complement number represented by the Security Lock Byte. **Note that the page containing the flash Security Lock Byte is unlocked when no other flash pages are locked (all bits of the Lock Byte are '1') and locked when any other flash pages are locked (any bit of the Lock Byte is '0').** An example is shown in Figure 10.1.

Security Lock Byte:	11111101b
1s Complement:	00000010b
Flash pages locked:	3 (First two flash pages + Lock Byte Page)

Figure 10.1. Security Byte Decoding

The level of flash security depends on the flash access method. The three flash access methods that can be restricted are reads, writes, and erases from the C2 debug interface, user firmware executing on unlocked pages, and user firmware executing on locked pages. Table 10.1 summarizes the flash security features of the C8051F85x/86x devices.

Table 10.1. Flash Security Summary

Action	C2 Debug Interface	User Firmware executing from:	
		an unlocked page	a locked page
Read, Write or Erase unlocked pages (except page with Lock Byte)	Permitted	Permitted	Permitted
Read, Write or Erase locked pages (except page with Lock Byte)	Not Permitted	Flash Error Reset	Permitted
Read or Write page containing Lock Byte (if no pages are locked)	Permitted	Permitted	N/A
Read or Write page containing Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted

Register 11.3. REVID: Revision Identifcation

Bit	7	6	5	4	3	2	1	0
Name	REVID							
Type	R							
Reset	X	X	X	X	X	X	X	X
SFR Address: 0xB6								

Table 11.4. REVID Register Bit Descriptions

Bit	Name	Function
7:0	REVID	**Revision ID.** This read-only register returns the 8-bit revision ID. 00000000: Revision A 00000001: Revision B 00000010: Revision C 00000011-11111111: Reserved.

14.10. ADC Control Registers

Register 14.1. ADC0CN0: ADC0 Control 0

Bit	7	6	5	4	3	2	1	0
Name	ADEN	ADBMEN	ADINT	ADBUSY	ADWINT	ADCM		
Type	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xE8 (bit-addressable)								

Table 14.4. ADC0CN0 Register Bit Descriptions

Bit	Name	Function
7	ADEN	**Enable.** 0: ADC0 Disabled (low-power shutdown). 1: ADC0 Enabled (active and ready for data conversions).
6	ADBMEN	**Burst Mode Enable.** 0: ADC0 Burst Mode Disabled. 1: ADC0 Burst Mode Enabled.
5	ADINT	**Conversion Complete Interrupt Flag.** Set by hardware upon completion of a data conversion (ADBMEN=0), or a burst of conversions (ADBMEN=1). Can trigger an interrupt. Must be cleared by software.
4	ADBUSY	**ADC Busy.** Writing 1 to this bit initiates an ADC conversion when ADC0CM = 000. This bit should not be polled to indicate when a conversion is complete. Instead, the ADINT bit should be used when polling for conversion completion.
3	ADWINT	**Window Compare Interrupt Flag.** Set by hardware when the contents of ADC0H:ADC0L fall within the window specified by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL. Can trigger an interrupt. Must be cleared by software.
2:0	ADCM	**Start of Conversion Mode Select.** Specifies the ADC0 start of conversion source. All remaining bit combinations are reserved. 000: ADC0 conversion initiated on write of 1 to ADBUSY. 001: ADC0 conversion initiated on overflow of Timer 0. 010: ADC0 conversion initiated on overflow of Timer 2. 011: ADC0 conversion initiated on overflow of Timer 3. 100: ADC0 conversion initiated on rising edge of CNVSTR. 101-111: Reserved.

Register 14.4. ADC0AC: ADC0 Accumulator Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD12BE	ADAE	ADSJST			ADRPT		
Type	RW	RW	RW			RW		
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xB3								

Table 14.7. ADC0AC Register Bit Descriptions

Bit	Name	Function
7	AD12BE	**12-Bit Mode Enable.** Enables 12-bit Mode. In 12-bit mode, the ADC throughput is reduced by a factor of 4. 0: 12-bit Mode Disabled. 1: 12-bit Mode Enabled.
6	ADAE	**Accumulate Enable.** Enables multiple conversions to be accumulated when burst mode is disabled. 0: ADC0H:ADC0L contain the result of the latest conversion when Burst Mode is disabled. 1: ADC0H:ADC0L contain the accumulated conversion results when Burst Mode is disabled. Software must write 0x0000 to ADC0H:ADC0L to clear the accumulated result.
5:3	ADSJST	**Accumulator Shift and Justify.** Specifies the format of data read from ADC0H:ADC0L. All remaining bit combinations are reserved. 000: Right justified. No shifting applied. 001: Right justified. Shifted right by 1 bit. 010: Right justified. Shifted right by 2 bits. 011: Right justified. Shifted right by 3 bits. 100: Left justified. No shifting applied. 101-111: Reserved.
2:0	ADRPT	**Repeat Count.** Selects the number of conversions to perform and accumulate in Burst Mode. This bit field must be set to 000 if Burst Mode is disabled. 000: Perform and Accumulate 1 conversion (not used in 12-bit mode). 001: Perform and Accumulate 4 conversions (1 conversion in 12-bit mode). 010: Perform and Accumulate 8 conversions (2 conversions in 12-bit mode). 011: Perform and Accumulate 16 conversions (4 conversions in 12-bit mode). 100: Perform and Accumulate 32 conversions (8 conversions in 12-bit mode). 101: Perform and Accumulate 64 conversions (16 conversions in 12-bit mode). 110-111: Reserved.

20.3.4. High-Speed Output Mode

In High-Speed Output mode, a module's associated CEXn pin is toggled each time a match occurs between the PCA Counter and the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode. If ECOMn is cleared, the associated pin will retain its state, and not toggle on the next match event.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

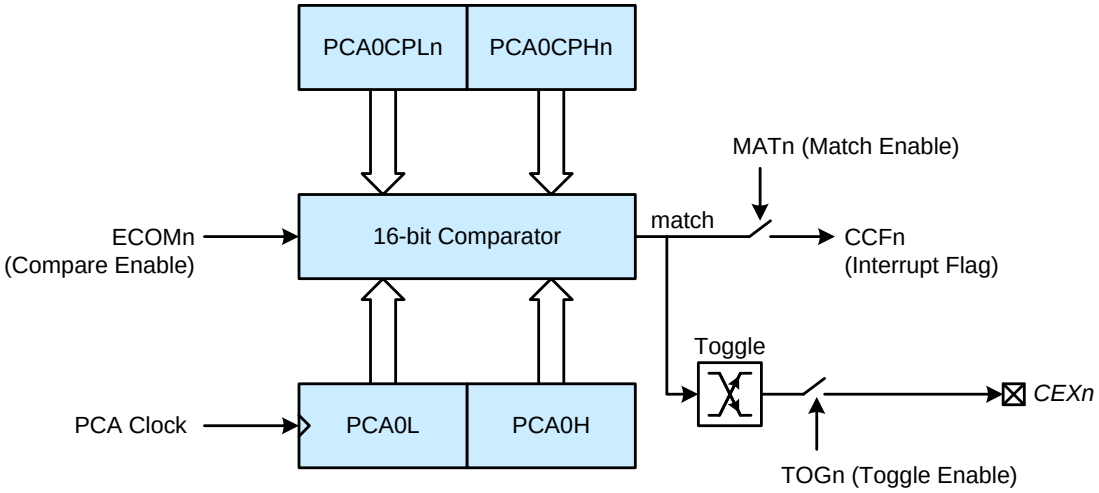

Figure 20.4. PCA High-Speed Output Mode Diagram

20.4. PWM Waveform Generation

The PCA can generate edge- or center-aligned PWM waveforms with resolutions of 8, 9, 10, 11 or 16 bits. PWM resolution depends on the module setup, as specified within the individual module PCA0CPMn registers as well as the PCA0PWM register. Modules can be configured for 8-11 bit mode, or for 16-bit mode individually using the PCA0CPMn registers. All modules configured for 8-11 bit mode will have the same resolution, specified by the PCA0PWM register. When operating in one of the PWM modes, each module may be individually configured for center or edge-aligned PWM waveforms. Each channel has a single bit in the PCA0CENT register to select between the two options.

20.4.1. Edge Aligned PWM

When configured for edge-aligned mode, a module will generate an edge transition at two points for every 2^N PCA clock cycles, where N is the selected PWM resolution in bits. In edge-aligned mode, these two edges are referred to as the “match” and “overflow” edges. The polarity at the output pin is selectable, and can be inverted by setting the appropriate channel bit to ‘1’ in the PCA0POL register. Prior to inversion, a match edge sets the channel to logic high, and an overflow edge clears the channel to logic low.

The match edge occurs when the the lowest N bits of the module’s PCA0CPn register match the corresponding bits of the main PCA0 counter register. For example, with 10-bit PWM, the match edge will occur any time bits 9-0 of the PCA0CPn register match bits 9-0 of the PCA0 counter value.

The overflow edge occurs when an overflow of the PCA0 counter happens at the desired resolution. For example, with 10-bit PWM, the overflow edge will occur when bits 0-9 of the PCA0 counter transition from all 1’s to all 0’s. All modules configured for edge-aligned mode at the same resolution will align on the overflow edge of the waveforms.

An example of the PWM timing in edge-aligned mode for two channels is shown in Figure 20.6. In this example, the CEX0POL and CEX1POL bits are cleared to 0.

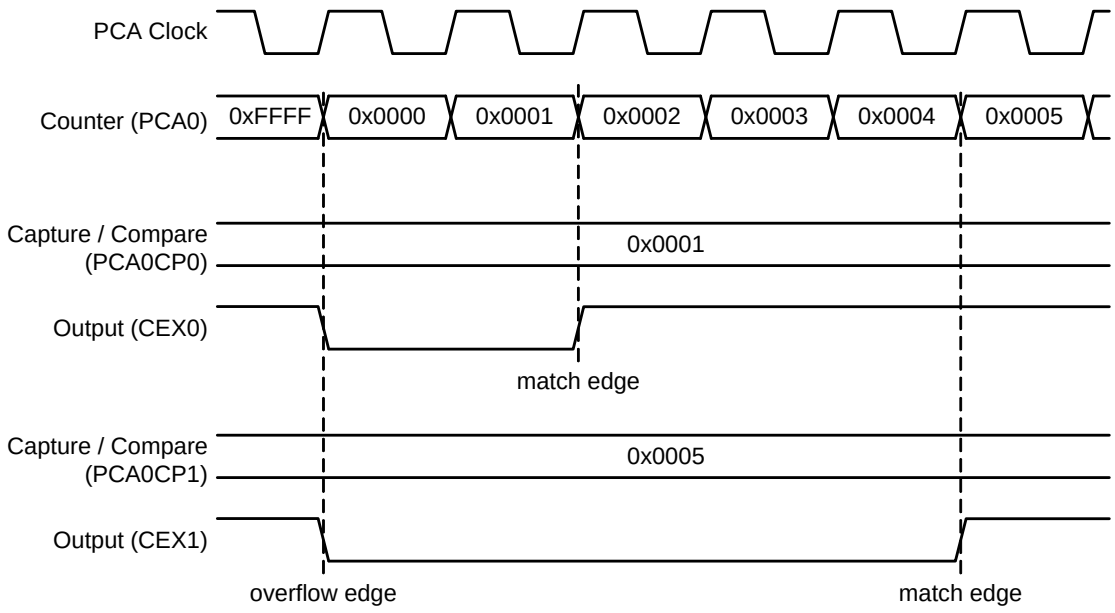

Figure 20.6. Edge-Aligned PWM Timing

For a given PCA resolution, the unused high bits in the PCA0 counter and the PCA0CPn compare registers are ignored, and only the used bits of the PCA0CPn register determine the duty cycle. Equation 20.2 describes the duty cycle when CEXnPOL in the PCA0POL regsiter is cleared to 0. Equation 20.3 describes the duty cycle when CEXnPOL in the PCA0POL regsiter is set to 1. A 0% duty cycle for the channel (with CEXnPOL = 0) is achieved by clearing the module’s ECOM bit to 0. This will

20.4.4. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. 16-bit PWM mode is independent of the other (8 through 11-bit) PWM modes. The entire PCA0CP register is used to determine the duty cycle in 16-bit PWM mode.

To output a varying duty cycle, new value writes should be synchronized with the PCA CCFn match flag to ensure seamless updates.

16-Bit PWM mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, the match interrupt flag should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. If the MATn bit is set to 1, the CCFn flag for the module will be set each time a match edge or up edge occurs. The CF flag in PCA0CN can be used to detect the overflow or down edge.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

Register 21.9. P0MDOUT: Port 0 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDOUT							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xA4								

Table 21.12. P0MDOUT Register Bit Descriptions

Bit	Name	Function
7:0	P0MDOUT	**Port 0 Output Mode.** These bits are only applicable when the pin is configured for digital mode using the P0MDIN register. 0: Corresponding P0.n Output is open-drain. 1: Corresponding P0.n Output is push-pull.

24. System Management Bus / I^{2}C (SMBus0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^{2}C serial bus.

Reads and writes to the SMBus by the system controller are byte oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/20th of the system clock as a master or slave (this can be faster than allowed by the SMBus specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation. The SMBus peripherals can be fully driven by software (i.e., software accepts/rejects slave addresses, and generates ACKs), or hardware slave address recognition and automatic ACK generation can be enabled to minimize software overhead. A block diagram of the SMBus0 peripheral is shown in Figure 24.1.

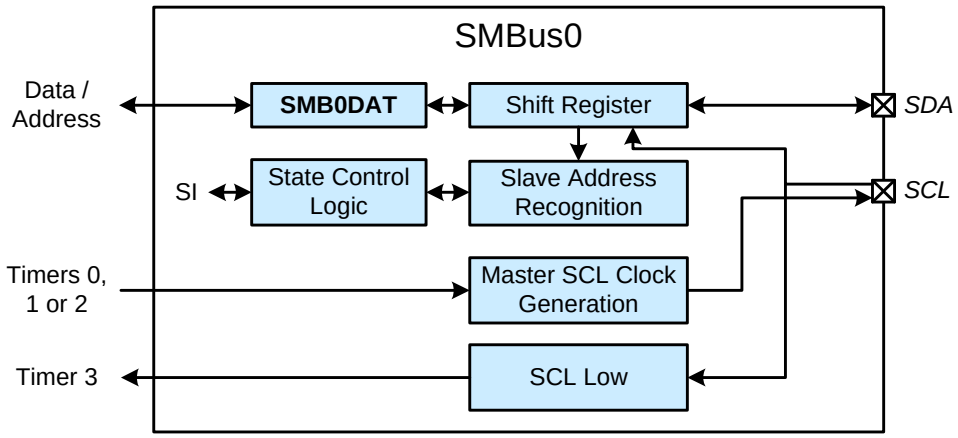

Figure 24.1. SMBus0 Block Diagram

Table 24.4. Hardware Address Recognition Examples (EHACK = 1)

Hardware Slave Address SLV	Slave Address Mask SLVM	GC bit	Slave Addresses Recognized by Hardware
0x34	0x7E	1	0x34, 0x35, 0x00 (General Call)
0x70	0x73	0	0x70, 0x74, 0x78, 0x7C

24.4.6. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

Register 24.5. SMB0ADM: SMBus0 Slave Address Mask

Bit	7	6	5	4	3	2	1	0
Name	SLVM							EHACK
Type	RW							RW
Reset	1	1	1	1	1	1	1	0
SFR Address: 0xD6								

Table 24.11. SMB0ADM Register Bit Descriptions

Bit	Name	Function
7:1	SLVM	**SMBus0 Slave Address Mask.** Defines which bits of register SMB0ADR are compared with an incoming address byte, and which bits are ignored. Any bit set to 1 in SLVM enables comparisons with the corresponding bit in SLV. Bits set to 0 are ignored (can be either 0 or 1 in the incoming address).
0	EHACK	**Hardware Acknowledge Enable.** Enables hardware acknowledgement of slave address and received data bytes. 0: Firmware must manually acknowledge all incoming address and data bytes. 1: Automatic slave address recognition and hardware acknowledge is enabled.

Register 25.3. TMOD: Timer 0/1 Mode

Bit	7	6	5	4	3	2	1	0
Name	GATE1	CT1	T1M		GATE0	CT0	T0M	
Type	RW	RW	RW		RW	RW	RW	
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x89								

Table 25.5. TMOD Register Bit Descriptions

Bit	Name	Function
7	GATE1	**Timer 1 Gate Control.** 0: Timer 1 enabled when TR1 = 1 irrespective of INT1 logic level. 1: Timer 1 enabled only when TR1 = 1 and INT1 is active as defined by bit IN1PL in register IT01CF.
6	CT1	**Counter/Timer 1 Select.** 0: Timer Mode. Timer 1 increments on the clock defined by T1M in the CKCON register. 1: Counter Mode. Timer 1 increments on high-to-low transitions of an external pin (T1).
5:4	T1M	**Timer 1 Mode Select.** These bits select the Timer 1 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Timer 1 Inactive
3	GATE0	**Timer 0 Gate Control.** 0: Timer 0 enabled when TR0 = 1 irrespective of INT0 logic level. 1: Timer 0 enabled only when TR0 = 1 and INT0 is active as defined by bit IN0PL in register IT01CF.
2	CT0	**Counter/Timer 0 Select.** 0: Timer Mode. Timer 0 increments on the clock defined by T0M in the CKCON register. 1: Counter Mode. Timer 0 increments on high-to-low transitions of an external pin (T0).
1:0	T0M	**Timer 0 Mode Select.** These bits select the Timer 0 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Two 8-bit Counter/Timers

Table 25.15. TMR3CN Register Bit Descriptions

Bit	Name	Function
0	T3XCLK	**Timer 3 External Clock Select.** This bit selects the external clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 3 clock is the system clock divided by 12. 1: Timer 3 clock is the external clock divided by 8 (synchronized with SYSCLK).

Register 25.16. TMR3L: Timer 3 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3L							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x94								

Table 25.18. TMR3L Register Bit Descriptions

Bit	Name	Function
7:0	TMR3L	**Timer 3 Low Byte.** In 16-bit mode, the TMR3L register contains the low byte of the 16-bit Timer 3. In 8-bit mode, TMR3L contains the 8-bit low byte timer value.