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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f855-c-iur

Table 1.10. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPnMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
Response Time, CPnMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.5	—	µs
		–100 mV Differential	—	3.5	—	µs
Positive Hysterisis Mode 0 (CPnMD = 00)	HYS_{CP+}	CPnHYP = 00	—	0.4	—	mV
		CPnHYP = 01	—	8	—	mV
		CPnHYP = 10	—	16	—	mV
		CPnHYP = 11	—	32	—	mV
Negative Hysterisis Mode 0 (CPnMD = 00)	HYS_{CP-}	CPnHYN = 00	—	-0.4	—	mV
		CPnHYN = 01	—	–8	—	mV
		CPnHYN = 10	—	–16	—	mV
		CPnHYN = 11	—	–32	—	mV
Positive Hysterisis Mode 1 (CPnMD = 01)	HYS_{CP+}	CPnHYP = 00	—	0.5	—	mV
		CPnHYP = 01	—	6	—	mV
		CPnHYP = 10	—	12	—	mV
		CPnHYP = 11	—	24	—	mV
Negative Hysterisis Mode 1 (CPnMD = 01)	HYS_{CP-}	CPnHYN = 00	—	-0.5	—	mV
		CPnHYN = 01	—	–6	—	mV
		CPnHYN = 10	—	–12	—	mV
		CPnHYN = 11	—	–24	—	mV
Positive Hysterisis Mode 2 (CPnMD = 10)	HYS_{CP+}	CPnHYP = 00	—	0.7	—	mV
		CPnHYP = 01	—	4.5	—	mV
		CPnHYP = 10	—	9	—	mV
		CPnHYP = 11	—	18	—	mV
Negative Hysterisis Mode 2 (CPnMD = 10)	HYS_{CP-}	CPnHYN = 00	—	-0.6	—	mV
		CPnHYN = 01	—	–4.5	—	mV
		CPnHYN = 10	—	–9	—	mV
		CPnHYN = 11	—	–18	—	mV

2.1.3.1. Normal Mode

Normal mode encompasses the typical full-speed operation. The power consumption of the device in this mode will vary depending on the system clock speed and any analog peripherals that are enabled.

2.1.3.2. Idle Mode

Setting the IDLE bit in PCON causes the hardware to halt the CPU and enter idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the IDLE bit to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

2.1.3.3. Stop Mode (Regulator On)

Setting the STOP bit in PCON when STOPCF in REG0CN is clear causes the controller core to enter stop mode as soon as the instruction that sets the bit completes execution. In stop mode the internal oscillator, CPU, and all digital peripherals are stopped. Each analog peripheral may be shut down individually prior to entering stop mode. Stop mode can only be terminated by an internal or external reset.

2.1.3.4. Shutdown Mode (Regulator Off)

Shutdown mode is an extension of the normal stop mode operation. Setting the STOP bit in PCON when STOPCF in REG0CN is also set causes the controller core to enter shutdown mode as soon as the instruction that sets the bit completes execution, and then the internal regulator is powered down. In shutdown mode, all core functions, memories and peripherals are powered off. An external pin reset or power-on reset is required to exit shutdown mode.

2.2. I/O

2.2.1. General Features

The C8051F85x/86x ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes.
- Port Match allows the device to recognize a change on a port pin value and wake from idle mode or generate an interrupt.
- Internal pull-up resistors can be globally enabled or disabled.
- Two external interrupts provide unique interrupt vectors for monitoring time-critical events.
- Above-rail tolerance allows 5 V interface when device is powered.

2.2.2. Crossbar

The C8051F85x/86x devices have a digital peripheral crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PnSKIP registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.

3.3. C8051F860/1/2/3/4/5 SOIC16 Pin Definitions

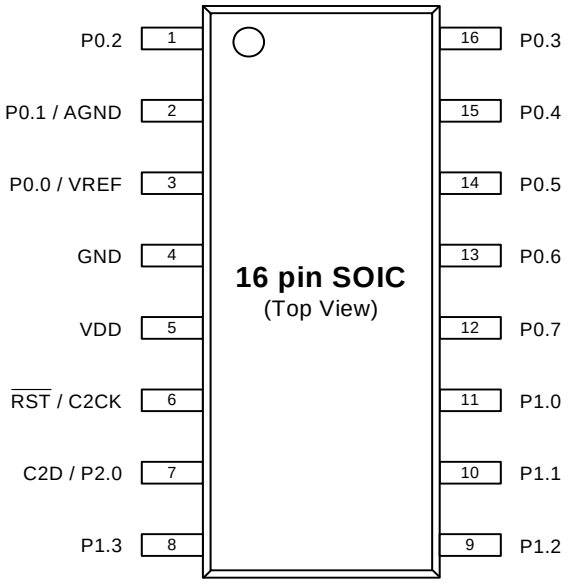

Figure 3.3. C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS Pinout

Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	4			
VDD	Power	5			
RST / C2CK	Active-low Reset / C2 Debug Clock	6			
P0.0	Standard I/O	3	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0

9. Special Function Register Memory Map

This section details the special function register memory map for the C8051F85x/86x devices.

Table 9.1. Special Function Register (SFR) Memory Map

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	P0MAT	P0MASK	VDM0CN
F0	B	P0MDIN	P1MDIN	EIP1	-	-	PRTDRV	PCA0PWM
E8	ADC0CN0	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	P1MAT	P1MASK	RSTSRC
E0	ACC	XBR0	XBR1	XBR2	IT01CF	-	EIE1	-
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	CRC0IN	CRC0DAT	ADC0PWR
D0	PSW	REF0CN	CRC0AUTO	CRC0CNT	P0SKIP	P1SKIP	SMB0ADM	SMB0ADR
C8	TMR2CN	REG0CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H	CRC0CN	CRC0FLIP
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	OSCICL
B8	IP	ADC0TK	-	ADC0MX	ADC0CF	ADC0L	ADC0H	CPT1CN
B0	-	OSCLCN	ADC0CN1	ADC0AC	-	DEVICEID	REVID	FLKEY
A8	IE	CLKSEL	CPT1MX	CPT1MD	SMB0TC	DERIVID	-	-
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	-
98	SCON0	SBUF0	-	CPT0CN	PCA0CLR	CPT0MD	PCA0CENT	CPT0MX
90	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	PCA0POL	WDTCN
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH	-	-	-	PCON
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

(bit addressable)

Table 9.2. Special Function Registers

Register	Address	Register Description	Page
ACC	0xE0	Accumulator	122
ADC0AC	0xB3	ADC0 Accumulator Configuration	102
ADC0CF	0xBC	ADC0 Configuration	101
ADC0CN0	0xE8	ADC0 Control 0	99
ADC0CN1	0xB2	ADC0 Control 1	100
ADC0GTH	0xC4	ADC0 Greater-Than High Byte	107
ADC0GTL	0xC3	ADC0 Greater-Than Low Byte	108
ADC0H	0xBE	ADC0 Data Word High Byte	105

The ADSJST bits can be used to format the contents of the 16-bit accumulator. The accumulated result can be shifted right by 1, 2, or 3 bit positions. Based on the principles of oversampling and averaging, the effective ADC resolution increases by 1 bit each time the oversampling rate is increased by a factor of 4. The example below shows how to increase the effective ADC resolution by 1, 2, and 3 bits to obtain an effective ADC resolution of 11-bit, 12-bit, or 13-bit respectively without CPU intervention.

Input Voltage	**Repeat Count = 4** **Shift Right = 1** **11-Bit Result**	**Repeat Count = 16** **Shift Right = 2** **12-Bit Result**	**Repeat Count = 64** **Shift Right = 3** **13-Bit Result**
V_{REF} x 1023/1024	0x07F7	0x0FFC	0x1FF8
V_{REF} x 512/1024	0x0400	0x0800	0x1000
V_{REF} x 511/1024	0x03FE	0x04FC	0x0FF8
0	0x0000	0x0000	0x0000

14.7. Programmable Window Detector

The ADC Programmable Window Detector continuously compares the ADC0 output registers to user-programmed limits, and notifies the system when a desired condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (ADWINT in register ADC0CN0) can also be used in polled mode. The ADC0 Greater-Than (ADC0GTH, ADC0GTL) and Less-Than (ADC0LTH, ADC0LTL) registers hold the comparison values. The window detector flag can be programmed to indicate when measured data is inside or outside of the user-programmed limits, depending on the contents of the ADC0 Less-Than and ADC0 Greater-Than registers.

14.7.1. Window Detector In Single-Ended Mode

Figure 14.6 shows two example window comparisons for right-justified data, with ADC0LTH:ADC0LTL = 0x0080 (128d) and ADC0GTH:ADC0GTL = 0x0040 (64d). The input voltage can range from 0 to VREF x (1023/1024) with respect to GND, and is represented by a 10-bit unsigned integer value. In the left example, an ADWINT interrupt will be generated if the ADC0 conversion word (ADC0H:ADC0L) is within the range defined by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL (if 0x0040 < ADC0H:ADC0L < 0x0080). In the right example, and ADWINT interrupt will be generated if the ADC0 conversion word is outside of the range defined by the ADC0GT and ADC0LT registers (if ADC0H:ADC0L < 0x0040 or ADC0H:ADC0L > 0x0080). Figure 14.7 shows an example using left-justified data with the same comparison values.

Register 14.10. ADC0GTL: ADC0 Greater-Than Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTL							
Type	RW							
Reset	1	1	1	1	1	1	1	1
SFR Address: 0xC3								

Table 14.13. ADC0GTL Register Bit Descriptions

Bit	Name	Function
7:0	ADC0GTL	**Greater-Than Low Byte.** Least Significant Byte of the 16-bit Greater-Than window compare register.
Note: In 8-bit mode, this register should be set to 0x00.		

Register 14.11. ADC0LTH: ADC0 Less-Than High Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0LTH							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xC6								

Table 14.14. ADC0LTH Register Bit Descriptions

Bit	Name	Function
7:0	ADC0LTH	**Less-Than High Byte.** Most Significant Byte of the 16-bit Less-Than window compare register.

Table 15.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
XRL A, Rn	Exclusive-OR Register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR indirect RAM to A	1	2
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	2
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through Carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through Carry	1	1
SWAP A	Swap nibbles of A	1	1
Data Transfer			
MOV A, Rn	Move Register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move indirect RAM to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to Register	1	1
MOV Rn, direct	Move direct byte to Register	2	2
MOV Rn, #data	Move immediate to Register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move Register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2

17.2. Functional Description

The comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the port pins: a synchronous “latched” output (CPn), or an asynchronous “raw” output (CPnA). The asynchronous CPnA signal is available even when the system clock is not active. This allows the comparator to operate and generate an output with the device in STOP mode.

When disabled, the comparator output (if assigned to a port I/O pin via the crossbar) defaults to the logic low state, and the power supply to the comparator is turned off.

The comparator response time may be configured in software via the CPTnMD register. Selecting a longer response time reduces the comparator supply current.

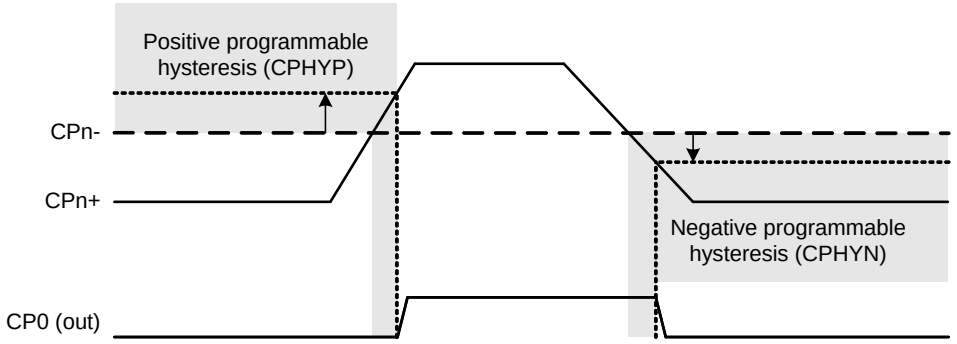

Figure 17.2. Comparator Hysteresis Plot

The comparator hysteresis is software-programmable via its Comparator Control register CPTnCN. The user can program both the amount of hysteresis voltage (referred to the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage.

The comparator hysteresis is programmable using the CPHYN and CPHYP fields in the Comparator Control Register CPTnCN. The amount of negative hysteresis voltage is determined by the settings of the CPHYN bits. As shown in Figure 17.2, settings of 20, 10, or 5 mV (nominal) of negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of positive hysteresis is determined by the setting the CPHYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. The CPFIF flag is set to logic 1 upon a comparator falling-edge occurrence, and the CPRIF flag is set to logic 1 upon the comparator rising-edge occurrence. Once set, these bits remain set until cleared by software. The comparator rising-edge interrupt mask is enabled by setting CPRIE to a logic 1. The comparator falling-edge interrupt mask is enabled by setting CPFIE to a logic 1.

The output state of the comparator can be obtained at any time by reading the CPOUT bit. The comparator is enabled by setting the CPEN bit to logic 1, and is disabled by clearing this bit to logic 0.

Note that false rising edges and falling edges can be detected when the comparator is first powered on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed, before enabling comparator interrupts.

Table 19.1. IT01CF Register Bit Descriptions

Bit	Name	Function
2:0	IN0SL	**INT0 Port Pin Selection Bits.** These bits select which Port pin is assigned to INT0. This pin assignment is independent of the Crossbar; INT0 will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7

20.3. Capture/Compare Modules

Each module can be configured to operate independently in one of six operation modes: edge-triggered capture, software timer, high-speed output, frequency output, 8 to 11-bit pulse width modulator, or 16-bit pulse width modulator. Table 20.2 summarizes the bit settings in the PCA0CPMn and PCA0PWM registers used to select the PCA capture/compare module's operating mode. Note that all modules set to use 8-, 9-, 10-, or 11-bit PWM mode must use the same cycle length (8–11 bits). Setting the ECCFn bit in a PCA0CPMn register enables the module's CCFn interrupt.

Table 20.2. PCA0CPM and PCA0PWM Bit Settings for PCA Capture/Compare Modules

Operational Mode	PCA0CPMn								PCA0PWM				
Bit Number	7	6	5	4	3	2	1	0	7	6	5	4–3	2–0
Capture triggered by positive edge on CEXn	X	X	1	0	0	0	0	A	0	X	B	XX	XXX
Capture triggered by negative edge on CEXn	X	X	0	1	0	0	0	A	0	X	B	XX	XXX
Capture triggered by any transition on CEXn	X	X	1	1	0	0	0	A	0	X	B	XX	XXX
Software Timer	X	C	0	0	1	0	0	A	0	X	B	XX	XXX
High Speed Output	X	C	0	0	1	1	0	A	0	X	B	XX	XXX
Frequency Output	X	C	0	0	0	1	1	A	0	X	B	XX	XXX
8-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	0	X	B	XX	000
9-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XX	001
10-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XX	010
11-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XX	011
16-Bit Pulse Width Modulator	1	C	0	0	E	0	1	A	0	X	B	XX	XXX

Notes:
1. X = Don't Care (no functional difference for individual module if 1 or 0).
2. A = Enable interrupts for this module (PCA interrupt triggered on CCFn set to 1).
3. B = Enable 8th - 11th bit overflow interrupt (Depends on setting of CLSEL).
4. C = When set to 0, the digital comparator is off. For high speed and frequency output modes, the associated pin will not toggle. In any of the PWM modes, this generates a 0% duty cycle (output = 0).
5. D = Selects whether the Capture/Compare register (0) or the Auto-Reload register (1) for the associated channel is accessed via addresses PCA0CPHn and PCA0CPLn.
6. E = When set, a match event will cause the CCFn flag for the associated channel to be set.
7. All modules set to 8, 9, 10 or 11-bit PWM mode use the same cycle length setting.

20.3.1. Output Polarity

The output polarity of each PCA channel is individually selectable using the PCA0POL register. By default, all output channels are configured to drive the PCA output signals (CEXn) with their internal polarity. When the CEXnPOL bit for a specific channel is set to 1, that channel's output signal will be inverted at the pin. All other properties of the channel are unaffected, and the inversion does not apply to PCA input signals. Note that changes in the PCA0POL register take effect immediately at the associated output pin.

20.4.2. Center Aligned PWM

When configured for center-aligned mode, a module will generate an edge transition at two points for every $2^{(N+1)}$ PCA clock cycles, where N is the selected PWM resolution in bits. In center-aligned mode, these two edges are referred to as the “up” and “down” edges. The polarity at the output pin is selectable, and can be inverted by setting the appropriate channel bit to ‘1’ in the PCA0POL register.

The generated waveforms are centered about the points where the lower N bits of the PCA0 counter are zero. The $(N+1)^{th}$ bit in the PCA0 counter acts as a selection between up and down edges. In 16-bit mode, a special 17th bit is implemented internally for this purpose. At the center point, the (non-inverted) channel output will be low when the $(N+1)^{th}$ bit is ‘0’ and high when the $(N+1)^{th}$ bit is ‘1’, except for cases of 0% and 100% duty cycle. Prior to inversion, an up edge sets the channel to logic high, and a down edge clears the channel to logic low.

Down edges occur when the $(N+1)^{th}$ bit in the PCA0 counter is one, and a logical inversion of the value in the module’s PCA0CPn register matches the main PCA0 counter register for the lowest N bits. For example, with 10-bit PWM, the down edge will occur when the one’s complement of bits 9-0 of the PCA0CPn register match bits 9-0 of the PCA0 counter, and bit 10 of the PCA0 counter is ‘1’.

Up edges occur when the $(N+1)^{th}$ bit in the PCA0 counter is zero, and the lowest N bits of the module’s PCA0CPn register match the value of (PCA0 - 1). For example, with 10-bit PWM, the up edge will occur when bits 9-0 of the PCA0CPn register are one less than bits 9-0 of the PCA0 counter, and bit 10 of the PCA0 counter is ‘0’.

An example of the PWM timing in center-aligned mode for two channels is shown in Figure 20.7. In this example, the CEX0POL and CEX1POL bits are cleared to 0.

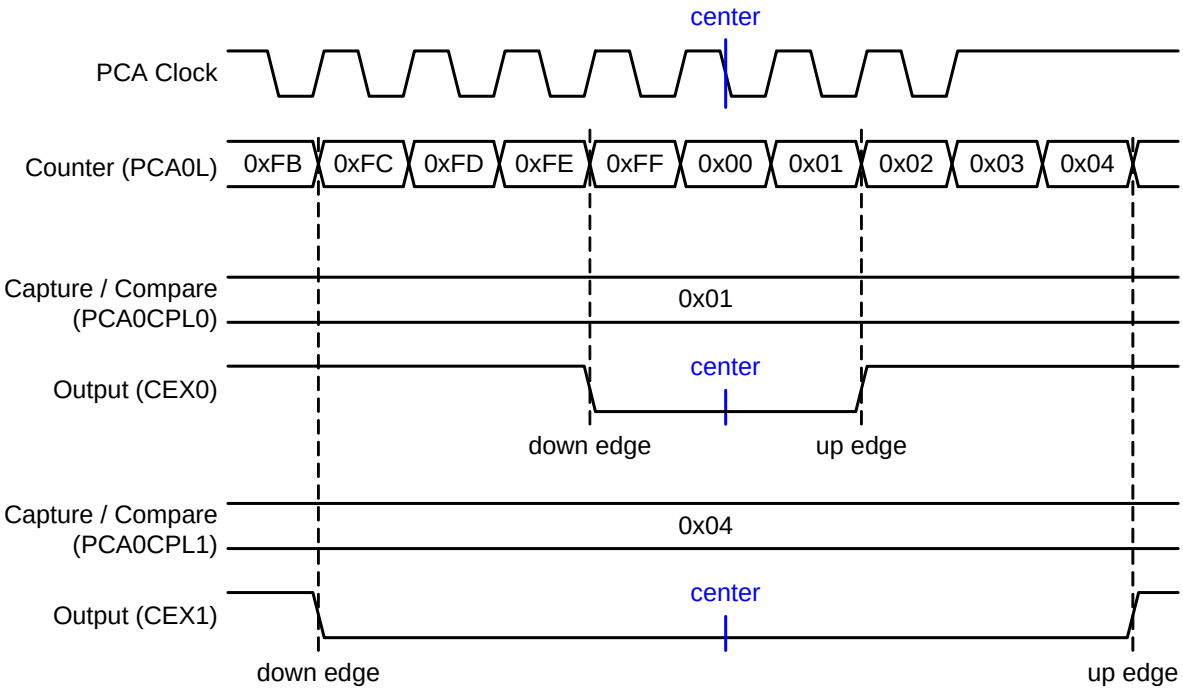

Figure 20.7. Center-Aligned PWM Timing

Register 20.7. PCA0H: PCA Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0H							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xFA								

Table 20.9. PCA0H Register Bit Descriptions

Bit	Name	Function
7:0	PCA0H	**PCA Counter/Timer High Byte.** The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer. Reads of this register will read the contents of a snapshot register, whose contents are updated only when the contents of PCA0L are read.

Register 20.11. PCA0CENT: PCA Center Alignment Enable

Bit	7	6	5	4	3	2	1	0
Name	Reserved					CEX2CEN	CEX1CEN	CEX0CEN
Type	R					RW	RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x9E								

Table 20.13. PCA0CENT Register Bit Descriptions

Bit	Name	Function
7:3	Reserved	Must write reset value.
2	CEX2CEN	**CEX2 Center Alignment Enable.** Selects the alignment properties of the CEX2 output channel when operated in any of the PWM modes. This bit does not affect the operation of non-PWM modes. 0: Edge-aligned. 1: Center-aligned.
1	CEX1CEN	**CEX1 Center Alignment Enable.** Selects the alignment properties of the CEX1 output channel when operated in any of the PWM modes. This bit does not affect the operation of non-PWM modes. 0: Edge-aligned. 1: Center-aligned.
0	CEX0CEN	**CEX0 Center Alignment Enable.** Selects the alignment properties of the CEX0 output channel when operated in any of the PWM modes. This bit does not affect the operation of non-PWM modes. 0: Edge-aligned. 1: Center-aligned.

Register 20.17. PCA0CPH2: PCA Capture Module High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPH2							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xEC								

Table 20.19. PCA0CPH2 Register Bit Descriptions

Bit	Name	Function
7:0	PCA0CPH2	**PCA Capture Module High Byte.** The PCA0CPH2 register holds the high byte (MSB) of the 16-bit capture module.This register address also allows access to the high byte of the corresponding PCA channels auto-reload value for 9 to 11-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.
Note: A write to this register will set the modules ECOM bit to a 1.		

Register 21.11. P1MASK: Port 1 Mask

Bit	7	6	5	4	3	2	1	0
Name	P1MASK							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xEE								

Table 21.14. P1MASK Register Bit Descriptions

Bit	Name	Function
7:0	P1MASK	**Port 1 Mask Value.** Selects P1 pins to be compared to the corresponding bits in P1MAT. 0: P1.x pin logic value is ignored and will cause a port mismatch event. 1: P1.x pin logic value is compared to P1MAT.x.
Note: Port 1 consists of 8 bits (P1.0-P1.7) on QSOP24 packages and 7 bits (P1.0-P1.6) on QFN20 packages and 4 bits (P1.0-P1.3) on SOIC16 packages.		

Table 23.2. SPI0CFG Register Bit Descriptions

Bit	Name	Function
0	RXBMT	**Receive Buffer Empty (valid in slave mode only).** This bit will be set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0. RXBMT = 1 when in Master Mode.
Note: In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device.		

Table 24.7. SMB0CF Register Bit Descriptions

Bit	Name	Function
1:0	SMBCS	**SMBus0 Clock Source Selection.** These two bits select the SMBus0 clock source, which is used to generate the SMBus0 bit rate. See the SMBus clock timing section for additional details. 00: Timer 0 Overflow 01: Timer 1 Overflow 10: Timer 2 High Byte Overflow 11: Timer 2 Low Byte Overflow

Table 24.9. SMB0CN Register Bit Descriptions

Bit	Name	Function
0	SI	**SMBus0 Interrupt Flag.** This bit is set by hardware to indicate that the current SMBus0 state machine operation (such as writing a data or address byte) is complete. While SI is set, SCL0 is held low and SMBus0 is stalled. SI0 must be cleared by software. Clearing SI0 initiates the next SMBus0 state machine operation.

25.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.