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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f860-c-is

2.3. Clocking

The C8051F85x/86x devices have two internal oscillators and the option to use an external CMOS input at a pin as the system clock. A programmable divider allows the user to internally run the system clock at a slower rate than the selected oscillator if desired.

2.4. Counters/Timers and PWM

2.4.1. Programmable Counter Array (PCA0)

The C8051F85x/86x devices include a three-channel, 16-bit Programmable Counter Array with the following features:

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Three independently-configurable channels.
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation).
- Output polarity control.
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Can accept hardware “kill” signal from comparator 0.

2.4.2. Timers (Timer 0, Timer 1, Timer 2 and Timer 3)

Timers include the following features:

- Timer 0 and Timer 1 are standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Timer 2 and Timer 3 can each operate as 16-bit auto-reload or two independent 8-bit auto-reload timers, and include pin or LFO clock capture capabilities.

2.4.3. Watchdog Timer (WDT0)

The watchdog timer includes a 16-bit timer with a programmable reset period. The registers are protected from inadvertent access by an independent lock and key interface.

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Runs from the low frequency oscillator.
- Lock-out feature to prevent any modification until a system reset.

3. Pin Definitions

3.1. C8051F850/1/2/3/4/5 QSOP24 Pin Definitions

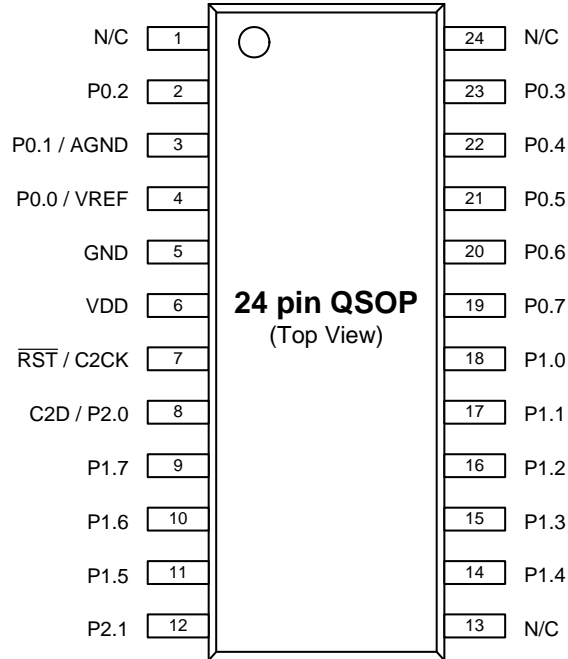


Figure 3.1. C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU Pinout

Table 3.1. Pin Definitions for C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	5			
VDD	Power	6			
$\overline{\text{RST}}$ / C2CK	Active-low Reset / C2 Debug Clock	7			

Register 12.3. EIE1: Extended Interrupt Enable 1

Bit	7	6	5	4	3	2	1	0
Name	ET3	ECP1	ECP0	EPCA0	EADC0	EWADC0	EMAT	ESMB0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

SFR Address: 0xE6

Table 12.4. EIE1 Register Bit Descriptions

Bit	Name	Function
7	ET3	Enable Timer 3 Interrupt. This bit sets the masking of the Timer 3 interrupt. 0: Disable Timer 3 interrupts. 1: Enable interrupt requests generated by the TF3L or TF3H flags.
6	ECP1	Enable Comparator1 (CP1) Interrupt. This bit sets the masking of the CP1 interrupt. 0: Disable CP1 interrupts. 1: Enable interrupt requests generated by the comparator 1 CPRIF or CPFIF flags.
5	ECP0	Enable Comparator0 (CP0) Interrupt. This bit sets the masking of the CP0 interrupt. 0: Disable CP0 interrupts. 1: Enable interrupt requests generated by the comparator 0 CPRIF or CPFIF flags.
4	EPCA0	Enable Programmable Counter Array (PCA0) Interrupt. This bit sets the masking of the PCA0 interrupts. 0: Disable all PCA0 interrupts. 1: Enable interrupt requests generated by PCA0.
3	EADC0	Enable ADC0 Conversion Complete Interrupt. This bit sets the masking of the ADC0 Conversion Complete interrupt. 0: Disable ADC0 Conversion Complete interrupt. 1: Enable interrupt requests generated by the ADINT flag.
2	EWADC0	Enable Window Comparison ADC0 Interrupt. This bit sets the masking of ADC0 Window Comparison interrupt. 0: Disable ADC0 Window Comparison interrupt. 1: Enable interrupt requests generated by ADC0 Window Compare flag (ADWINT).
1	EMAT	Enable Port Match Interrupts. This bit sets the masking of the Port Match Event interrupt. 0: Disable all Port Match interrupts. 1: Enable interrupt requests generated by a Port Match.

Table 12.5. EIP1 Register Bit Descriptions

Bit	Name	Function
0	PSMB0	SMBus (SMB0) Interrupt Priority Control. This bit sets the priority of the SMB0 interrupt. 0: SMB0 interrupt set to low priority level. 1: SMB0 interrupt set to high priority level.

14.10. ADC Control Registers

Register 14.1. ADC0CN0: ADC0 Control 0

Bit	7	6	5	4	3	2	1	0
Name	ADEN	ADBMEN	ADINT	ADBUSY	ADWINT	ADCM		
Type	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0

SFR Address: 0xE8 (bit-addressable)

Table 14.4. ADC0CN0 Register Bit Descriptions

Bit	Name	Function
7	ADEN	Enable. 0: ADC0 Disabled (low-power shutdown). 1: ADC0 Enabled (active and ready for data conversions).
6	ADBMEN	Burst Mode Enable. 0: ADC0 Burst Mode Disabled. 1: ADC0 Burst Mode Enabled.
5	ADINT	Conversion Complete Interrupt Flag. Set by hardware upon completion of a data conversion (ADBMEN=0), or a burst of conversions (ADBMEN=1). Can trigger an interrupt. Must be cleared by software.
4	ADBUSY	ADC Busy. Writing 1 to this bit initiates an ADC conversion when ADC0CM = 000. This bit should not be polled to indicate when a conversion is complete. Instead, the ADINT bit should be used when polling for conversion completion.
3	ADWINT	Window Compare Interrupt Flag. Set by hardware when the contents of ADC0H:ADC0L fall within the window specified by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL. Can trigger an interrupt. Must be cleared by software.
2:0	ADCM	Start of Conversion Mode Select. Specifies the ADC0 start of conversion source. All remaining bit combinations are reserved. 000: ADC0 conversion initiated on write of 1 to ADBUSY. 001: ADC0 conversion initiated on overflow of Timer 0. 010: ADC0 conversion initiated on overflow of Timer 2. 011: ADC0 conversion initiated on overflow of Timer 3. 100: ADC0 conversion initiated on rising edge of CNVSTR. 101-111: Reserved.

Register 14.14. REF0CN: Voltage Reference Control

Bit	7	6	5	4	3	2	1	0
Name	IREFLVL	Reserved	GNDSL	REFSL		TEMPE	Reserved	
Type	RW	R	RW	RW		RW	R	
Reset	0	0	0	1	1	0	0	0

SFR Address: 0xD1**Table 14.17. REF0CN Register Bit Descriptions**

Bit	Name	Function
7	IREFLVL	Internal Voltage Reference Level. Sets the voltage level for the internal reference source. 0: The internal reference operates at 1.65 V nominal. 1: The internal reference operates at 2.4 V nominal.
6	Reserved	Must write reset value.
5	GNDSL	Analog Ground Reference. Selects the ADC0 ground reference. 0: The ADC0 ground reference is the GND pin. 1: The ADC0 ground reference is the AGND pin.
4:3	REFSL	Voltage Reference Select. Selects the ADC0 voltage reference. 00: The ADC0 voltage reference is the VREF pin. 01: The ADC0 voltage reference is the VDD pin. 10: The ADC0 voltage reference is the internal 1.8 V digital supply voltage. 11: The ADC0 voltage reference is the internal voltage reference.
2	TEMPE	Temperature Sensor Enable. Enables/Disables the internal temperature sensor. 0: Temperature Sensor Disabled. 1: Temperature Sensor Enabled.
1:0	Reserved	Must write reset value.

16. Clock Sources and Selection (HFOSC0, LFOSC0, and EXTCLK)

The C8051F85x/86x devices can be clocked from the internal low power 24.5 MHz oscillator, the internal low-frequency 80 kHz oscillator, or an external CMOS clock signal at the EXTCLK pin. An adjustable clock divider allows the selected clock source to be post-scaled by powers of 2, up to a factor of 128. By default, the system clock comes up as the 24.5 MHz oscillator divided by 8.

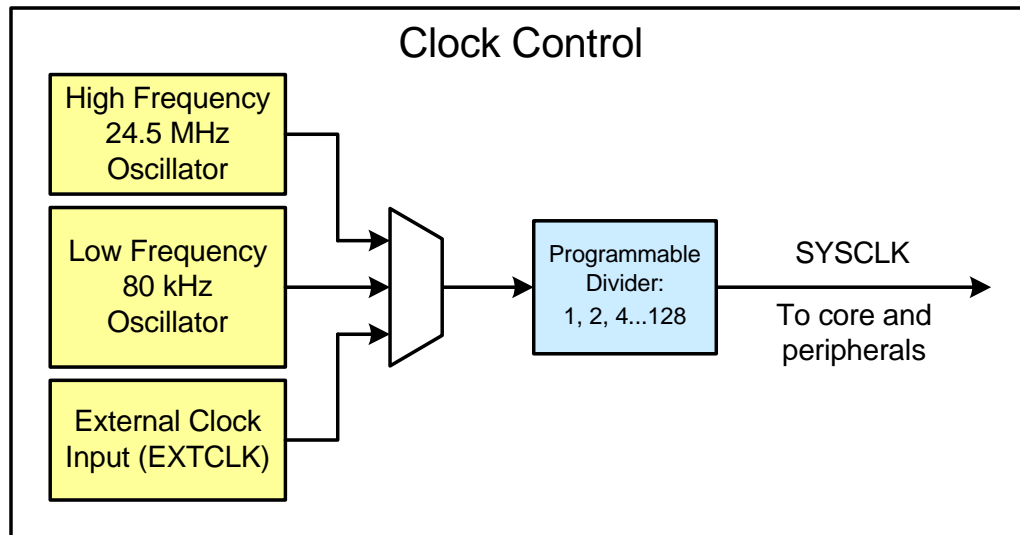


Figure 16.1. Clocking Options

16.1. Programmable High-Frequency Oscillator

All C8051F85x/86x devices include a programmable internal high-frequency oscillator that defaults as the system clock after a system reset. The oscillator is automatically enabled when it is requested. The internal oscillator period can be adjusted via the OSCICL register. On C8051F85x/86x devices, OSCICL is factory calibrated to obtain a 24.5 MHz base frequency.

16.2. Programmable Low-Frequency Oscillator

A programmable low-frequency internal oscillator is also included. The low-frequency oscillator is calibrated to a nominal frequency of 80 kHz. A divider at the oscillator output is capable of dividing the output clock of the module by 1, 2, 4, or 8, using the OSCLD bits in the OSCLCN register. Additionally, the OSCLF bits can be used to coarsely adjust the oscillator's output frequency.

16.2.1. Calibrating the Internal L-F Oscillator

Timer 3 includes a capture function that can be used to capture the oscillator frequency, when running from a known time base. When Timer 3 is configured for L-F Oscillator Capture Mode, a rising edge of the low-frequency oscillator's output will cause a capture event on the corresponding timer. As a capture event occurs, the current timer value (TMR3H:TMR3L) is copied into the timer reload registers (TMR3RLH:TMR3RLL). By recording the difference between two successive timer capture values, the low-frequency oscillator's period can be calculated. The OSCLF bits can then be adjusted to produce the desired oscillator frequency.

16.5. High Frequency Oscillator Control Registers

Register 16.1. OSCICL: High Frequency Oscillator Calibration

Bit	7	6	5	4	3	2	1	0
Name	OSCICL							
Type	RW							
Reset	X	X	X	X	X	X	X	X
SFR Address: 0xC7								

Table 16.1. OSCICL Register Bit Descriptions

Bit	Name	Function
7:0	OSCICL	Oscillator Calibration Bits. These bits determine the internal oscillator period. When set to 00000000b, the oscillator operates at its fastest setting. When set to 11111111b, the oscillator operates at its slowest setting. The reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

18.6. CRC Control Registers

Register 18.1. CRC0CN: CRC0 Control

Bit	7	6	5	4	3	2	1	0
Name	Reserved				CRCINIT	CRCVAL	Reserved	CRCPNT
Type	R				RW	RW	R	RW
Reset	0	0	0	1	0	0	0	0

SFR Address: 0xCE

Table 18.2. CRC0CN Register Bit Descriptions

Bit	Name	Function
7:4	Reserved	Must write reset value.
3	CRCINIT	CRC Result Initialization Bit. Writing a 1 to this bit initializes the entire CRC result based on CRCVAL.
2	CRCVAL	CRC Set Value Initialization Bit. This bit selects the set value of the CRC result. 0: CRC result is set to 0x0000 on write of 1 to CRCINIT. 1: CRC result is set to 0xFFFF on write of 1 to CRCINIT.
1	Reserved	Must write reset value.
0	CRCPNT	CRC Result Pointer. Specifies the byte of the CRC result to be read/written on the next access to CRC0DAT. This bit will automatically toggle upon each read or write. 0: CRC0DAT accesses bits 7-0 of the 16-bit CRC result. 1: CRC0DAT accesses bits 15-8 of the 16-bit CRC result.

Note: Upon initiation of an automatic CRC calculation, the three cycles following a write to CRC0CN that initiate a CRC operation must only contain instructions which execute in the same number of cycles as the number of bytes in the instruction. An example of such an instruction is a 3-byte MOV that targets the CRC0FLIP register. When programming in C, the dummy value written to CRC0FLIP should be a non-zero value to prevent the compiler from generating a 2-byte MOV instruction.

Register 18.2. CRC0IN: CRC0 Data Input

Bit	7	6	5	4	3	2	1	0
Name	CRC0IN							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xDD								

Table 18.3. CRC0IN Register Bit Descriptions

Bit	Name	Function
7:0	CRC0IN	CRC Data Input. Each write to CRCIN results in the written data being computed into the existing CRC result according to the CRC algorithm.

20.3.3. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

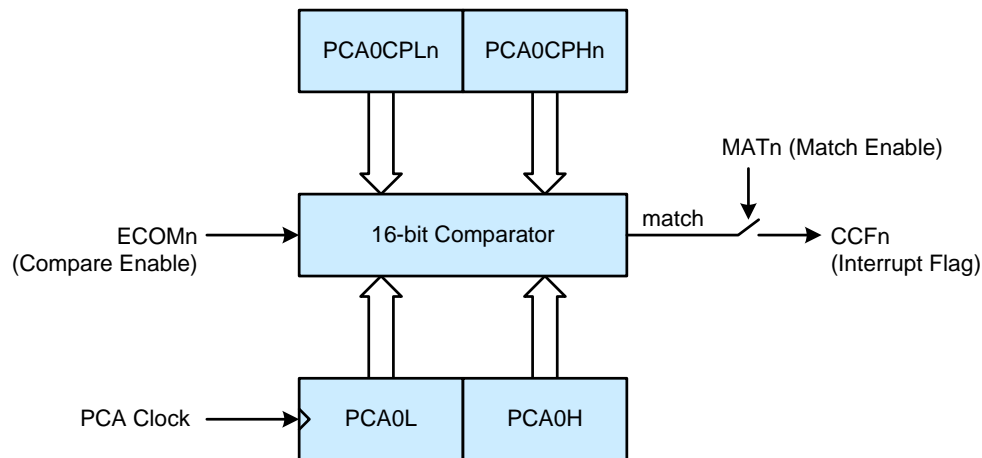


Figure 20.3. PCA Software Timer Mode Diagram

20.4. PWM Waveform Generation

The PCA can generate edge- or center-aligned PWM waveforms with resolutions of 8, 9, 10, 11 or 16 bits. PWM resolution depends on the module setup, as specified within the individual module PCA0CPMn registers as well as the PCA0PWM register. Modules can be configured for 8-11 bit mode, or for 16-bit mode individually using the PCA0CPMn registers. All modules configured for 8-11 bit mode will have the same resolution, specified by the PCA0PWM register. When operating in one of the PWM modes, each module may be individually configured for center or edge-aligned PWM waveforms. Each channel has a single bit in the PCA0CENT register to select between the two options.

20.4.1. Edge Aligned PWM

When configured for edge-aligned mode, a module will generate an edge transition at two points for every 2^N PCA clock cycles, where N is the selected PWM resolution in bits. In edge-aligned mode, these two edges are referred to as the “match” and “overflow” edges. The polarity at the output pin is selectable, and can be inverted by setting the appropriate channel bit to ‘1’ in the PCA0POL register. Prior to inversion, a match edge sets the channel to logic high, and an overflow edge clears the channel to logic low.

The match edge occurs when the the lowest N bits of the module’s PCA0CPn register match the corresponding bits of the main PCA0 counter register. For example, with 10-bit PWM, the match edge will occur any time bits 9-0 of the PCA0CPn register match bits 9-0 of the PCA0 counter value.

The overflow edge occurs when an overflow of the PCA0 counter happens at the desired resolution. For example, with 10-bit PWM, the overflow edge will occur when bits 0-9 of the PCA0 counter transition from all 1’s to all 0’s. All modules configured for edge-aligned mode at the same resolution will align on the overflow edge of the waveforms.

An example of the PWM timing in edge-aligned mode for two channels is shown in Figure 20.6. In this example, the CEX0POL and CEX1POL bits are cleared to 0.

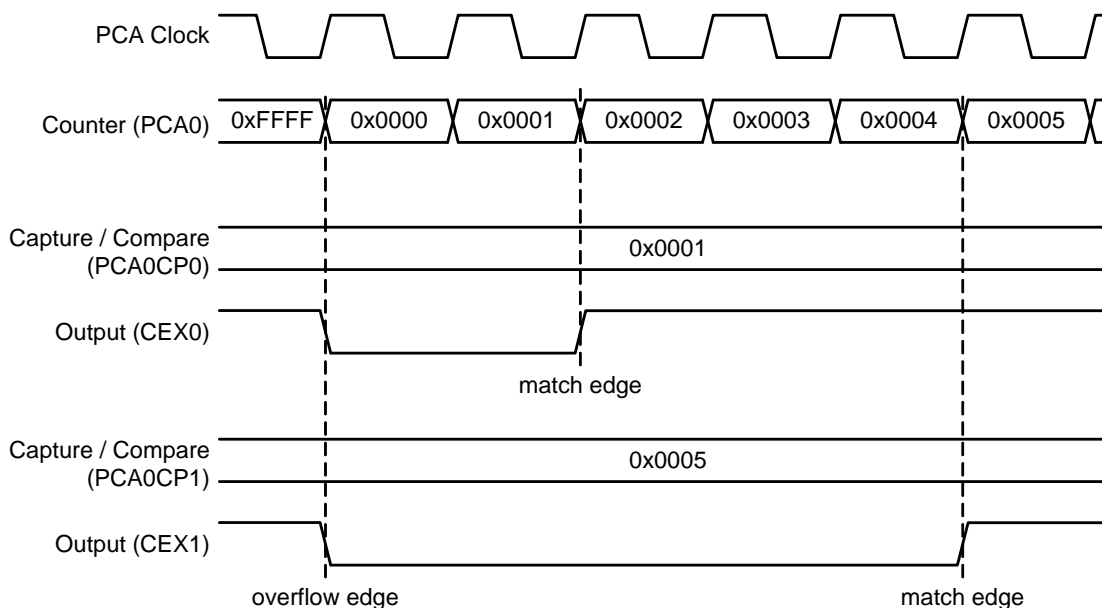


Figure 20.6. Edge-Aligned PWM Timing

For a given PCA resolution, the unused high bits in the PCA0 counter and the PCA0CPn compare registers are ignored, and only the used bits of the PCA0CPn register determine the duty cycle. Equation 20.2 describes the duty cycle when CEXnPOL in the PCA0POL register is cleared to 0. Equation 20.3 describes the duty cycle when CEXnPOL in the PCA0POL register is set to 1. A 0% duty cycle for the channel (with CEXnPOL = 0) is achieved by clearing the module’s ECOM bit to 0. This will

Register 20.2. PCA0MD: PCA Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	Reserved			CPS			ECF
Type	RW	R			RW			RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xD9								

Table 20.4. PCA0MD Register Bit Descriptions

Bit	Name	Function
7	CIDL	PCA Counter/Timer Idle Control. Specifies PCA behavior when CPU is in Idle Mode. 0: PCA continues to function normally while the system controller is in Idle Mode. 1: PCA operation is suspended while the system controller is in Idle Mode.
6:4	Reserved	Must write reset value.
3:1	CPS	PCA Counter/Timer Pulse Select. These bits select the timebase source for the PCA counter. 000: System clock divided by 12. 001: System clock divided by 4. 010: Timer 0 overflow. 011: High-to-low transitions on ECI (max rate = system clock divided by 4). 100: System clock. 101: External clock divided by 8 (synchronized with the system clock). 110: Low frequency oscillator divided by 8. 111: Reserved.
0	ECF	PCA Counter/Timer Overflow Interrupt Enable. This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.

21. Port I/O (Port 0, Port 1, Port 2, Crossbar, and Port Match)

Digital and analog resources on the C8051F85x/86x family are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P1.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar, or assigned to an analog function. Port pins P2.0 and P2.1 can be used as GPIO. Port pin P2.0 is shared with the C2 Interface Data signal (C2D). The designer has complete control over which functions are assigned, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a priority crossbar decoder. Note that the state of a port I/O pin can always be read in the corresponding port latch, regardless of the crossbar settings.

The crossbar assigns the selected internal digital resources to the I/O pins based on the Priority Decoder (Figure 21.2 and Figure 21.3). The registers XBR0, XBR1 and XBR2 are used to select internal digital functions.

The port I/O cells are configured as either push-pull or open-drain in the Port Output Mode registers (PnMDOUT, where n = 0,1). Additionally, each bank of port pins (P0, P1, and P2) has two selectable drive strength settings.

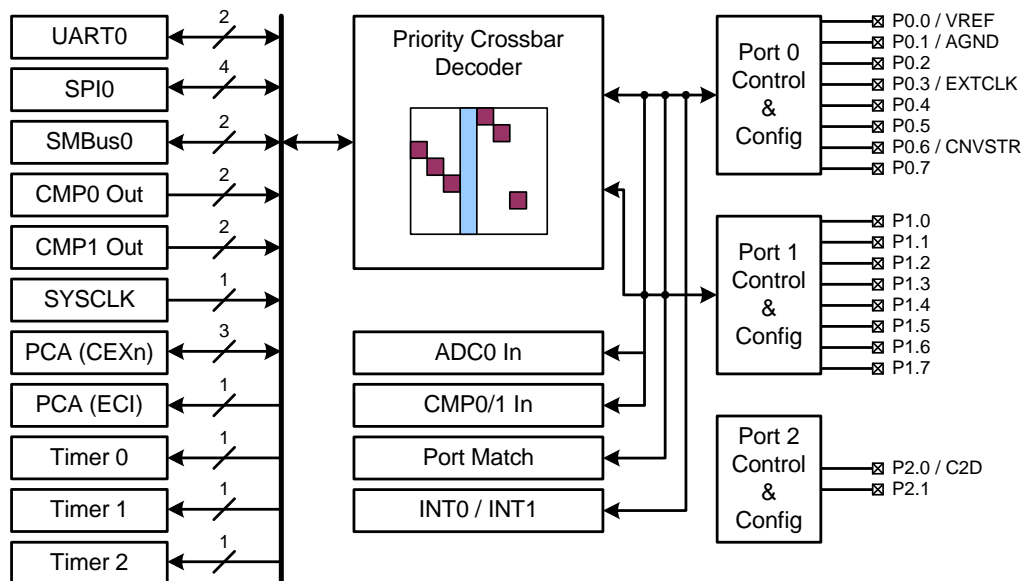


Figure 21.1. Port I/O Functional Block Diagram

24.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses an arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames. The position of the ACK interrupt when operating as a receiver depends on whether hardware ACK generation is enabled. As a receiver, the interrupt for an ACK occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled. As a transmitter, interrupts occur **after** the ACK, regardless of whether hardware ACK generation is enabled or not.

24.5.1. Write Sequence (Master)

During a write sequence, an SMBus master writes data to a slave device. The master in this transfer will be a transmitter during the address byte, and a transmitter during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. The interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 24.5 shows a typical master write sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that all of the “data byte transferred” interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.

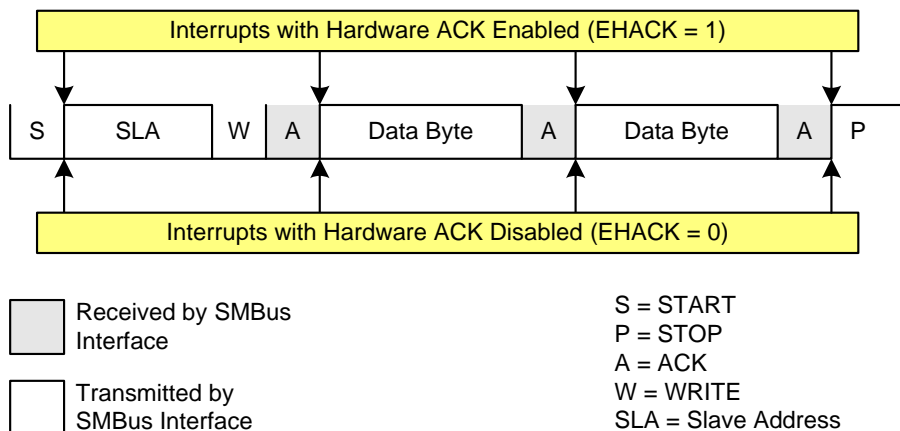


Figure 24.5. Typical Master Write Sequence

Register 24.5. SMB0ADM: SMBus0 Slave Address Mask

Bit	7	6	5	4	3	2	1	0
Name	SLVM							EHACK
Type	RW							RW
Reset	1	1	1	1	1	1	1	0

SFR Address: 0xD6

Table 24.11. SMB0ADM Register Bit Descriptions

Bit	Name	Function
7:1	SLVM	SMBus0 Slave Address Mask. Defines which bits of register SMB0ADR are compared with an incoming address byte, and which bits are ignored. Any bit set to 1 in SLVM enables comparisons with the corresponding bit in SLV. Bits set to 0 are ignored (can be either 0 or 1 in the incoming address).
0	EHACK	Hardware Acknowledge Enable. Enables hardware acknowledgement of slave address and received data bytes. 0: Firmware must manually acknowledge all incoming address and data bytes. 1: Automatic slave address recognition and hardware acknowledge is enabled.

25.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

Register 25.2. TCON: Timer 0/1 Control

Bit	7	6	5	4	3	2	1	0
Name	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

SFR Address: 0x88 (bit-addressable)

Table 25.4. TCON Register Bit Descriptions

Bit	Name	Function
7	TF1	Timer 1 Overflow Flag. Set to 1 by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
6	TR1	Timer 1 Run Control. Timer 1 is enabled by setting this bit to 1.
5	TF0	Timer 0 Overflow Flag. Set to 1 by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
4	TR0	Timer 0 Run Control. Timer 0 is enabled by setting this bit to 1.
3	IE1	External Interrupt 1. This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine in edge-triggered mode.
2	IT1	Interrupt 1 Type Select. This bit selects whether the configured INT1 interrupt will be edge or level sensitive. INT1 is configured active low or high by the IN1PL bit in register IT01CF. 0: INT1 is level triggered. 1: INT1 is edge triggered.
1	IE0	External Interrupt 0. This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine in edge-triggered mode.
0	IT0	Interrupt 0 Type Select. This bit selects whether the configured INT0 interrupt will be edge or level sensitive. INT0 is configured active low or high by the IN0PL bit in register IT01CF. 0: INT0 is level triggered. 1: INT0 is edge triggered.

Register 25.8. TMR2CN: Timer 2 Control

Bit	7	6	5	4	3	2	1	0
Name	TF2H	TF2L	TF2LEN	TF2CEN	T2SPLIT	TR2	Reserved	T2XCLK
Type	RW	RW	RW	RW	RW	RW	R	RW
Reset	0	0	0	0	0	0	0	0

SFR Address: 0xC8 (bit-addressable)

Table 25.10. TMR2CN Register Bit Descriptions

Bit	Name	Function
7	TF2H	Timer 2 High Byte Overflow Flag. Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF2L	Timer 2 Low Byte Overflow Flag. Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. TF2L will be set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.
5	TF2LEN	Timer 2 Low Byte Interrupt Enable. When set to 1, this bit enables Timer 2 Low Byte interrupts. If Timer 2 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 2 overflows.
4	TF2CEN	Timer 2 Capture Enable. When set to 1, this bit enables Timer 2 Capture Mode. If TF2CEN is set and Timer 2 interrupts are enabled, an interrupt will be generated on a falling edge of the selected T2 input pin, and the current 16-bit timer value in TMR2H:TMR2L will be copied to TMR2RLH:TMR2RLL.
3	T2SPLIT	Timer 2 Split Mode Enable. When this bit is set, Timer 2 operates as two 8-bit timers with auto-reload. 0: Timer 2 operates in 16-bit auto-reload mode. 1: Timer 2 operates as two 8-bit auto-reload timers.
2	TR2	Timer 2 Run Control. Timer 2 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in split mode.
1	Reserved	Must write reset value.

29.2. C2 Interface Registers

The following describes the C2 registers necessary to perform flash programming through the C2 interface. All C2 registers are accessed through the C2 interface, and are not available in the SFR map for firmware access.

Register 29.1. C2ADD: C2 Address

Bit	7	6	5	4	3	2	1	0
Name	C2ADD							
Type	RW							
Reset	0	0	0	0	0	0	0	0

This register is part of the C2 protocol.

Table 29.1. C2ADD Register Bit Descriptions

Bit	Name	Function
7:0	C2ADD	C2 Address. The C2ADD register is accessed via the C2 interface. The value written to C2ADD selects the target data register for C2 Data Read and Data Write commands. 0x00: C2DEVID 0x01: C2REVID 0x02: C2FPCTL 0xB4: C2FPDAT