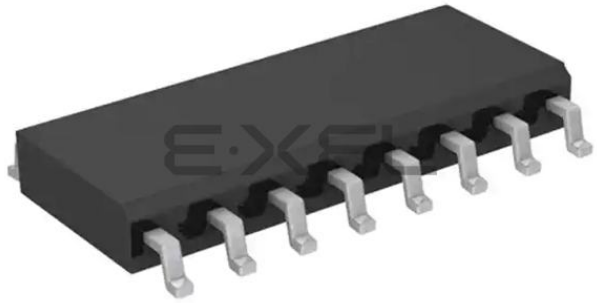

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f861-c-gsr

3.3. C8051F860/1/2/3/4/5 SOIC16 Pin Definitions

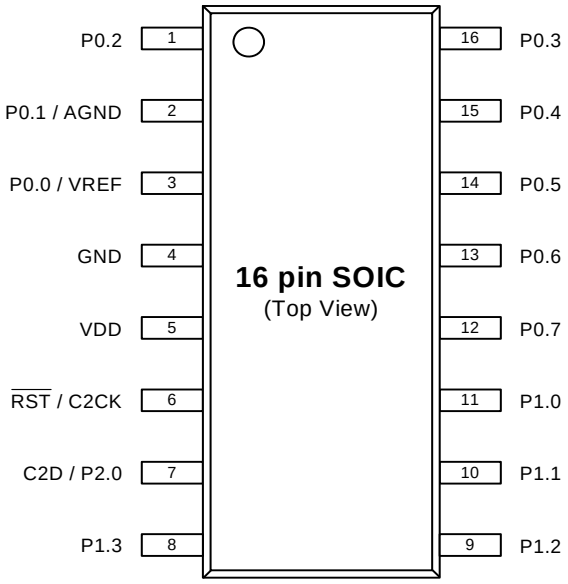

Figure 3.3. C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS Pinout

Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	4			
VDD	Power	5			
RST / C2CK	Active-low Reset / C2 Debug Clock	6			
P0.0	Standard I/O	3	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0

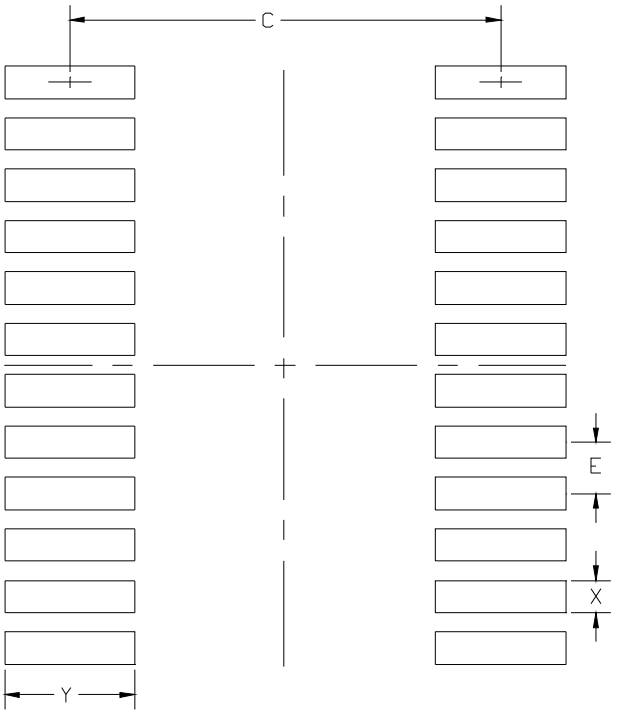

Figure 5.2. QSOP-24 PCB Land Pattern

Table 5.2. QSOP-24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.5. Flash Control Registers

Register 10.1. PSCTL: Program Store Control

Bit	7	6	5	4	3	2	1	0
Name	Reserved						PSEE	PSWE
Type	R						RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x8F								

Table 10.2. PSCTL Register Bit Descriptions

Bit	Name	Function
7:2	Reserved	Must write reset value.
1	PSEE	**Program Store Erase Enable.** Setting this bit (in combination with PSWE) allows an entire page of flash program memory to be erased. If this bit is logic 1 and flash writes are enabled (PSWE is logic 1), a write to flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter. 0: Flash program memory erasure disabled. 1: Flash program memory erasure enabled.
0	PSWE	**Program Store Write Enable.** Setting this bit allows writing a byte of data to the flash program memory using the MOVX write instruction. The flash location should be erased before writing data. 0: Writes to flash program memory disabled. 1: Writes to flash program memory enabled; the MOVX write instruction targets flash memory.

11.1. Device Identification Registers

Register 11.1. DEVICEID: Device Identification

Bit	7	6	5	4	3	2	1	0
Name	DEVICEID							
Type	R							
Reset	0	0	1	1	0	0	0	0
SFR Address: 0xB5								

Table 11.2. DEVICEID Register Bit Descriptions

Bit	Name	Function
7:0	DEVICEID	**Device ID.** This read-only register returns the 8-bit device ID: 0x30 (C8051F85x/86x).

Table 12.4. EIE1 Register Bit Descriptions

Bit	Name	Function
0	ESMB0	**Enable SMBus (SMB0) Interrupt.** This bit sets the masking of the SMB0 interrupt. 0: Disable all SMB0 interrupts. 1: Enable interrupt requests generated by SMB0.

Register 14.10. ADC0GTL: ADC0 Greater-Than Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTL							
Type	RW							
Reset	1	1	1	1	1	1	1	1
SFR Address: 0xC3								

Table 14.13. ADC0GTL Register Bit Descriptions

Bit	Name	Function
7:0	ADC0GTL	**Greater-Than Low Byte.** Least Significant Byte of the 16-bit Greater-Than window compare register.
Note: In 8-bit mode, this register should be set to 0x00.		

16. Clock Sources and Selection (HFOSC0, LFOSC0, and EXTCLK)

The C8051F85x/86x devices can be clocked from the internal low power 24.5 MHz oscillator, the internal low-frequency 80 kHz oscillator, or an external CMOS clock signal at the EXTCLK pin. An adjustable clock divider allows the selected clock source to be post-scaled by powers of 2, up to a factor of 128. By default, the system clock comes up as the 24.5 MHz oscillator divided by 8.

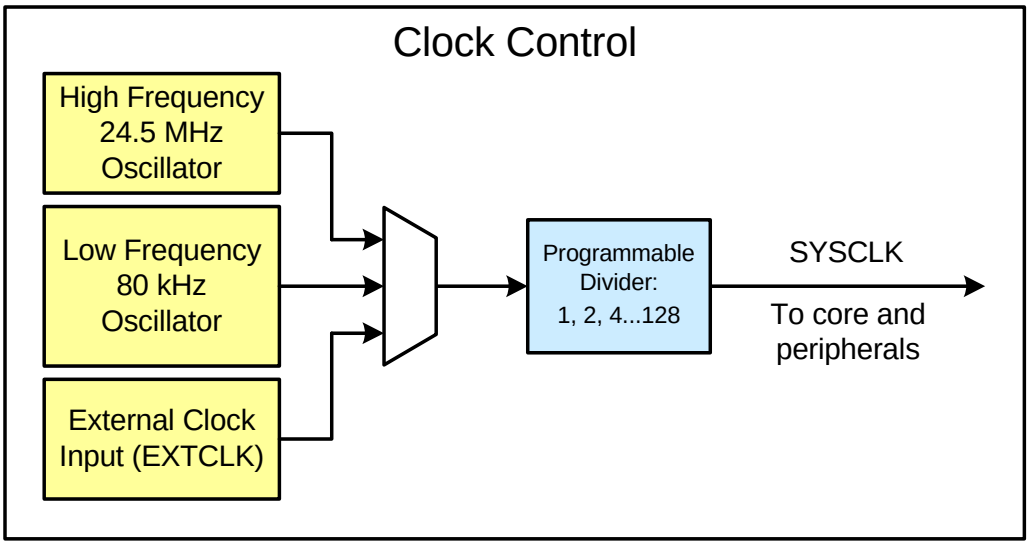

Figure 16.1. Clocking Options

16.1. Programmable High-Frequency Oscillator

All C8051F85x/86x devices include a programmable internal high-frequency oscillator that defaults as the system clock after a system reset. The oscillator is automatically enabled when it is requested. The internal oscillator period can be adjusted via the OSCICL register. On C8051F85x/86x devices, OSCICL is factory calibrated to obtain a 24.5 MHz base frequency.

16.2. Programmable Low-Frequency Oscillator

A programmable low-frequency internal oscillator is also included. The low-frequency oscillator is calibrated to a nominal frequency of 80 kHz. A divider at the oscillator output is capable of dividing the output clock of the module by 1, 2, 4, or 8, using the OSCLD bits in the OSCLCN register. Additionally, the OSCLF bits can be used to coarsely adjust the oscillator's output frequency.

16.2.1. Calibrating the Internal L-F Oscillator

Timer 3 includes a capture function that can be used to capture the oscillator frequency, when running from a known time base. When Timer 3 is configured for L-F Oscillator Capture Mode, a rising edge of the low-frequency oscillator's output will cause a capture event on the corresponding timer. As a capture event occurs, the current timer value (TMR3H:TMR3L) is copied into the timer reload registers (TMR3RLH:TMR3RLL). By recording the difference between two successive timer capture values, the low-frequency oscillator's period can be calculated. The OSCLF bits can then be adjusted to produce the desired oscillator frequency.

Register 18.6. CRC0FLIP: CRC0 Bit Flip

Bit	7	6	5	4	3	2	1	0
Name	CRC0FLIP							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xCF								

Table 18.7. CRC0FLIP Register Bit Descriptions

Bit	Name	Function
7:0	CRC0FLIP	**CRC0 Bit Flip.** Any byte written to CRC0FLIP is read back in a bit-reversed order, i.e., the written LSB becomes the MSB. For example: If 0xC0 is written to CRC0FLIP, the data read back will be 0x03. If 0x05 is written to CRC0FLIP, the data read back will be 0xA0.

Table 19.1. IT01CF Register Bit Descriptions

Bit	Name	Function
2:0	IN0SL	**INT0 Port Pin Selection Bits.** These bits select which Port pin is assigned to INT0. This pin assignment is independent of the Crossbar; INT0 will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7

20.1. PCA Counter/Timer

The 16-bit PCA counter/timer consists of two 8-bit SFRs: PCA0L and PCA0H. PCA0H is the high byte of the 16-bit counter/timer and PCA0L is the low byte. Reading PCA0L automatically latches the value of PCA0H into a “snapshot” register; the following PCA0H read accesses this “snapshot” register. **Reading the PCA0L Register first guarantees an accurate reading of the entire 16-bit PCA0 counter.** Reading PCA0H or PCA0L does not disturb the counter operation. The CPS2–CPS0 bits in the PCA0MD register select the timebase for the counter/timer as shown in Table 20.1.

When the counter/timer overflows from 0xFFFF to 0x0000, the Counter Overflow Flag (CF) in PCA0MD is set to logic 1 and an interrupt request is generated if CF interrupts are enabled. Setting the ECF bit in PCA0MD to logic 1 enables the CF flag to generate an interrupt request. The CF bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Clearing the CIDL bit in the PCA0MD register allows the PCA to continue normal operation while the CPU is in Idle mode.

Table 20.1. PCA Timebase Input Options

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)*
1	0	0	System clock
1	0	1	External oscillator source divided by 8*
1	1	0	Low frequency oscillator divided by 8*
1	1	1	Reserved

***Note:** Synchronized with the system clock.

20.2. PCA0 Interrupt Sources

The PCA0 module shares one interrupt vector among all of its modules. There are are several event flags that can be used to generate a PCA0 interrupt. They are: the main PCA counter overflow flag (CF), which is set upon a 16-bit overflow of the PCA0 counter, an intermediate overflow flag (COVF), which can be set on an overflow from the 8th - 11th bit of the PCA0 counter, and the individual flags for each PCA channel (CCFn), which are set according to the operation mode of that module. These event flags are always set when the trigger condition occurs. Each of these flags can be individually selected to generate a PCA0 interrupt, using the corresponding interrupt enable flag (ECF for CF, ECOV for COVF, and ECCFn for each CCFn). PCA0 interrupts must be globally enabled before any individual interrupt sources are recognized by the processor. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1.

Register 20.9. PCA0CPH0: PCA Capture Module High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPH0							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xFC								

Table 20.11. PCA0CPH0 Register Bit Descriptions

Bit	Name	Function
7:0	PCA0CPH0	**PCA Capture Module High Byte.** The PCA0CPH0 register holds the high byte (MSB) of the 16-bit capture module.This register address also allows access to the high byte of the corresponding PCA channels auto-reload value for 9 to 11-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.
Note: A write to this register will set the module's ECOM bit to a 1.		

Registers XBR0, XBR1 and XBR2 are used to assign the digital I/O resources to the physical I/O port pins. Note that when the SMBus is selected, the crossbar assigns both pins associated with the SMBus (SDA and SCL); when UART0 is selected, the crossbar assigns both pins associated with UART0 (TX and RX). UART0 pin assignments are fixed for bootloading purposes: UART0 TX is always assigned to P0.4; UART0 RX is always assigned to P0.5. Standard port I/Os appear contiguously after the prioritized functions have been assigned.

Figure 21.3 shows an example of the resulting pin assignments of the device with UART0 and SPI0 enabled and the EXTCLK (P0.3) pin skipped (P0SKIP = 0x08). UART0 is the highest priority and it will be assigned first. The UART0 pins can only appear on P0.4 and P0.5, so that is where it is assigned. The next-highest enabled peripheral is SPI0. P0.0, P0.1 and P0.2 are free, so SPI0 takes these three pins. The fourth pin, NSS, is routed to P0.6 because P0.3 is skipped and P0.4 and P0.5 are already occupied by the UART. The other pins on the device are available for use as general-purpose digital I/O or analog functions.

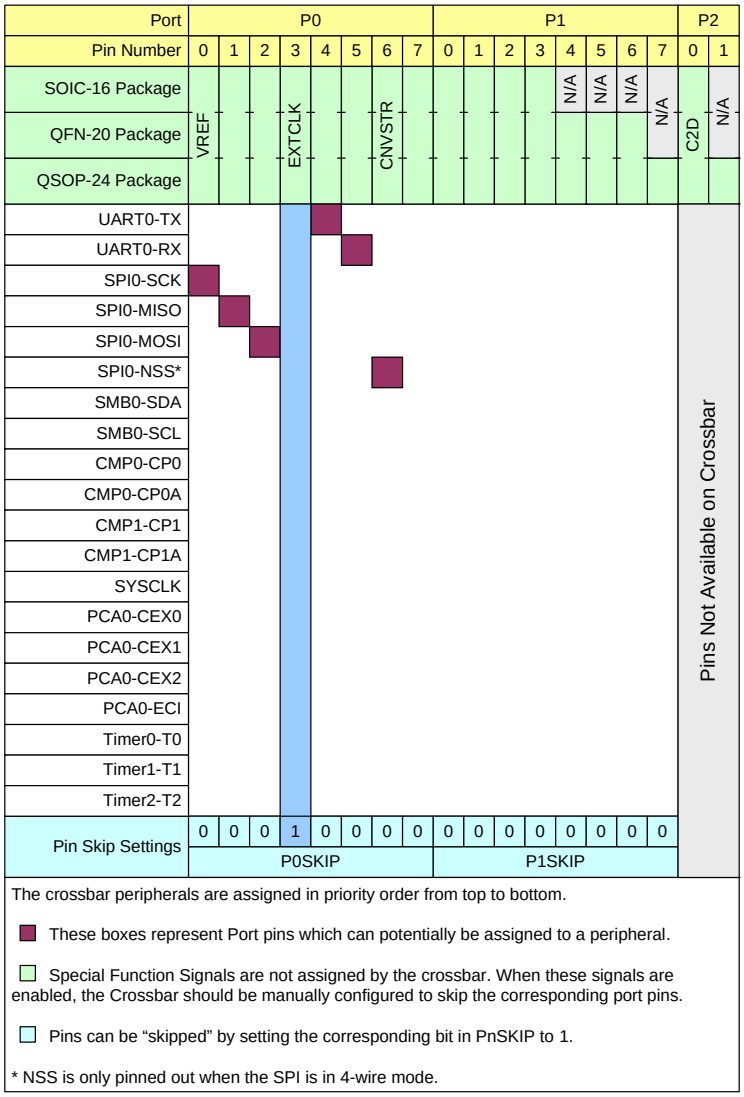

Figure 21.3. Crossbar Priority Decoder Example

Register 21.8. P0MDIN: Port 0 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDIN							
Type	RW							
Reset	1	1	1	1	1	1	1	1
SFR Address: 0xF1								

Table 21.11. P0MDIN Register Bit Descriptions

Bit	Name	Function
7:0	P0MDIN	**Port 0 Input Mode.** Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. 0: Corresponding P0.x pin is configured for analog mode. 1: Corresponding P0.x pin is configured for digital mode.

23. Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

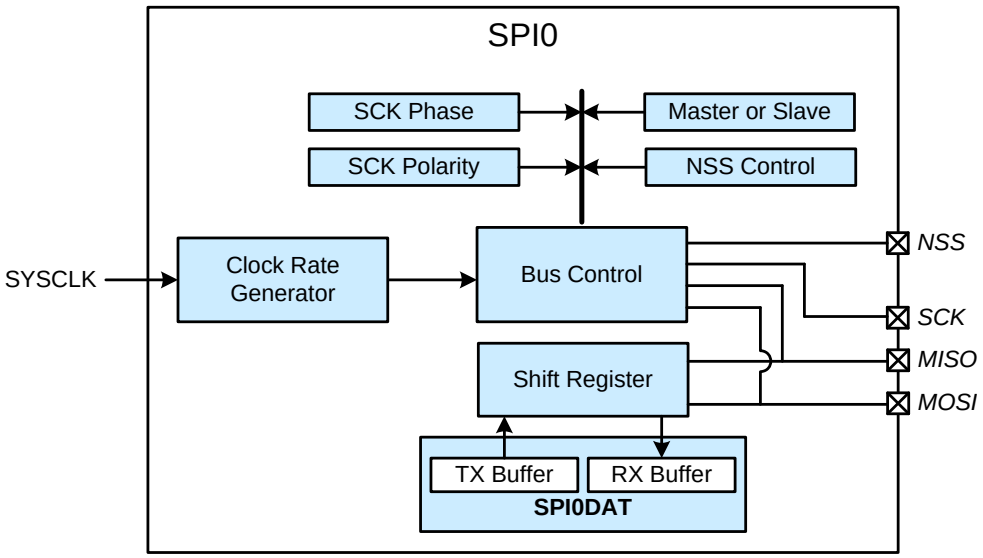

Figure 23.1. SPI0 Block Diagram

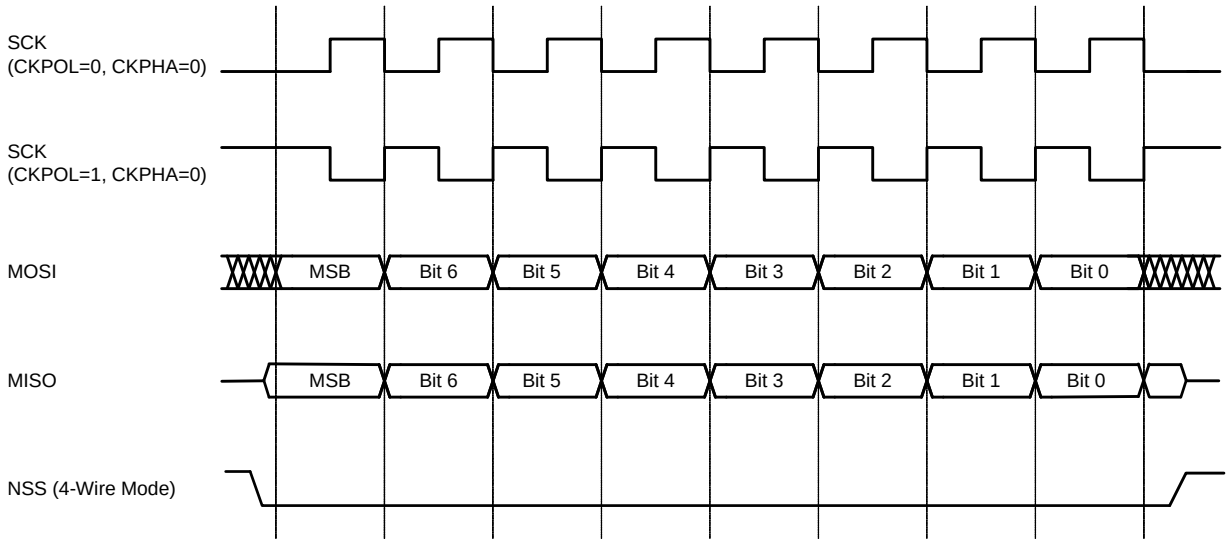

Figure 23.6. Slave Mode Data/Clock Timing (CKPHA = 0)

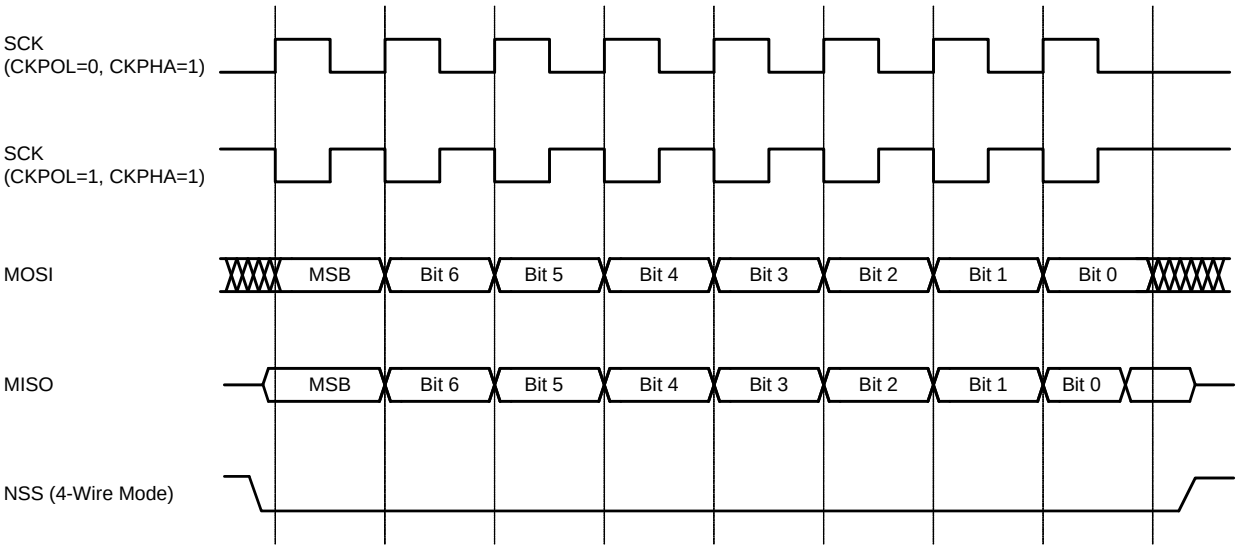

Figure 23.7. Slave Mode Data/Clock Timing (CKPHA = 1)

23.6. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following figures.

Register 25.14. TMR3RLL: Timer 3 Reload Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLL							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x92								

Table 25.16. TMR3RLL Register Bit Descriptions

Bit	Name	Function
7:0	TMR3RLL	**Timer 3 Reload Low Byte.** When operating in one of the auto-reload modes, TMR3RLL holds the reload value for the low byte of Timer 3 (TMR3L). When operating in capture mode, TMR3RLL is the captured value of TMR3L.

Register 25.16. TMR3L: Timer 3 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3L							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x94								

Table 25.18. TMR3L Register Bit Descriptions

Bit	Name	Function
7:0	TMR3L	**Timer 3 Low Byte.** In 16-bit mode, the TMR3L register contains the low byte of the 16-bit Timer 3. In 8-bit mode, TMR3L contains the 8-bit low byte timer value.

26.2.2. 9-Bit UART

9-bit UART mode uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB8, which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB8 and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TI Transmit Interrupt Flag is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN Receive Enable bit is set to 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: (1) RI must be logic 0, and (2) if MCE is logic 1, the 9th bit must be logic 1 (when MCE is logic 0, the state of the ninth data bit is unimportant). If these conditions are met, the eight bits of data are stored in SBUF0, the ninth bit is stored in RB8, and the RI flag is set to 1. If the above conditions are not met, SBUF0 and RB8 will not be loaded and the RI flag will not be set to 1. A UART0 interrupt will occur if enabled when either TI or RI is set to 1.

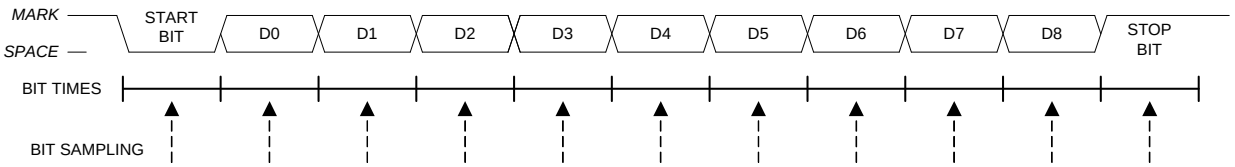

Figure 26.4. 9-Bit UART Timing Diagram

28. Revision-Specific Behavior

C8051F85x/86x Revision B devices have differences from Revision C devices:

- Temperature Sensor offset and slope
- Flash endurance
- Latch-up performance
- Unique Identifier

28.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figure 28.1, Figure 28.2, and Figure 28.3 show how to find the Lot ID Code on the top side of the device package.

Firmware can distinguish between a Revision B and Revision C device using the value of the REVID register described in “Device Identification and Unique Identifier” on page 68.

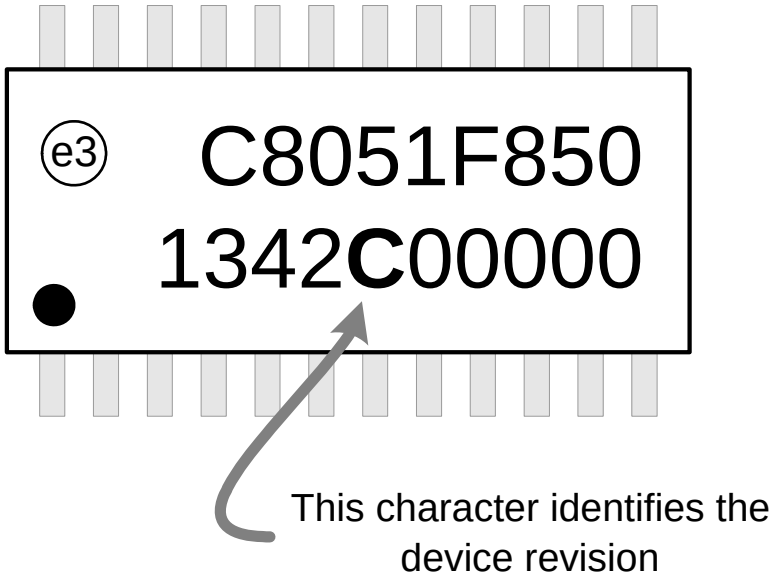

Figure 28.1. QSOP-24 Package Revision Marking

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 0.6

- Updated front page block diagram.
- Updated ADC supply current parameters in Table 1.2, “Power Consumption,” on page 8.
- Corrected flash programming voltage range in "Table 1.4. Flash Memory" on page 11.
- Added ADC Power-On Time specification in Table 1.7, “ADC,” on page 13.
- Added section "1.2. Typical Performance Curves" on page 19.
- Corrected DERIVID Information in Table 11.3, “DERIVID Register Bit Descriptions,” on page 70.
- Updated ADC chapter ("14. Analog-to-Digital Converter (ADC0)" on page 85) and expanded section "14.5. Power Considerations" on page 85 with recommended power configuration settings.
- Updated Figure 21.1, “Port I/O Functional Block Diagram,” on page 184.
- Corrected reset value in Register 24.5, “SMB0ADM: SMBus0 Slave Address Mask,” on page 257.
- Corrected description of IE0 in "Table 25.4. TCON Register Bit Descriptions" on page 259.

Revision 0.6 to Revision 0.7

- Added mention of the UID to the front page.
- Updated some TBD values in the "1. Electrical Specifications" on page 8 section.
- Updated Power-On Reset (POR) Threshold maximum Falling Voltage on V_{DD} specification in Table 1.3.
- Updated Reset Delay from non-POR source typical specification in Table 1.3.
- Removed V_{DD} Ramp Time maximum specification in Table 1.3.
- Updated Flash Memory Erase Time specification and added Note 2 to Table 1.4.
- Updated maximum ADC DC performance specifications in Table 1.7.
- Updated minimum and maximum ADC offset error and slope error specifications in Table 1.7.
- Updated conditions on Internal Fast Settling Reference Output Voltage (Full Temperature and Supply Range) in Table 1.8.
- Added a new section "1.2.3. Port I/O Output Drive" on page 21.
- Updated pinout Figure 3.1, Figure 3.2, Figure 3.3, Table 3.1, Table 3.2, and Table 3.3 titles to the correct part numbers.
- Updated the Ordering Information ("4. Ordering Information" on page 42.) for Revision C devices.
- Added mention of the unique identifier to "8. Memory Organization" on page 52.
- Added unique identifier information to "11. Device Identification and Unique Identifier" on page 68.
- Updated device part numbers listed in Table 11.3, “DERIVID Register Bit Descriptions,” on page 70 to include the revision.
- Added "28. Revision-Specific Behavior" on page 301.

Revision 0.7 to Revision 1.0

- Updated Digital Core, ADC, and Temperature Sensor electrical specifications information for -I devices.
- Updated -I part number information in "4. Ordering Information" on page 42.
- Replaced reference to AMX0P and AMX0N with ADC0MX in Table 21.1, “Port I/O Assignment for Analog Functions,” on page 186.
- Added a note to Table 1.13, “Absolute Maximum Ratings,” on page 22 and added a link to the Quality and Reliability Monitor Report.
- Added Operating Junction Temperature to Table 1.13, “Absolute Maximum Ratings,” on page 22.
- Updated all TBDs in "1. Electrical Specifications" on page 8.