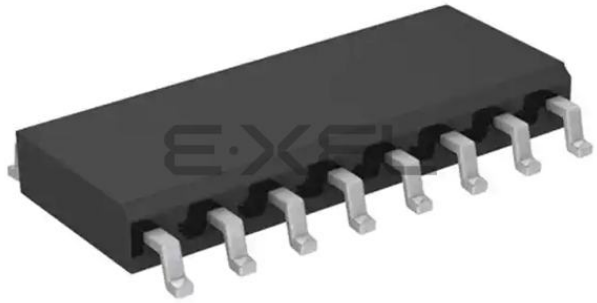

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f864-c-gsr

Table 1.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	490	—	µA
		100 ksps, V_{DD} = 3.0 V	—	245	—	µA
		10 ksps, V_{DD} = 3.0 V	—	23	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	530	—	µA
		50 ksps, V_{DD} = 3.0 V	—	265	—	µA
		10 ksps, V_{DD} = 3.0 V	—	53	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	950	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	420	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	85	—	µA
Internal ADC0 Reference, Always-on[5]	I_{IREF}	Normal Power Mode	—	680	790	µA
		Low Power Mode	—	160	210	µA
Temperature Sensor	I_{TSENSE}		—	75	120	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CPnMD = 11	—	0.5	—	µA
		CPnMD = 10	—	3	—	µA
		CPnMD = 01	—	10	—	µA
		CPnMD = 00	—	25	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	µA

Notes:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

Table 1.7. ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset Error	E_{OFF}	12 Bit Mode, VREF = 1.65 V	–3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	–2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	71	—	dB
		10 Bit Mode	—	70	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB

***Note:** Absolute input pin voltage is limited by the V_{DD} supply.

1.4. Absolute Maximum Ratings

Stresses above those listed under Table 1.13 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 1.13. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on V_{DD}	V_{DD}		GND–0.3	4.2	V
Voltage on I/O pins or $\overline{RST}$	V_{IN}	$V_{DD} \geq 3.3$ V	GND–0.3	5.8	V
		$V_{DD} < 3.3$ V	GND–0.3	V_{DD}+2.5	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by Any I/O Pin or $\overline{RST}$	I_{PIO}		-100	100	mA
Operating Junction Temperature	T_J	Commercial Grade Devices (-GM, -GS, -GU)	–40	105	°C
		Industrial Grade Devices (-IM, -IS, -IU)	–40	125	°C
Note: Exposure to maximum rating conditions for extended periods may affect device reliability.					

2.7. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VDD Supply Monitor and power-on resets, the $\overline{\text{RST}}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal low-power oscillator. The Watchdog Timer is enabled with the Low Frequency Oscillator (LFO0) as its clock source. Program execution begins at location 0x0000.

2.8. On-Chip Debugging

The C8051F85x/86x devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.2. C8051F850/1/2/3/4/5 QFN20 Pin Definitions

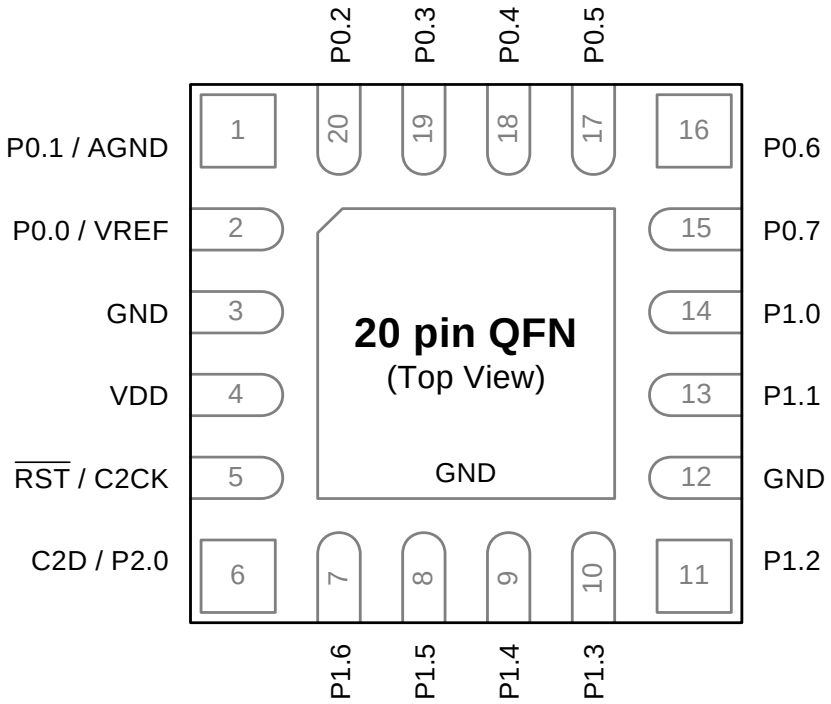


Figure 3.2. C8051F850/1/2/3/4/5-GM and C8051F850/1/2/3/4/5-IM Pinout

Table 3.2. Pin Definitions for C8051F850/1/2/3/4/5-GM and C8051F850/1/2/3/4/5-IM

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	Center 3 12			
VDD	Power	4			
$\overline{\text{RST}}$ / C2CK	Active-low Reset / C2 Debug Clock	5			

Detector or Comparator, for example, and instructions which force a Software Reset. A global search on "RSTSRC" can quickly verify this.

10.4.2. PSWE Maintenance

7. Reduce the number of places in code where the PSWE bit (in register PSCTL) is set to a 1. There should be exactly one routine in code that sets PSWE to a '1' to write flash bytes and one routine in code that sets PSWE and PSEE both to a '1' to erase flash pages.
8. Minimize the number of variable accesses while PSWE is set to a 1. Handle pointer address updates and loop variable maintenance outside the "PSWE = 1;... PSWE = 0;" area. Code examples showing this can be found in “AN201: Writing to Flash From Firmware", available from the Silicon Laboratories web site.
9. Disable interrupts prior to setting PSWE to a '1' and leave them disabled until after PSWE has been reset to 0. Any interrupts posted during the flash write or erase operation will be serviced in priority order after the flash operation has been completed and interrupts have been re-enabled by software.
10. Make certain that the flash write and erase pointer variables are not located in XRAM. See your compiler documentation for instructions regarding how to explicitly locate variables in different memory areas.
11. Add address bounds checking to the routines that write or erase flash memory to ensure that a routine called with an illegal address does not result in modification of the flash.

10.4.3. System Clock

12. If operating from an external crystal-based source, be advised that crystal performance is susceptible to electrical interference and is sensitive to layout and to changes in temperature. If the system is operating in an electrically noisy environment, use the internal oscillator or use an external CMOS clock.
13. If operating from the external oscillator, switch to the internal oscillator during flash write or erase operations. The external oscillator can continue to run, and the CPU can switch back to the external oscillator after the flash operation has completed.

Additional flash recommendations and example code can be found in “AN201: Writing to Flash From Firmware", available from the Silicon Laboratories website.

Table 15.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2
Boolean Manipulation			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/3
JNC rel	Jump if Carry is not set	2	2/3
JB bit, rel	Jump if direct bit is set	3	3/4
JNB bit, rel	Jump if direct bit is not set	3	3/4
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/4
Program Branching			
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3

20.1. PCA Counter/Timer

The 16-bit PCA counter/timer consists of two 8-bit SFRs: PCA0L and PCA0H. PCA0H is the high byte of the 16-bit counter/timer and PCA0L is the low byte. Reading PCA0L automatically latches the value of PCA0H into a “snapshot” register; the following PCA0H read accesses this “snapshot” register. **Reading the PCA0L Register first guarantees an accurate reading of the entire 16-bit PCA0 counter.** Reading PCA0H or PCA0L does not disturb the counter operation. The CPS2–CPS0 bits in the PCA0MD register select the timebase for the counter/timer as shown in Table 20.1.

When the counter/timer overflows from 0xFFFF to 0x0000, the Counter Overflow Flag (CF) in PCA0MD is set to logic 1 and an interrupt request is generated if CF interrupts are enabled. Setting the ECF bit in PCA0MD to logic 1 enables the CF flag to generate an interrupt request. The CF bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Clearing the CIDL bit in the PCA0MD register allows the PCA to continue normal operation while the CPU is in Idle mode.

Table 20.1. PCA Timebase Input Options

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)*
1	0	0	System clock
1	0	1	External oscillator source divided by 8*
1	1	0	Low frequency oscillator divided by 8*
1	1	1	Reserved

***Note:** Synchronized with the system clock.

20.2. PCA0 Interrupt Sources

The PCA0 module shares one interrupt vector among all of its modules. There are are several event flags that can be used to generate a PCA0 interrupt. They are: the main PCA counter overflow flag (CF), which is set upon a 16-bit overflow of the PCA0 counter, an intermediate overflow flag (COVF), which can be set on an overflow from the 8th - 11th bit of the PCA0 counter, and the individual flags for each PCA channel (CCFn), which are set according to the operation mode of that module. These event flags are always set when the trigger condition occurs. Each of these flags can be individually selected to generate a PCA0 interrupt, using the corresponding interrupt enable flag (ECF for CF, ECOV for COVF, and ECCFn for each CCFn). PCA0 interrupts must be globally enabled before any individual interrupt sources are recognized by the processor. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1.

Register 20.6. PCA0L: PCA Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0L							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xF9								

Table 20.8. PCA0L Register Bit Descriptions

Bit	Name	Function
7:0	PCA0L	**PCA Counter/Timer Low Byte.** The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.

Register 20.8. PCA0CPL0: PCA Capture Module Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPL0							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xFB								

Table 20.10. PCA0CPL0 Register Bit Descriptions

Bit	Name	Function
7:0	PCA0CPL0	**PCA Capture Module Low Byte.** The PCA0CPL0 register holds the low byte (LSB) of the 16-bit capture module.This register address also allows access to the low byte of the corresponding PCA channels auto-reload value for 9 to 11-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.
Note: A write to this register will clear the module's ECOM bit to a 0.		

21.1. General Port I/O Initialization

Port I/O initialization consists of the following steps:

1. Select the input mode (analog or digital) for all port pins, using the Port Input Mode register (PnMDIN).
2. Select the output mode (open-drain or push-pull) for all port pins, using the Port Output Mode register (PnMDOUT).
3. Select any pins to be skipped by the I/O crossbar using the Port Skip registers (PnSKIP).
4. Assign port pins to desired peripherals.
5. Enable the crossbar (XBARE = ‘1’).

All port pins must be configured as either analog or digital inputs. Any pins to be used as Comparator or ADC inputs should be configured as an analog inputs. When a pin is configured as an analog input, its weak pullup, digital driver, and digital receiver are disabled. This process saves power and reduces noise on the analog input. Pins configured as digital inputs may still be used by analog peripherals; however this practice is not recommended.

Additionally, all analog input pins should be configured to be skipped by the crossbar (accomplished by setting the associated bits in PnSKIP). Port input mode is set in the PnMDIN register, where a ‘1’ indicates a digital input, and a ‘0’ indicates an analog input. All pins default to digital inputs on reset.

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMDOUT). Each port output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is the SMBus (SDA, SCL) pins, which are configured as open-drain regardless of the PnMDOUT settings. When the WEAKPUD bit in XBR1 is ‘0’, a weak pullup is enabled for all Port I/O configured as open-drain. WEAKPUD does not affect the push-pull Port I/O. Furthermore, the weak pullup is turned off on an output that is driving a ‘0’ to avoid unnecessary power dissipation.

Registers XBR0 and XBR1 must be loaded with the appropriate values to select the digital I/O functions required by the design. Setting the XBARE bit in XBR2 to ‘1’ enables the crossbar. Until the crossbar is enabled, the external pins remain as standard port I/O (in input mode), regardless of the XBRn Register settings. For given XBRn Register settings, one can determine the I/O pin-out using the Priority Decode Table; as an alternative, Silicon Labs provides configuration utility software to determine the port I/O pin-assignments based on the crossbar register settings.

The crossbar must be enabled to use port pins as standard port I/O in output mode. Port output drivers of all crossbar pins are disabled whenever the crossbar is disabled.

Register 21.18. P2MDOUT: Port 2 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	Reserved						P2MDOUT	
Type	R						RW	
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xA6								

Table 21.21. P2MDOUT Register Bit Descriptions

Bit	Name	Function
7:2	Reserved	Must write reset value.
1:0	P2MDOUT	**Port 2 Output Mode.** 0: Corresponding P2.n Output is open-drain. 1: Corresponding P2.n Output is push-pull.
Note: Port 2 consists of 2 bits (P2.0-P2.1) on QSOP24 devices and 1 bit (P2.0) on QFN20 and SOIC16 packages.		

Register 24.4. SMB0ADR: SMBus0 Slave Address

Bit	7	6	5	4	3	2	1	0
Name	SLV							GC
Type	RW							RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xD7								

Table 24.10. SMB0ADR Register Bit Descriptions

Bit	Name	Function
7:1	SLV	**SMBus Hardware Slave Address.** Defines the SMBus0 Slave Address(es) for automatic hardware acknowledgement. Only address bits which have a 1 in the corresponding bit position in SLVM are checked against the incoming address. This allows multiple addresses to be recognized.
0	GC	**General Call Address Enable.** When hardware address recognition is enabled (EHACK = 1), this bit will determine whether the General Call Address (0x00) is also recognized by hardware. 0: General Call Address is ignored. 1: General Call Address is recognized.

Register 25.4. TL0: Timer 0 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL0							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x8A								

Table 25.6. TL0 Register Bit Descriptions

Bit	Name	Function
7:0	TL0	**Timer 0 Low Byte.** The TL0 register is the low byte of the 16-bit Timer 0.

Register 25.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH0							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x8C								

Table 25.8. TH0 Register Bit Descriptions

Bit	Name	Function
7:0	TH0	**Timer 0 High Byte.** The TH0 register is the high byte of the 16-bit Timer 0.

Register 25.10. TMR2RLH: Timer 2 Reload High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2RLH							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0xCB								

Table 25.12. TMR2RLH Register Bit Descriptions

Bit	Name	Function
7:0	TMR2RLH	**Timer 2 Reload High Byte.** When operating in one of the auto-reload modes, TMR2RLH holds the reload value for the high byte of Timer 2 (TMR2H). When oeprating in capture mode, TMR2RLH is the captured value of TMR2H.

Register 25.15. TMR3RLH: Timer 3 Reload High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLH							
Type	RW							
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x93								

Table 25.17. TMR3RLH Register Bit Descriptions

Bit	Name	Function
7:0	TMR3RLH	**Timer 3 Reload High Byte.** When operating in one of the auto-reload modes, TMR3RLH holds the reload value for the high byte of Timer 3 (TMR3H). When oeprating in capture mode, TMR3RLH is the captured value of TMR3H.

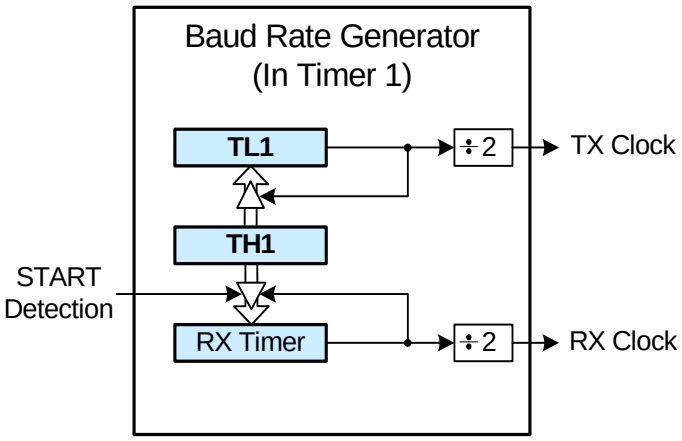


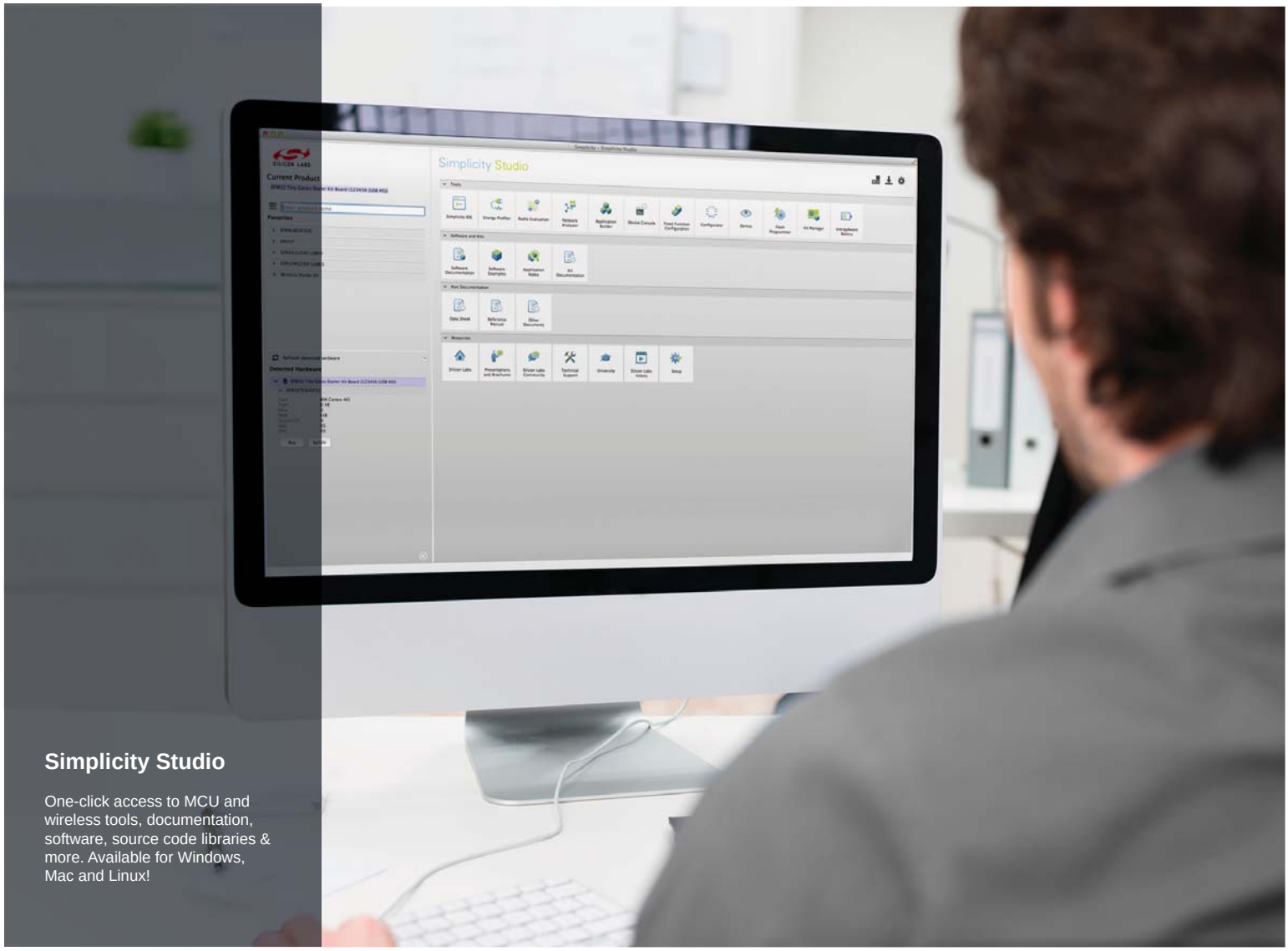
Figure 26.2. UART0 Baud Rate Logic

Timer 1 should be configured for Mode 2, 8-bit auto-reload. The Timer 1 reload value should be set so that overflows will occur at two times the desired UART baud rate frequency. Note that Timer 1 may be clocked by one of six sources: SYSCLK, SYSCLK/4, SYSCLK/12, SYSCLK/48, the external oscillator clock/8, or an external input T1. For any given Timer 1 overflow rate, the UART0 baud rate is determined by Equation 26.1.

$$\text{UartBaudRate} = \frac{1}{2} \times \text{T1\_Overflow\_Rate}$$

Equation 26.1. UART0 Baud Rate

Timer 1 overflow rate is selected as described in the Timer section. A quick reference for typical baud rates and system clock frequencies is given in Table 26.1.



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