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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

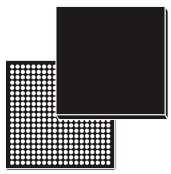
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	450MHz
Co-Processors/DSP	ARM® Cortex®-M3
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	LCD, Touchscreen
Ethernet	-
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-TFBGA
Supplier Device Package	256-TFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/sta1079eoa

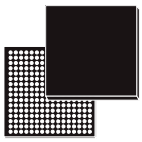
STA1074, STA1078 STA1079, STA1088

Telemaco2 family of telematics and connectivity microprocessors

Data brief



LFBGA361
(16 x 16 x 1.7 mm)



TFBGA256
(11 x 11 x 1.2 mm)

GAPG0209150756PS

Features

Core and infrastructure

- ARM® Cortex™-R4 MCU
- Embedded SRAM
- SDRAM controller
- Serial QIO NOR interface executable in place
- Parallel NAND/NOR controller

Audio subsystem

- Stereo channels hardware Sample Rate Converter
- Digital audio interfaces (I2S/ multichannel ports)
- Stereo audio DAC with 103 dB SNR A-Weighted
- Single ended stereo ADC with internal switching logic
- Differential Mono ADC with internal switching logic

Media interfaces

- Secure-Digital Multimedia Memory Card Interfaces (SD3.0/MMC4.4/SDIO)
- USB 2.0 with integrated PHY with charging function support

Embedded secure CAN subsystem

- Dedicated ARM Cortex-M3 core
- Isolated embedded memory
- CAN ports
- Secured NOR interface

I/O interfaces

- General purpose ADCs
- I2C multi-master/slave interfaces
- UART Controllers
- Synchronous Serial Ports (SSP/SPI)
- GPIOs
- JTAG based in-circuit emulator (ICE) with Embedded Trace Module

Operating conditions

- VDD: 1.14 V - 1.26 V
- VDDIO: 3.3 V ±10%
- VDDIOON: 3.3 V ±10%
- Ambient temperature range: -40 / +85 °C

Contents

1 Description

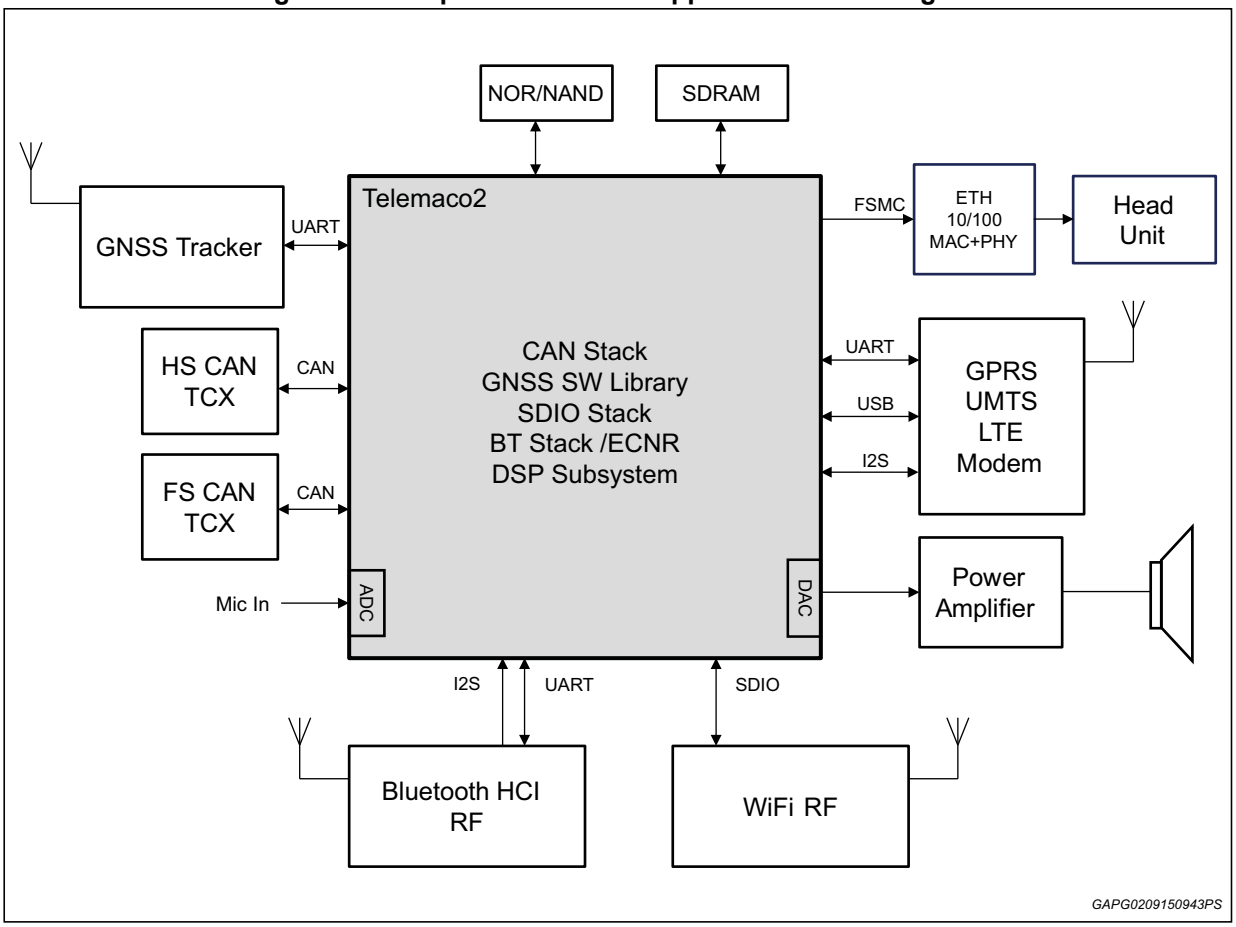
Devices from Telemaco2 family provide a cost effective microprocessor solution for automotive telematics applications based on a MIPS efficient ARM - Cortex R4 processor.

In addition, an ARM - Cortex M3 controller is dedicated to real-time processing tasks.

Telemaco2 devices come with a complete set of common interfaces (UART/I2S/I2C/USB/MMC) which make this family optimal for implementing a feature reach system as well as a cost effective solutions for automotive connectivity.

Telemaco2 devices can provide enough processing capability to handle positioning and wireless data management typically required in telematics use cases. Moreover, they can handle the control of the in-vehicle CAN bus thanks to the independent and secure Cortex-M3 subsystem running its dedicated real-time OS. With its flexible memory configuration, they allow implementing a variety of systems, starting from very low cost applications based on a real time OS and scaling up to demanding applications based on rich Linux OS.

Figure 1. Example of telematics application block diagram



2 System description

2.1 Processor MCU

Telemaco2 family devices processing capability relies on an ARM Cortex-R4. The MCU has instruction cache and data cache, as well as TCM Memory dedicated respectively to instructions and data for high throughput and low latency tasks.

2.2 Memory controller

2.2.1 Embedded memory

Telemaco2 family devices embed SRAM memory, which can be used for data or code storage.

Embedded memory can be used in conjunction with executable in place serial NOR devices to implement cost effective solutions. The whole embedded memory is also cacheable and can be accessed by DMA.

2.2.2 SDRAM controller

SDRAM controller supports SDRAM JEDEC interface 16-bits wide, which allows interfacing to automotive SDRAM memory devices to handle high footprint applications.

Such memory is cacheable, and can be accessed by DMA.

2.2.3 SQI executable in place

The SQIO controller allows interfacing Serial Quad I/O flash memories.

2.2.4 Parallel memory interface

FSMC static memory controller, provides a generic 16-bits parallel interface suitable to connect to NOR devices as well as SRAM and NAND devices.

NOR memory space can be partitioned so to reserve a portion of the parallel NOR device to the Secure CAN Subsystem.

2.3 USB

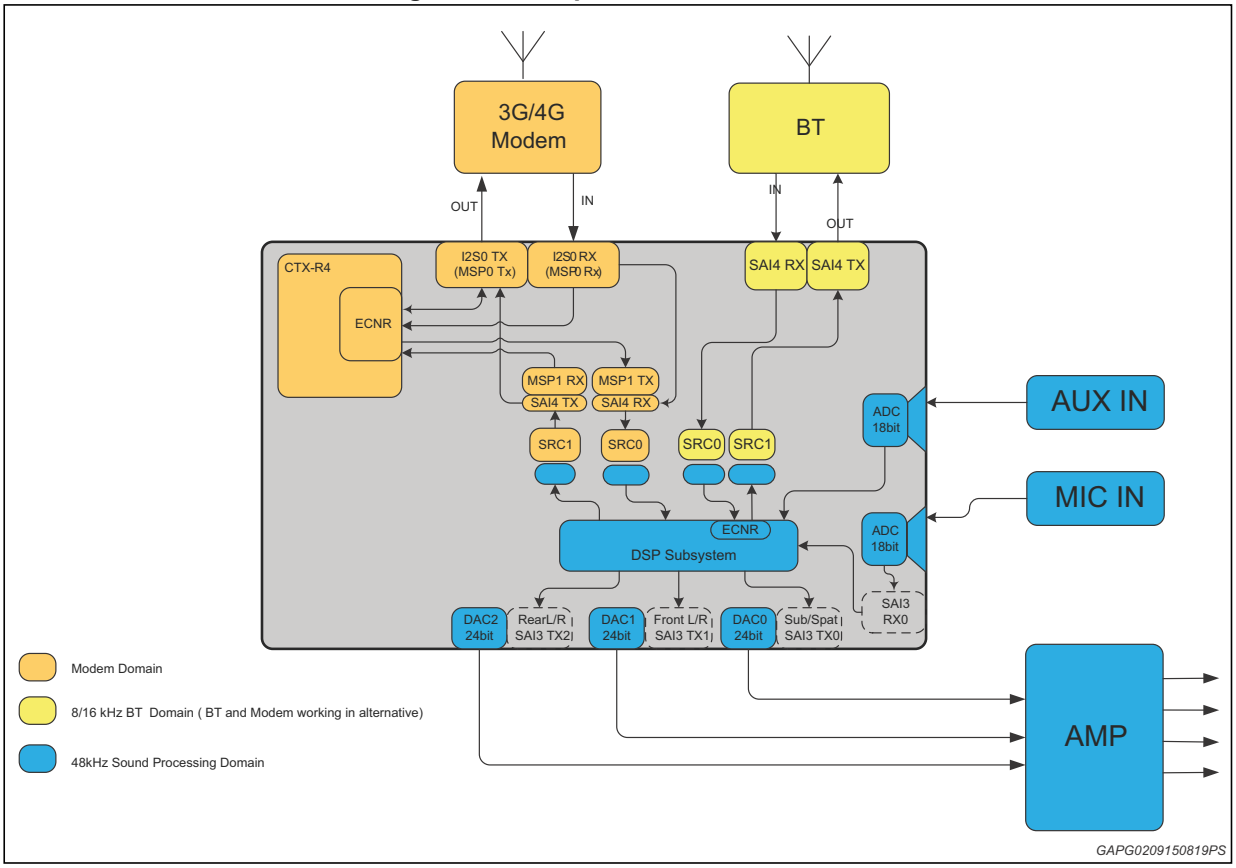
Telemaco2 family devices have one Host and one Dual role USB HS with embedded PHY, allowing connecting efficiently to mass storage devices, as well as portable devices (phones, pads). Along with USB connectivity, Telemaco2 family fully support USB charger specification.

2.4 Sound subsystem

Telemaco2 family devices implement a sound subsystem which allows the routing and the rate conversion of the different audio sources.

An application case which includes the connection of a 3G/4G Modem and of an optional BT is represented in the following *Figure 2*.

Figure 2. Example of sound use case



2.5 Audio interfaces

A complete set of audio interfaces is provided, in order to simplify integration with speakers, and input sources. Each interface can be routed to the sound subsystem. A complete list of audio interfaces is provided below:

- Audio ADC
  - For AUX IN Line
  - ADC Input is single ended 3.3 V
- Voice ADC
  - Shared among Voice and TEL-IN lines with embedded multiplexer
  - Both Mic and TEL-IN are differential inputs
- Stereo DAC
- Multiple I2S IN
- Multiple I2S OUT

2.5.1 Routing and sample rate converters

Each audio interface can be routed in both directions (IN/OUT) through sample rate converters, which allow normalizing the sampling rate to the sound processing engine. The audio routing infrastructure is designed to deliver high quality sample rate conversion on multiple channels, allowing simultaneous audio streams, such as Bluetooth Hands Free, to be handled without CPU load.

In order to generate multiple sampling rate audio frequencies, a dedicated fractional PLL is also provided. This PLL also allows an efficient implementation of cellular modem playback, by dynamically adjusting the reconstructed audio sampling rate without CPU overload.

2.5.2 DSP Subsystem

Some devices in Telemaco2 family are equipped with an embedded DSP subsystem dedicated to sound processing and other signal processing intensive tasks, like echo/noise cancellation, sound effects generation. DSP subsystem is integrated with the sound subsystem with a specific isochronous bus.

Each DSP is connected to other DSPs and audio peripherals by means of an isochronous bus infrastructure which guarantees a controlled throughput and latency for all audio transfers.

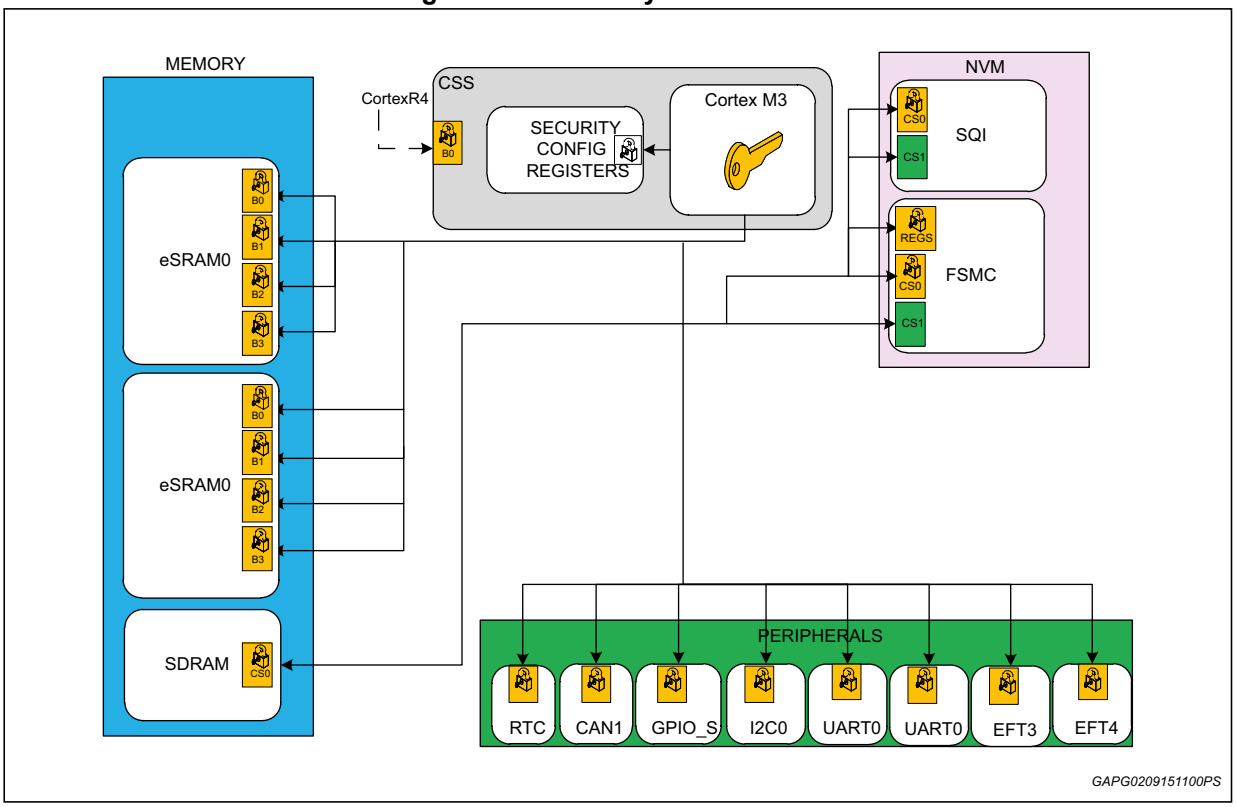
2.6 Secure CAN subsystem

Telemaco2 family devices allow isolating critical code from main application by implementing a dedicated subsystem based on ARM Cortex-M3, along with:

- Dedicated embedded SRAM
- CAN controller
- Dedicated GPIOs

In order to guarantee security of CAN network, all of the above can be completely isolated from the rest of the system, in such a way that no application running on CorteX-R4 can access by any mean to CAN specific re-sources. This subsystem can also be dedicated to implement secure features, such as boot authentication, as well as interrupt intensive tasks to offload main CPU. The secure subsystem communicates with the application running on CortexR4 using a Hardware Mailbox interrupt based mechanism.

Figure 3. CAN subsystem isolation



A specific set of peripherals can be reserved and locked to be only accessible from CortexM3, thus allowing the implementation of a complete independent subsystem. Moreover, specific secure GPIOs as well as wake signals are reserved for such a subsystem.

2.7 SDMMC

Telemaco2 family devices are equipped with SDMMC controllers, which allow interfacing to either mass storage devices, or to Wi-Fi modules. Both interfaces implement the following specification:

- eMMC - Multimedia Card 4.4
- SD/SDIO 4.0

2.8 DMA

DMA is designed to efficiently perform memory to memory, and memory to peripherals transfers, offloading such tasks from the processor, thus reducing interrupt handling load. DMA provides 16 independent channels which can be dynamically assigned to different data- path. Complex Scatter/gather transfers can be implemented by programming specific DMA command linked lists.

2.9 General purpose ADC

Telemaco2 family devices have ADC with a resolution of 10-bits.

2.10 GPIOs

Telemaco2 family devices have GPIOs which can be independently configured either as INPUT or OUTPUT. In order to make the system flexible, these IOs are multiplexed on PINs with other peripherals.

2.11 Generic interfaces

2.11.1 UARTS

- Programmable baud rates up to 3 Mbps
- Hardware Flow control
- DMA capability

2.11.2 I^2Cs

- Master/slave modes in multi-master environment
- Multiple baud rates supported: 100/400/1000/3400 Kbits/s
- DMA capability

2.11.3 SSP/SPI ports supporting

- Motorola SPI-compatible interface
- Texas Instrument synchronous serial interface
- National Semiconductor MICROWIRE® interface
- Unidirectional interface
- DMA capability

2.12 Power modes

Telemaco2 family devices support the following power modes:

- Normal
- Soft standby (Normal mode with clock gating)
- Standby
- Power Off

The SoC requires three power lines for internal logic (excluding analog block power lines), which are identified as:

- 3V3 Standby
- 3V3 IOs, switchable
- 1V2 Core, switchable

In each power state, the SoC is permanently protected from voltage drops by means of a brownout logic, which would trigger a system reset in case of a low voltage condition is detected.

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

3.1 TFBGA256 (11x11x1.2 mm) package information

Figure 4. TFBGA256 (11x11x1.2 mm) package outline

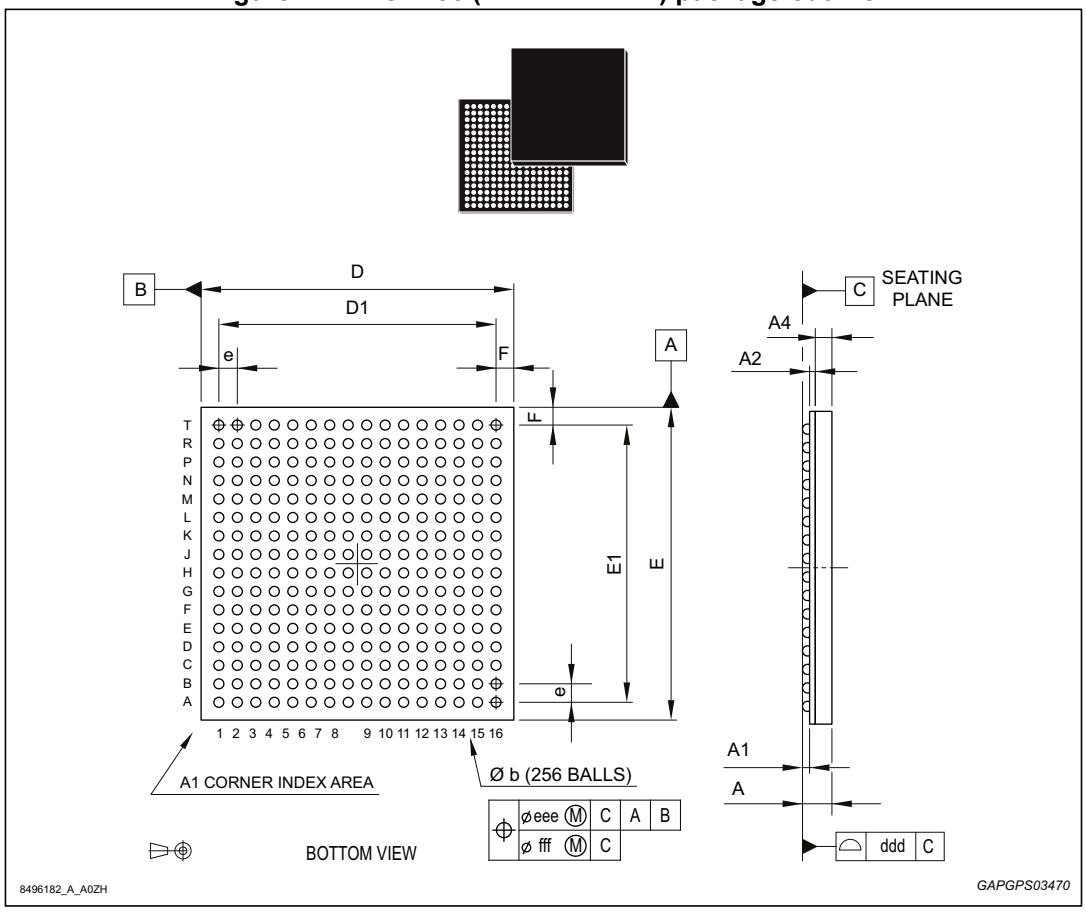


Table 1. TFBGA256 (11x11x1.2 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.200	-	-	0.0079	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.620	-	-	0.0244
b	0.300	0.370	0.430	0.0118	0.0146	0.0169
D	10.850	11.000	11.150	0.4272	0.4331	0.4390
D1	-	9.750	-	-	0.3839	-
E	10.850	11.000	11.150	0.4272	0.4331	0.4390
E1	-	9.750	-	-	0.3839	-
e	-	0.650	-	-	0.0256	-
Z	-	0.625	-	-	0.0246	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

3.2 LFBGA361 (16x16x1.7 mm) package information

Figure 5. LFBGA361 (16x16x1.7 mm) package outline

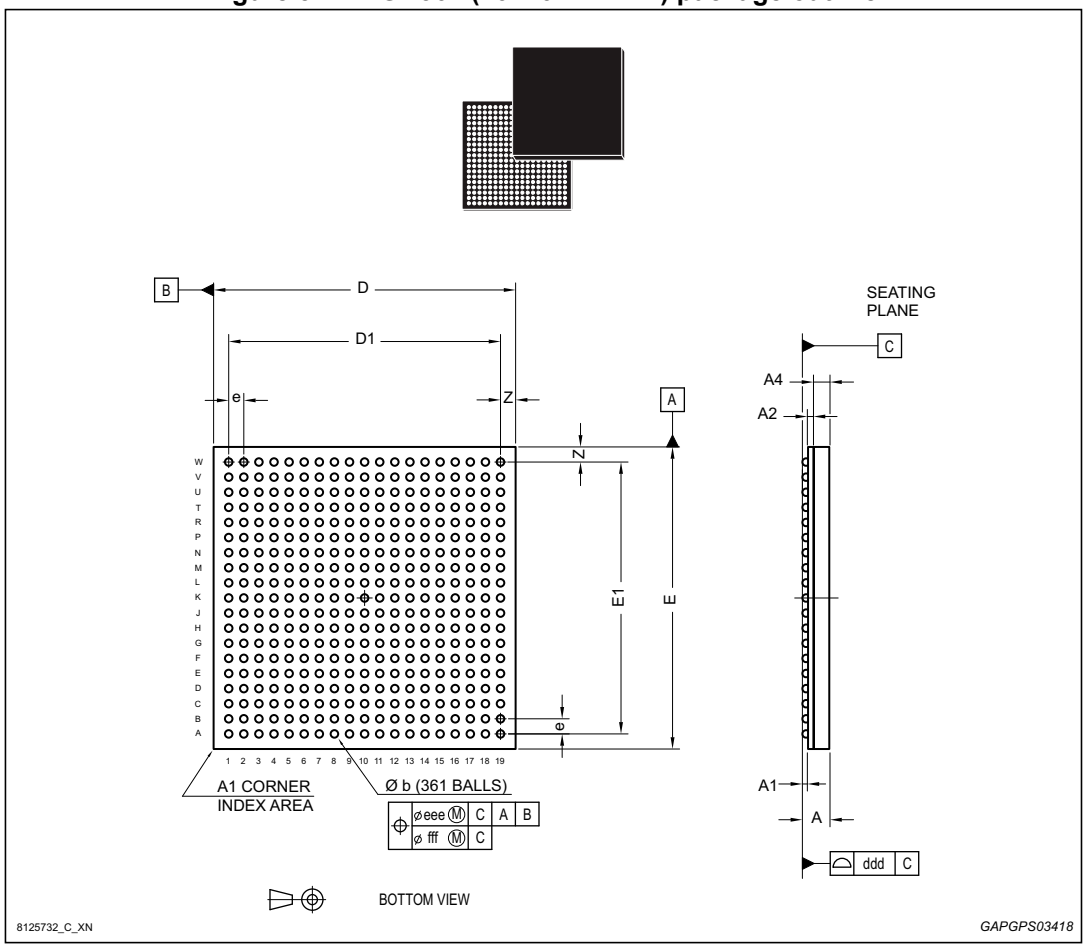


Table 2. LFBGA361 (16x16x1.7 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.7	-	-	0.0669
A1	0.25	-	-	0.0098	-	-
A2	-	0.3	-	-	0.0118	-
A4	-	-	0.8	-	-	0.0315
b	0.35	0.4	0.48	0.0138	0.0157	0.0189
D	15.85	16	16.15	0.624	0.6299	0.6358
D1	-	14.4	-	-	0.5669	-
E	15.85	16	16.15	0.624	0.6299	0.6358
E1	-	14.4	-	-	0.5669	-
e	-	0.8	-	-	0.0315	-
Z	-	0.8	-	-	0.0315	-
ddd	-	-	0.1	-	-	0.0039
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

4 Order codes

Table 3. Telemaco2 product versions

	STA1074	STA1078	STA1079	STA1088
SDRAM	16 bit			32 bit
CAN	No	2x	1x	2x
Audio DACs	No	1x Stereo	3x Stereo	
Audio ADCs	No	1x Stereo/1x Mono		
DSP Subsystem	No	No	Yes	Yes
Package	TFBGA256 (11x11 mm)			LFBGA361 (16x16 mm)

Table 4. Ordering information

[Root] Root Code	[Freq] CortexR4 Frequency	[Sec] Security	[Grade] Qualification Grade	[Pack] Packing
STA1074 **STA1078** **STA1079** **STA1088**	**E** = Eco (450MHz)	**L** = Locked	**A** = Automotive	**[empty]** = Tray
	H = High (533MHz)	**O** = Open	**C** = Consumer	**TR** = Tape & Reel
	P = Premium (600 MHz)			
Part number example: **STA1078EOA**				
STA1078	**E** = Eco (450 MHz)	**O** = Open	**A** = Automotive	**[empty]** = Tray

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
11-Sep-2015	1	Initial release.