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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	98
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f585lapmc-gtk5e1

MB91580S Series Product Lineup Comparison

- Memory size

Items	MB91F583SG MB91F583SH MB91F583SJ MB91F583SK	MB91F584SG MB91F584SH MB91F584SJ MB91F584SK	MB91F585SG MB91F585SH MB91F585SJ MB91F585SK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

- Function

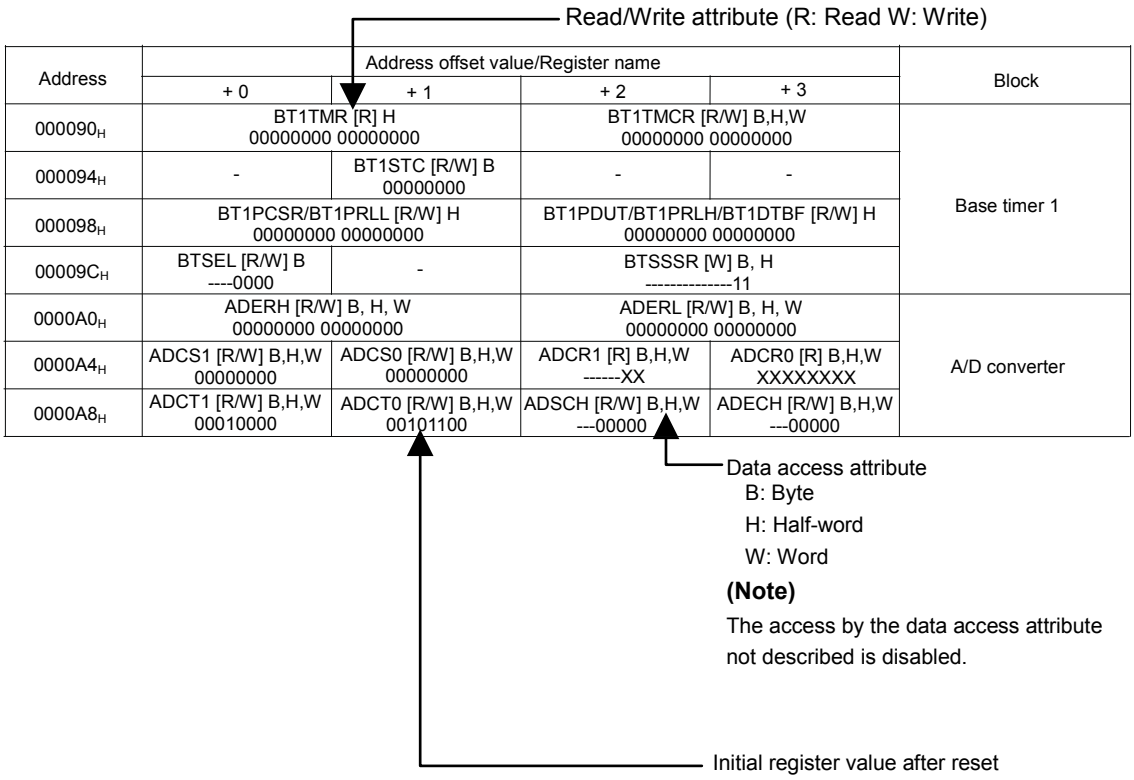
Items	MB91F583SG MB91F584SG MB91F585SG	MB91F583SH MB91F584SH MB91F585SH	MB91F583SJ MB91F584SJ MB91F585SJ	MB91F583SK MB91F584SK MB91F585SK
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during stand-by	Provided	Provided	Not provided	Not provided
External bus interface	Not provided			
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	4 channels			
Output compare	7 channels			
Waveform generator	2 unit (7channels)			
16-bit reload timer	4 channels			
PPG	6 channels			
External interrupt	7 channels			
A/D converter	3 units (17 channels)			
R/D converter	Not provided			
D/A converter	Provided			
Up/ down counter	2 channels			
Multi-function serial interface	2 channels			
CAN	64msb × 1 channel (ch.0)			
FlexRay	128msb × 1unit (ch.A / ch.B)	Not provided	128msb × 1unit (ch.A / ch.B)	Not provided
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	2 channels			
Low-voltage detection reset (Internal low-voltage detection)	Provided			
Low-voltage detection reset (External low-voltage detection)	Provided			
Device package	LQFP-64			
Debug interface	Built-in OCD (On Chip Debug Unit)			

Note: For details on the MB91580S series, see the "MB91580M/S Series HARDWARE MANUAL".

■ I/O MAP

The following I/O map shows the relationship between memory space and registers for peripheral resources.

- Legend of I/O Map



Address	Address offset value/Register name				Block
	+ 0	+ 1	+ 2	+ 3	
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] B,H,W 00000000 00000000		Base timer 1
000094_H	-	BT1STC [R/W] B 00000000	-	-	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL [R/W] B ----0000	-	BTSSSR [W] B, H ----------11		
$0000A0_H$	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B,H,W 00000000	ADCS0 [R/W] B,H,W 00000000	ADCR1 [R] B,H,W ------XX	ADCR0 [R] B,H,W XXXXXXXX	
$0000A8_H$	ADCT1 [R/W] B,H,W 00010000	ADCT0 [R/W] B,H,W 00101100	ADSCH [R/W] B,H,W ---00000	ADECH [R/W] B,H,W ---00000	

The initial register values after reset are indicated as follows:

"1": Initial value "1"
"0": Initial value "0"
"X": Initial value undefined
"-": Reserved bit/Undefined bit
"*": Initial value "0" or "1" according to the setting

Note:

It is prohibited to access addresses not described here.

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000588_H | $00058C_H$	-	-	-	-	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H | $00060C_H$	-	-	-	-	Reserved [S]
000610_H | $00063C_H$	-	-	-	-	Reserved [S]
000640_H | $00064C_H$	-	-	-	-	Reserved [S]
000650_H | $00067C_H$	-	-	-	-	Reserved [S]
000680_H | $00068C_H$	-	-	-	-	Reserved [S]
000690_H | $0006BC_H$	-	-	-	-	Reserved [S]
$0006C0_H$ | $0006CC_H$	-	-	-	-	Reserved [S]
$0006D0_H$ | $0006F0_H$	-	-	-	-	Reserved
$0006F4_H$	-				Reserved
$0006F8_H$ | $0006FC_H$	-	-	-	-	Reserved
000700_H	-				Reserved
000704_H | $00070C_H$	-	-	-	-	Reserved
000710_H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	-	Bus performance counter
000714_H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00156C_H$	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000000-0	SSR3[R/W] B,H,W 0--00011	ESCR3/(IBSR3) [R/W] B,H,W 00000000	Multi Function Serial I/F 3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001570_H	-/(RDR13/(TDR13))[R/W] H,W -------- -------- *3		RDR03/(TDR03)[R/W] B,H,W -------0 00000000 *1		
001574_H	SACSR3[R/W] B,H,W 0----000 00000000		STMR3[R] B,H,W 00000000 00000000		
001578_H	STMCR3[R/W] B,H,W 00000000 00000000		-/(SCSCR3/SFUR3) [R/W] B,H,W -------- -------- *3,*4		
$00157C_H$	-/(SCSTR33) [R/W] B,H,W -------- *3	-/(SCSTR23) [R/W] B,H,W -------- *3	-/(SCSTR13/SFLR13) [R/W] B,H,W -------- *3,*4	-/(SCSTR03/SFLR03) [R/W] B,H,W -------- *3,*4	
001580_H	-	-	-	-	
001584_H	-	-	-	TBYTE03[R/W] B,H,W 00000000	
001588_H	BGR3[R/W] H,W 00000000 00000000		-/(ISMK3)[R/W] B,H,W -------- *2	-/(ISBA3)[R/W] B,H,W -------- *2	
$00158C_H$	FCR13[R/W] B,H,W 00-00100	FCR03[R/W] B,H,W -0000000	FBYTE23[R/W] B,H,W 00000000	FBYTE13[R/W] B,H,W 00000000	
001590_H	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4[R/W] B,H,W 000000-0	SSR4[R/W] B,H,W 0--00011	ESCR4/(IBSR4) [R/W] B,H,W 00000000	Multi Function Serial I/F 4 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001594_H	-/(RDR14/(TDR14))[R/W] H,W -------- -------- *3		RDR04/(TDR04)[R/W] B,H,W -------0 00000000 *1		
001598_H	SACSR4[R/W] B,H,W 0----000 00000000		STMR4[R] B,H,W 00000000 00000000		
$00159C_H$	STMCR4[R/W] B,H,W 00000000 00000000		-/(SCSCR4/SFUR4) [R/W] B,H,W -------- -------- *3,*4		
$0015A0_H$	-/(SCSTR34) [R/W] B,H,W -------- *3	-/(SCSTR24) [R/W] B,H,W -------- *3	-/(SCSTR14/SFLR14) [R/W] B,H,W -------- *3,*4	-/(SCSTR04/SFLR04) [R/W] B,H,W -------- *3,*4	
$0015A4_H$	-	-/(SCSFR24)[R/W] B,H,W -------- *3	-/(SCSFR14)[R/W] B,H,W -------- *3	-/(SCSFR04)[R/W] B,H,W -------- *3	
$0015A8_H$	-/(TBYTE34)[R/W] B,H,W -------- *3	-/(TBYTE24)[R/W] B,H,W -------- *3	-/(TBYTE14)[R/W] B,H,W -------- *3	TBYTE04[R/W] B,H,W 00000000	
$0015AC_H$	BGR4[R/W] H,W 00000000 00000000		-/(ISMK4)[R/W] B,H,W -------- *2	-/(ISBA4)[R/W] B,H,W -------- *2	
$0015B0_H$	FCR14[R/W] B,H,W 00-00100	FCR04[R/W] B,H,W -0000000	FBYTE24[R/W] B,H,W 00000000	FBYTE14[R/W] B,H,W 00000000	
$0015B4_H$ | $001FFC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000100_H	TMRLRA1[R/W] H XXXXXXXX XXXXXXXX		TMR1[R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104_H	TMRLRB1[R/W] H XXXXXXXX XXXXXXXX		TMCSR1[R/W] B,H,W 00000000 0-000000		
000108_H	TMRLRA2[R/W] H XXXXXXXX XXXXXXXX		TMR2[R] H XXXXXXXX XXXXXXXX		Reload timer 2
$00010C_H$	TMRLRB2[R/W] H XXXXXXXX XXXXXXXX		TMCSR2[R/W] B,H,W 00000000 0-000000		
000110_H	TMRLRA3[R/W] H XXXXXXXX XXXXXXXX		TMR3[R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114_H	TMRLRB3[R/W] H XXXXXXXX XXXXXXXX		TMCSR3[R/W] B,H,W 00000000 0-000000		
000118_H | $00011C_H$	-	-	-	-	Reserved
000120_H	IRPR0H[R] B,H,W 00------	IRPR0L[R] B,H,W 00------	IRPR1H[R] B,H,W 00------	IRPR1L[R] B,H,W --------	Interrupt request batch read register
000124_H	IRPR2H[R] B,H,W --------	IRPR2L[R] B,H,W 0000----	IRPR3H[R] B,H,W 00------	IRPR3L[R] B,H,W 00------	
000128_H	IRPR4H[R] B,H,W 00------	IRPR4L[R] B,H,W 000000--	IRPR5H[R] B,H,W 00------	IRPR5L[R] B,H,W 00------	
$00012C_H$	IRPR6H[R] B,H,W 000000--	IRPR6L[R] B,H,W 000000--	IRPR7H[R] B,H,W 000000--	IRPR7L[R] B,H,W 000000--	
000130_H	IRPR8H[R] B,H,W 000000--	IRPR8L[R] B,H,W 00------	IRPR9H[R] B,H,W 00------	IRPR9L[R] B,H,W 00------	
000134_H	IRPR10H[R] B,H,W 00------	IRPR10L[R] B,H,W 00------	IRPR11H[R] B,H,W 00------	IRPR11L[R] B,H,W 0000000-	
000138_H	IRPR12H[R] B,H,W 0000000-	IRPR12L[R] B,H,W 00000000	IRPR13H[R] B,H,W 00000000	IRPR13L[R] B,H,W 00000000	
$00013C_H$	IRPR14H[R] B,H,W 00------	IRPR14L[R] B,H,W 00------	IRPR15H[R] B,H,W 00000000	IRPR15L[R] B,H,W 00000---	
000140_H	IRPR16H[R] B,H,W 00------	IRPR16L[R] B,H,W 00------	IRPR17H[R] B,H,W 00------	IRPR17L[R] B,H,W 00------	
000144_H	IRPR18H[R] B,H,W 00------	IRPR18L[R] B,H,W 000000--	-	-	
000148_H | $0001FC_H$	-	-	-	-	Reserved
000200_H	PCN0[R/W] B,H,W 00000000 000000-0		PCSR0[W] H,W XXXXXXXX XXXXXXXX		PPG0
000204_H	PDUT0[W] H,W XXXXXXXX XXXXXXXX		PTMR0[R] H,W 11111111 11111111		
000208_H	PCN1[R/W] B,H,W 00000000 000000-0		PCSR1[W] H,W XXXXXXXX XXXXXXXX		PPG1
$00020C_H$	PDUT1[W] H,W XXXXXXXX XXXXXXXX		PTMR1[R] H,W 11111111 11111111		
000210_H	PCN2[R/W] B,H,W 00000000 000000-0		PCSR2[W] H,W XXXXXXXX XXXXXXXX		PPG2
000214_H	PDUT2[W] H,W XXXXXXXX XXXXXXXX		PTMR2[R] H,W 11111111 11111111		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000354_H	-	-	PACR4[R/W] H 000000-0 00000--0		MPU [S] (Only the CPU can access this area)
000358_H	PABR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	-	-	PACR5[R/W] H 000000-0 00000--0		
000360_H	PABR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	-	-	PACR6[R/W] H 000000-0 00000--0		
000368_H	PABR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	-	-	PACR7[R/W] H 000000-0 00000--0		
000370_H	-				Reserved [S]
000374_H	-	-	-		
000378_H	-				
$00037C_H$	-	-	-		
000380_H	-				
000384_H	-	-	-		
000388_H	-				
$00038C_H$	-	-	-		
000390_H	-				
000394_H	-	-	-		Reserved [S]
000398_H	-				
$00039C_H$	-	-	-		
$0003A0_H$	-				
$0003A4_H$	-	-	-		
$0003A8_H$	-				
$0003AC_H$	-	-	-		
$0003B0_H$ | $0003FC_H$	-	-	-	-	Reserved [S]
000400_H	ICSEL0[R/W] B,H,W -----000	ICSEL1[R/W] B,H,W -------0	ICSEL2[R/W] B,H,W -------0	ICSEL3[R/W] B,H,W -------0	Generation and clearing of DMA transfer requests
000404_H	ICSEL4[R/W] B,H,W -------0	ICSEL5[R/W] B,H,W -------0	ICSEL6[R/W] B,H,W -------0	ICSEL7[R/W] B,H,W -----000	
000408_H	ICSEL8[R/W] B,H,W -------0	ICSEL9[R/W] B,H,W -------0	ICSEL10[R/W] B,H,W -----000	ICSEL11[R/W] B,H,W -----000	
$00040C_H$	ICSEL12[R/W] B,H,W -----000	ICSEL13[R/W] B,H,W -----000	ICSEL14[R/W] B,H,W -----000	ICSEL15[R/W] B,H,W -------0	
000410_H	ICSEL16[R/W] B,H,W -------0	ICSEL17[R/W] B,H,W -------0	ICSEL18[R/W] B,H,W -------0	ICSEL19[R/W] B,H,W -------0	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000508_H | $00050C_H$	-	-	-	-	Reserved
000510_H	CSELR[R/W] B,H,W -0----00	CMONR[R] B,H,W -01---00	MTMCR[R/W] B,H,W 00001111	-	Clock control [S]
000514_H	PLLCR[R/W] B,H,W 00-00000 11110000		CSTBR[R/W] B,H,W ----0000	PTMCR[R/W] B,H,W 00------	
000518_H	-	-	CPUAR[R/W] B,H,W 0---XXXX	-	Reset [S]
$00051C_H$	-	-	-	-	Reserved [S]
000520_H	CCPSSELR[R/W] B,H,W -------0	-	-	CCPSDIVR[R/W] B,H,W -000-000	Clock control 2
000524_H	-	CCPLLFBR[R/W] B,H,W -0000000	CCSSFBR0[R/W] B,H,W --000000	CCSSFBR1[R/W] B,H,W ---00000	
000528_H	-	CCSSCCR0[R/W] B,H,W ----0000	CCSSCCR1[R/W] H,W 000----- --------		
$00052C_H$	-	CCCGRCR0[R/W] B,H,W 00----00	CCCGRCR1[R/W] B,H,W 00000000	CCCGRCR2[R/W] B,H,W 00000000	
000530_H	-	-	CCPMUCR0[R/W] B,H,W 0-----00	CCPMUCR1[R/W] B,H,W 0--00000	
000534_H	-	-	-	-	
000538_H	-	-	-	-	
$00053C_H$	-	-	-	-	
000540_H | $00054C_H$	-	-	-	-	Reserved
000550_H	EIRR0[R/W] B,H,W XXXXXXXX	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt (INT0 to 7)
000554_H | 000568_H	-	-	-	-	Reserved
$00056C_H$	-	CSVCR[R/W] B -0--1--0	-	-	CSV
000570_H	CRTR[R/W] B,H,W 01111111	-	-	-	WDT1 calibration (trimming)
000574_H | $00057C_H$	-	-	-	-	Reserved
000580_H	REGSEL[R/W] B,H,W 01--110-	-	-	-	Regulator control
000584_H	LVD5R[R/W] B,H,W -------1	LVD5F[R/W] B,H,W 0-010--1	LVD[R/W] B,H,W 01000--0	-	Low-voltage detection

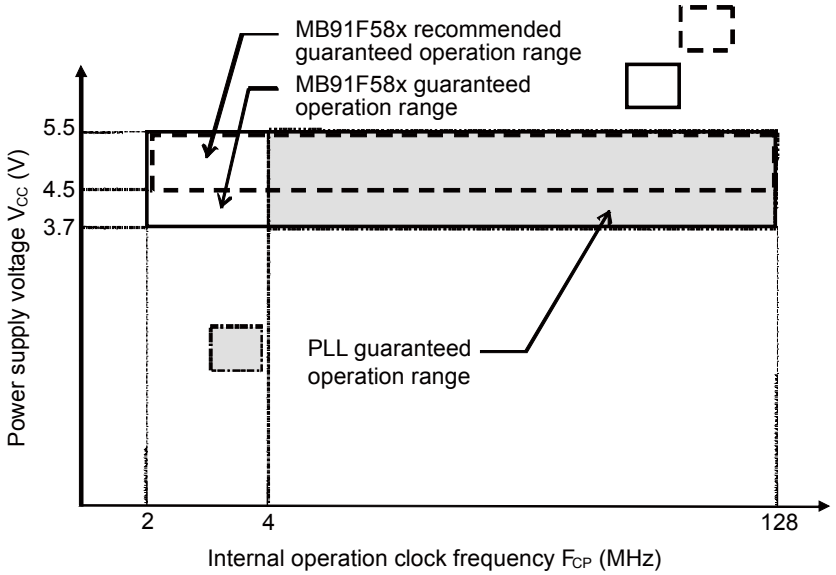
Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00110C_H$	CPCLRB1/CPCLR1[R/W] H,W 11111111 11111111		TCDT1[R/W] H,W 00000000 00000000		Free-run timer 1
001110_H	TCCS1[R/W] B,H,W 00000000 01000000 ----0000 --------				
001114_H	CPCLRB2/CPCLR2[R/W] H,W 11111111 11111111		TCDT2[R/W] H,W 00000000 00000000		Free-run timer 2
001118_H	TCCS2[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00111C_H$	CPCLRB3/CPCLR3[R/W] H,W 11111111 11111111		TCDT3[R/W] H,W 00000000 00000000		Free-run timer 3
001120_H	TCCS3[R/W] B,H,W 00000000 01000000 ----0000 --------				
001124_H	CPCLRB4/CPCLR4[R/W] H,W 11111111 11111111		TCDT4[R/W] H,W 00000000 00000000		Free-run timer 4
001128_H	TCCS4[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00112C_H$	CPCLRB5/CPCLR5[R/W] H,W 11111111 11111111		TCDT5[R/W] H,W 00000000 00000000		Free-run timer 5
001130_H	TCCS5[R/W] B,H,W 00000000 01000000 ----0000 --------				
001134_H	FRS0[R/W] B,H,W -------- -000-000 -000-000 -000-000				Free-run timer selection
001138_H	FRS1[R/W] B,H,W -------- -------- -000-000 -000-000				
$00113C_H$	FRS2[R/W] B,H,W -------- -000-000 -000-000 -000-000				
001140_H	FRS3[R/W] B,H,W -------- -------- -000-000 -000-000				
001144_H	FRS4[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001148_H	FRS5[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
$00114C_H$	FRS6[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001150_H	-				
001154_H	OCCPB0/OCCP0[R/W] H,W 00000000 00000000		OCCPB1/OCCP1[R/W] H,W 00000000 00000000		Output compare 0/1
001158_H	OCS01[R/W] B,H,W -110--00 00001100		-	OCMOD01[R/W] B,H,W ------00	
$00115C_H$	OCCPB2/OCCP2[R/W] H,W 00000000 00000000		OCCPB3/OCCP3[R/W] H,W 00000000 00000000		Output compare 2/3
001160_H	OCS23[R/W] B,H,W -110--00 00001100		-	OCMOD23[R/W] B,H,W ------00	
001164_H	OCCPB4/OCCP4[R/W] H,W 00000000 00000000		OCCPB5/OCCP5[R/W] H,W 00000000 00000000		Output compare 4/5
001168_H	OCS45[R/W] B,H,W -110--00 00001100		-	OCMOD45[R/W] B,H,W ------00	
$00116C_H$	OCCPB6/OCCP6[R/W] H,W 00000000 00000000		OCCPB7/OCCP7[R/W] H,W 00000000 00000000		Output compare 6/7
001170_H	OCS67[R/W] B,H,W -110--00 00001100		-	OCMOD67[R/W] B,H,W ------00	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001174_H	OCCPB8/OCCP8[R/W] H,W 00000000 00000000		OCCPB9/OCCP9[R/W] H,W 00000000 00000000		Output compare 8/9
001178_H	OCS89[R/W] B,H,W -110--00 00001100		-	OCMOD89[R/W] B,H,W ------00	
$00117C_H$	OCCPB10/OCCP10[R/W] H,W 00000000 00000000		OCCPB11/OCCP11[R/W] H,W 00000000 00000000		Output compare 10/11
001180_H	OCS1011[R/W] B,H,W -110--00 00001100		-	OCMOD1011 [R/W] B,H,W ------00	
001184_H	IPCP0[R] H,W 00000000 00000000		IPCP1[R] H,W 00000000 00000000		Input capture 0/1
001188_H	ICS01[R/W] B,H,W ------00 00000000		-	LSYNS[R/W] B,H,W ---00000	
$00118C_H$	IPCP2[R] H,W 00000000 00000000		IPCP3[R] H,W 00000000 00000000		Input capture 2/3
001190_H	ICS23[R/W] B,H,W ------00 00000000		-	-	
001194_H	IPCP4[R] H,W 00000000 00000000		IPCP5[R] H,W 00000000 00000000		Input capture 4/5
001198_H	ICS45[R/W] B,H,W ------00 00000000		-	-	
$00119C_H$	IPCP6[R] H,W 00000000 00000000		IPCP7[R] H,W 00000000 00000000		Input capture 6/7
$0011A0_H$	ICS67[R/W] B,H,W ------00 00000000		-	-	
$0011A4_H$	DTSR[R/W] B,H,W ------10	-	-	-	DTTI selection
$0011A8_H$	TMRR0[R/W] H,W 00000000 00000001		TMRR1[R/W] H,W 00000000 00000001		Waveform generator 0/1/2
$0011AC_H$	TMRR2[R/W] H,W 00000000 00000001		-	-	
$0011B0_H$	DTSCR0[R/W] B,H,W 00000000	DTSCR1[R/W] B,H,W 00000000	DTSCR2[R/W] B,H,W 00000000	-	
$0011B4_H$	-	DTIR0[R/W] B,H,W 000000--	-	DTMNS0[R/W] B,H,W 00---000	
$0011B8_H$	-	SIGCR10[R/W] B,H,W 00000000	-	SIGCR20[R/W] B,H,W 000000-1	
$0011BC_H$	PICS0[R/W] B,H,W 000000-- -------- -------- --------				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D190_H$	OSID9[R] W -------- -------- 00----00 00000000				FlexRay GTU
$00D194_H$	OSID10[R] W -------- -------- 00----00 00000000				
$00D198_H$	OSID11[R] W -------- -------- 00----00 00000000				
$00D19C_H$	OSID12[R] W -------- -------- 00----00 00000000				
$00D1A0_H$	OSID13[R] W -------- -------- 00----00 00000000				
$00D1A4_H$	OSID14[R] W -------- -------- 00----00 00000000				
$00D1A8_H$	OSID15[R] W -------- -------- 00----00 00000000				
$00D1AC_H$	-				Reserved
$00D1B0_H$	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM
$00D1B4_H$	NMV2[R] W 00000000 00000000 00000000 00000000				
$00D1B8_H$	NMV3[R] W 00000000 00000000 00000000 00000000				
$00D1BC_H$ | $00D2FC_H$	-				Reserved
$00D300_H$	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD
$00D304_H$	FRF[R/W] W -------1 10000000 ---00000 00000000				
$00D308_H$	FRFM[R/W] W -------- -------- ---00000 000000--				
$00D30C_H$	FCL[R/W] W -------- -------- -------- 10000000				
$00D310_H$	MHDS[R/W] W -0000000 -0000000 -0000000 00000000				
$00D314_H$	LDTS[R] W -----000 00000000 -----000 00000000				
$00D318_H$	FSR[R] W -------- -------- 00000000 -----000				
$00D31C_H$	MHDF[R/W] W -------- -------- -------0 00000000				
$00D320_H$	TXRQ1[R] W 00000000 00000000 00000000 00000000				
$00D324_H$	TXRQ2[R] W 00000000 00000000 00000000 00000000				
$00D328_H$	TXRQ3[R] W 00000000 00000000 00000000 00000000				
$00D32C_H$	TXRQ4[R] W 00000000 00000000 00000000 00000000				
$00D330_H$	NDAT1[R] W 00000000 00000000 00000000 00000000				
$00D334_H$	NDAT2[R] W 00000000 00000000 00000000 00000000				
$00D338_H$	NDAT3[R] W 00000000 00000000 00000000 00000000				

- Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

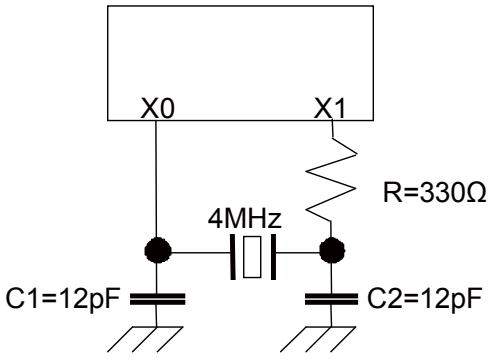


Note: The CPU will be reset at the power supply voltage of the low-voltage detection setting voltage or less.

Oscillation clock frequency vs. Internal operation clock frequency

		Internal operation clock frequency								
		Main clock	PLL clock							
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 20	...	Multiplied by 32
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	80MHz	...	128MHz

- Example of oscillation circuit



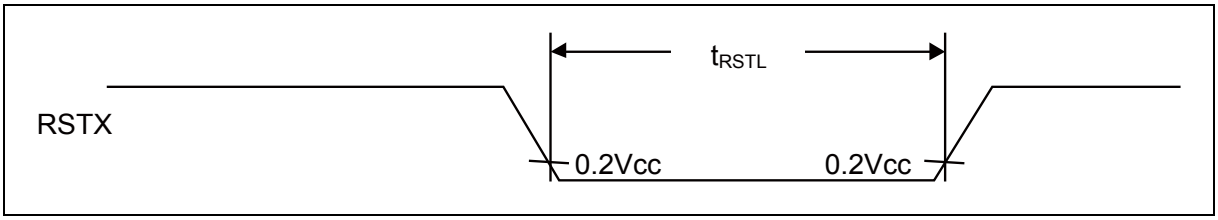
Note: If it is impossible to start the oscillation within or equal to 20ms when starting from the oscillation stop state, the clock supervisor performs a detection of oscillation stop and moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20ms.
In addition, when configuring the oscillator circuit, it is recommended to ask matching evaluation of the circuit to oscillator manufacturers for the design.

(2) Reset input

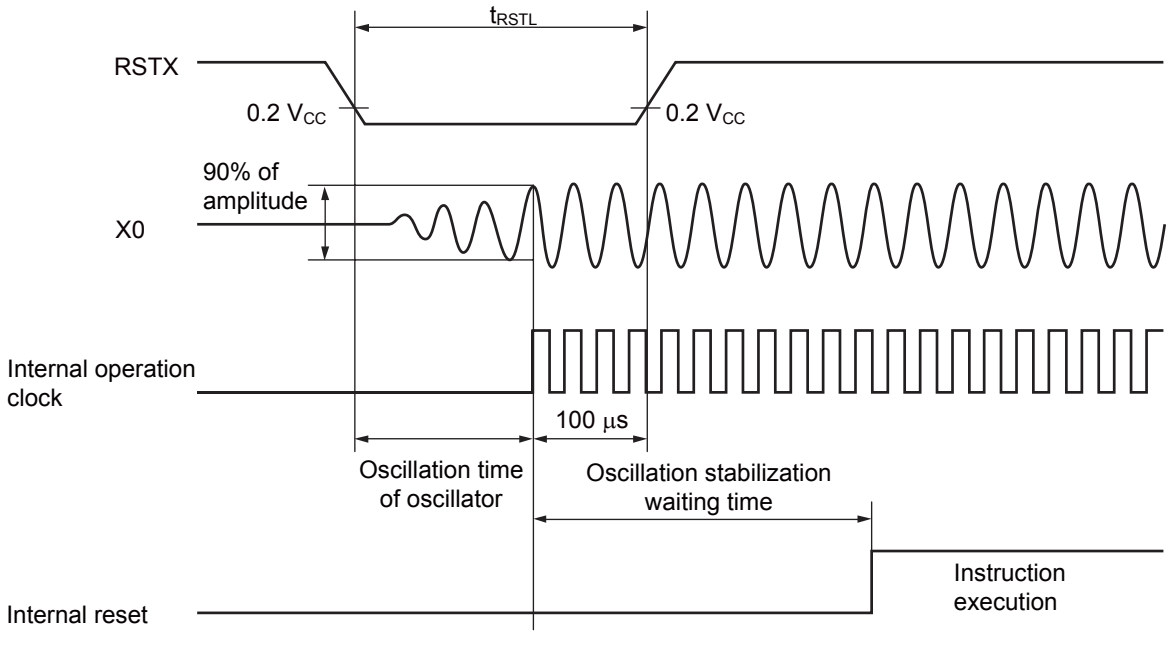
(T_A: Recommended operating conditions, Vcc =5.0V±10%, Vss=AVss=0.0V)

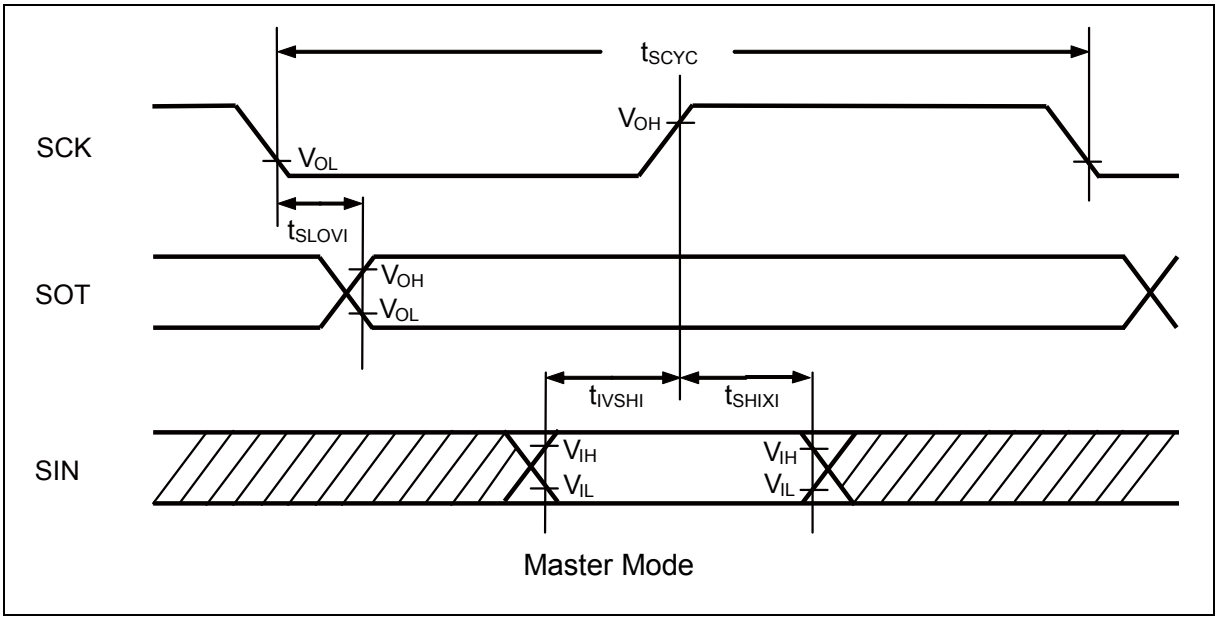
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	-	10	-	µs	During normal operation
				Oscillation time of oscillator * +0.1	-	ms	At Stop mode
				100	-	µs	At Clock mode
Width for reset input removal				1	-	µs	

*: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

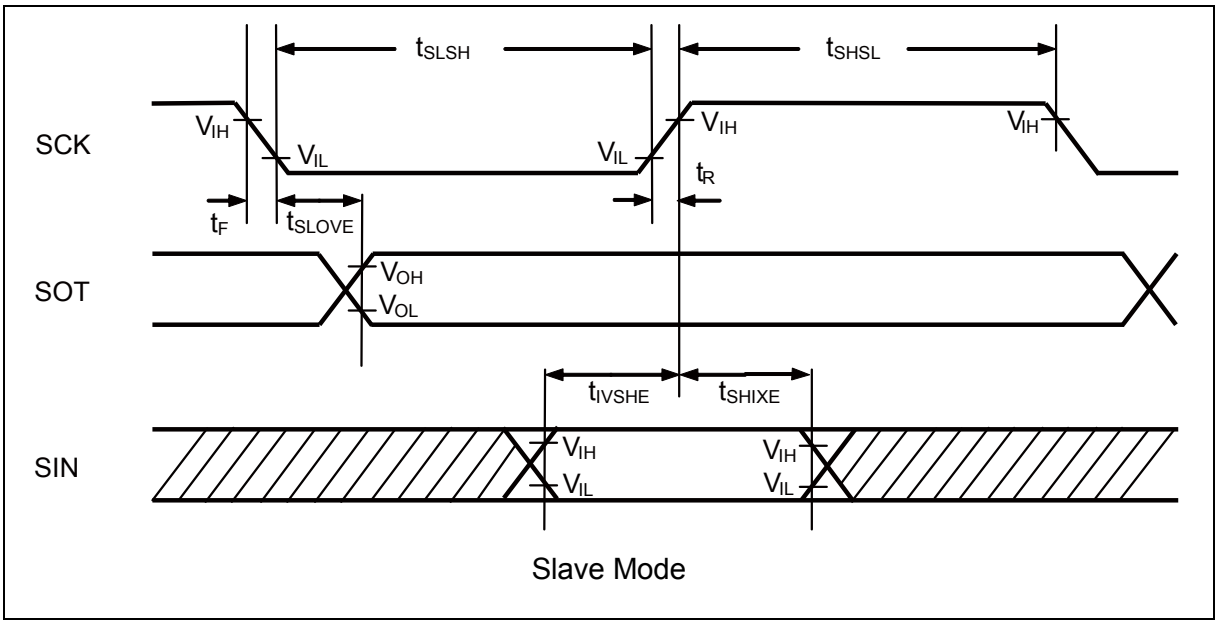


- In Stop mode

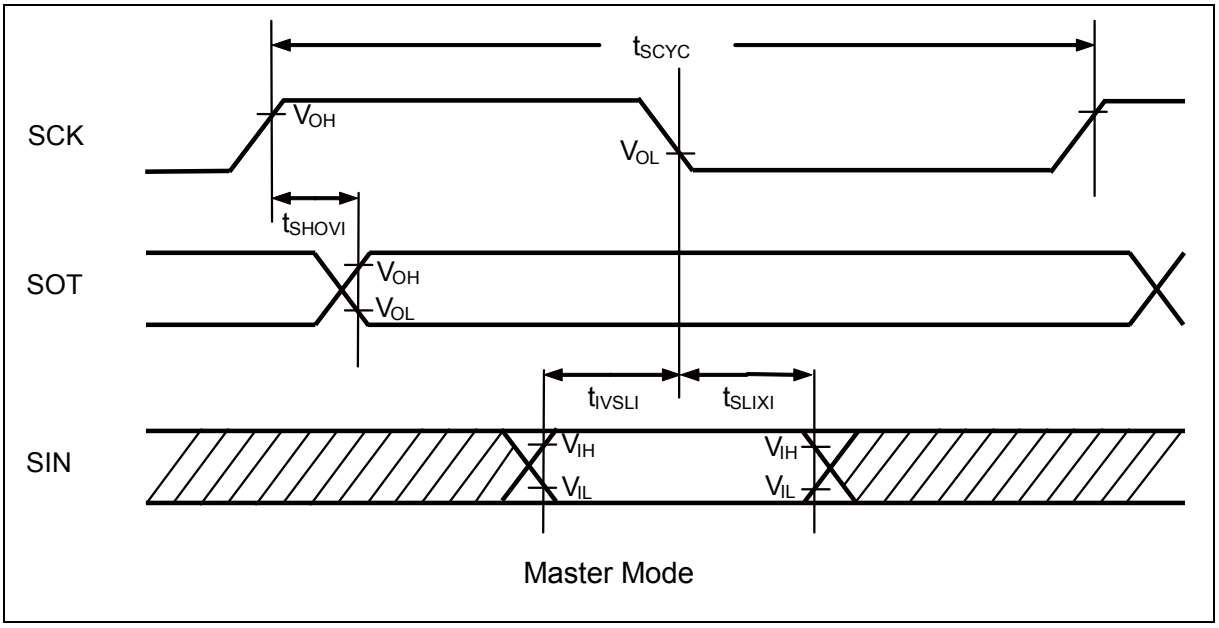




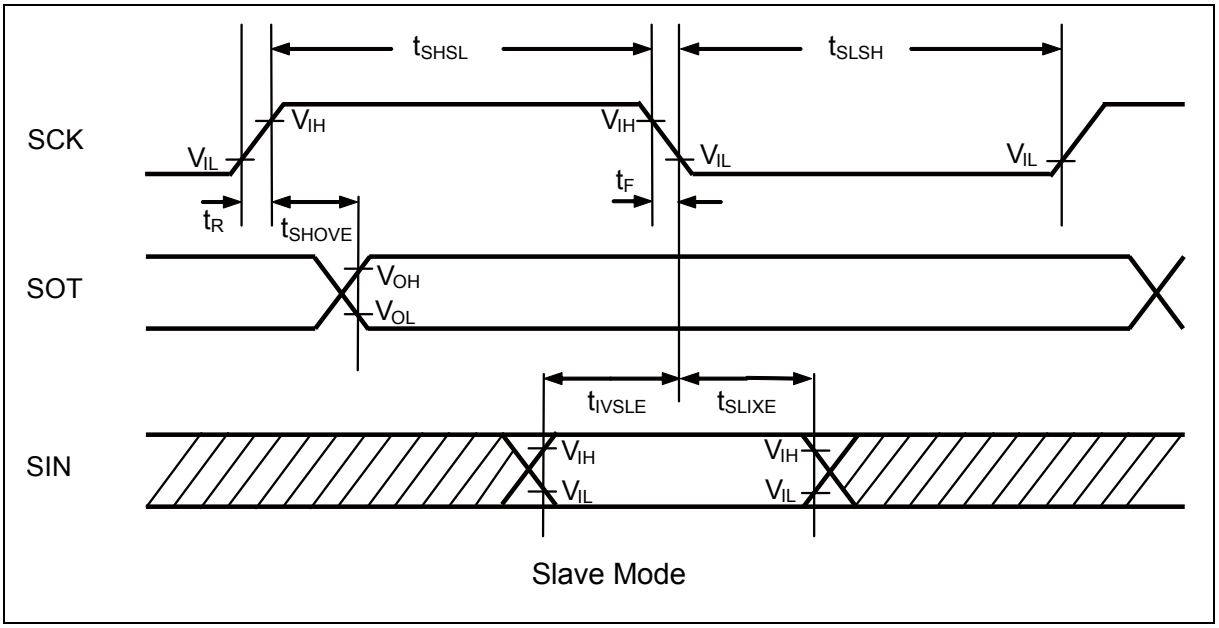
Master Mode



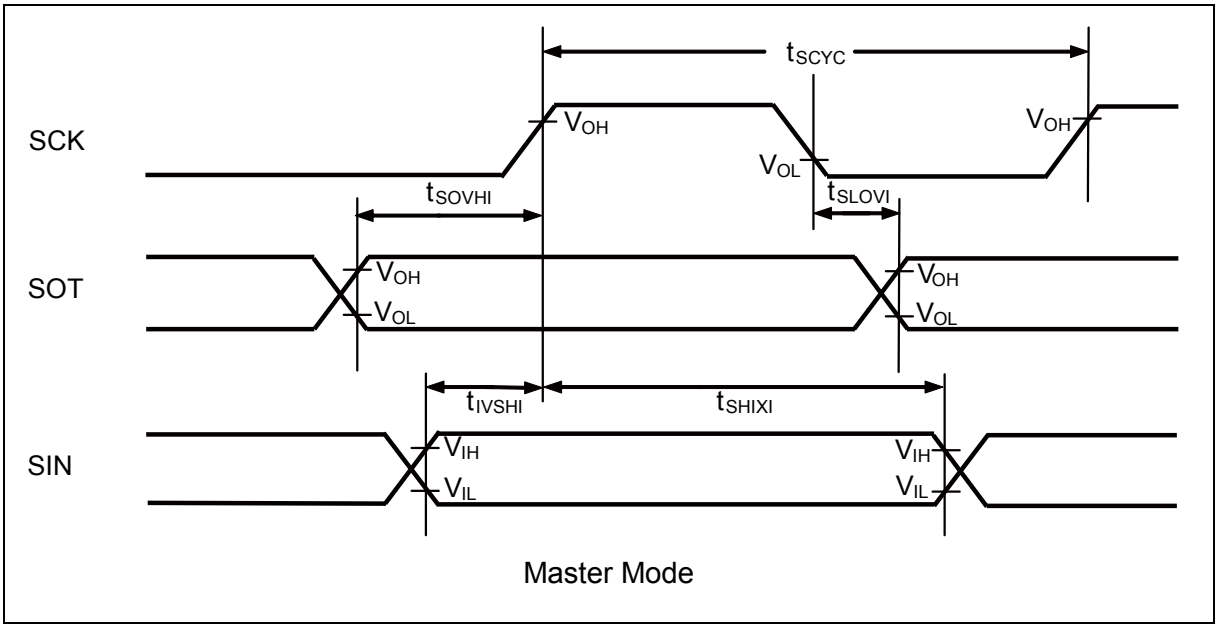
Slave Mode



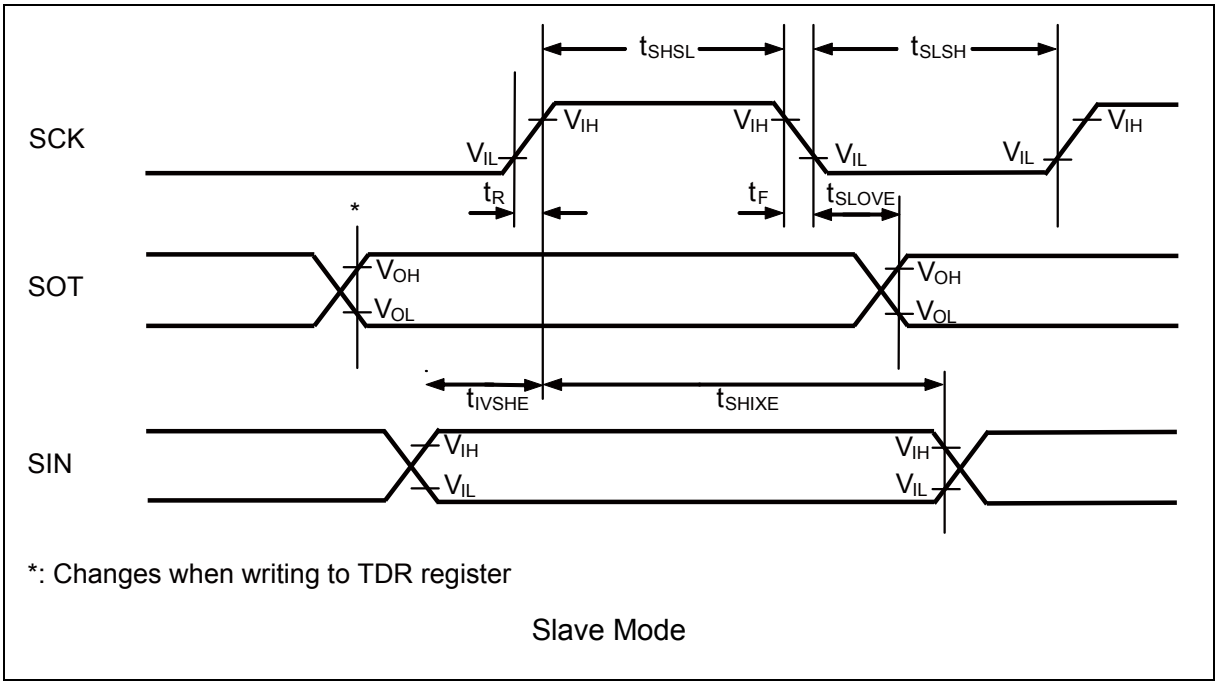
Master Mode



Slave Mode



Master Mode



*: Changes when writing to TDR register

Slave Mode

(4-1-8) When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "L"(SMR,SCSFR:SCINV=1)
- Serial chip select inactive level "L"(SCSCR,SCSFR:CSLVL=0)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ ⇒ SCK ↑ setup time	t_{CSSI}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode C_L=50pF	t_{CSSU} *1+0	t_{CSSU} *1+50	ns	
SCK ↓ ⇒ SCS ↓ hold time	t_{CSHI}			t_{CSHD} *2-50	t_{CSHD} *2+0	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1		-50+5t_{CPP} +t_{CSDS} *3	+50+5t_{CPP} +t_{CSDS} *3	ns	
SCS ↑ ⇒ SCK ↑ setup time	t_{CSSE}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↓ ⇒ SCS ↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1		3t_{CPP}+30	-	ns	
SCS ↑ ⇒ SOT delay time	t_{DSE}	SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	40	ns	
SCS ↓ ⇒ SOT delay time	t_{DEE}			0	-	ns	
SCK ↑ ⇒ SCS ↑ clock switch time	t_{SCC}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode round operation C_L=50pF	3t_{CPP}+0	3t_{CPP}+50	ns	

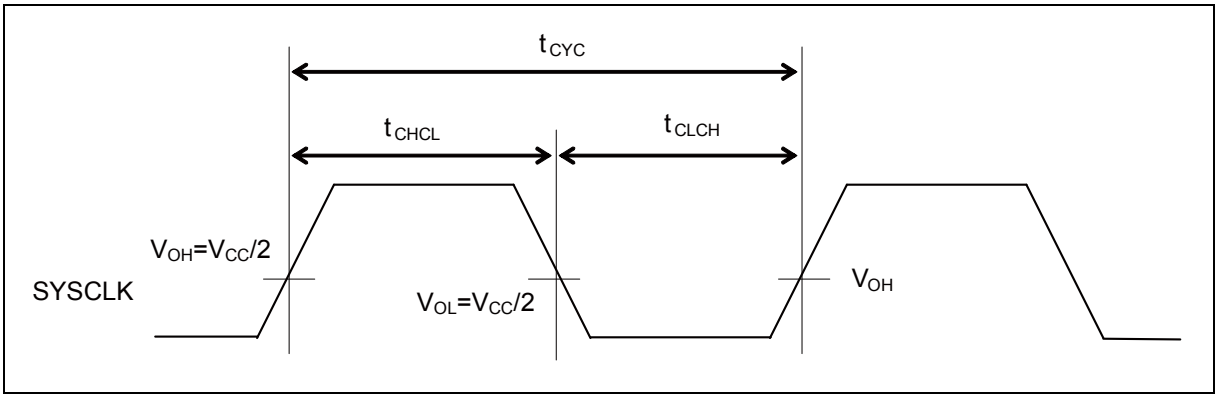
*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock
*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.

(10) Clock output timing

(T_A: Recommended operating conditions, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK	-	t_{CPT}	-	ns	
SYSCLK ↑ → SYSCLK ↓	t_{CHCL}	SYSCLK		(1/2 t_{CYC})- 7	(1/2 t_{CYC})+ 7	ns	
SYSCLK ↓ → SYSCLK ↑	t_{CLCH}	SYSCLK		(1/2 t_{CYC})- 7	(1/2 t_{CYC})+ 7	ns	



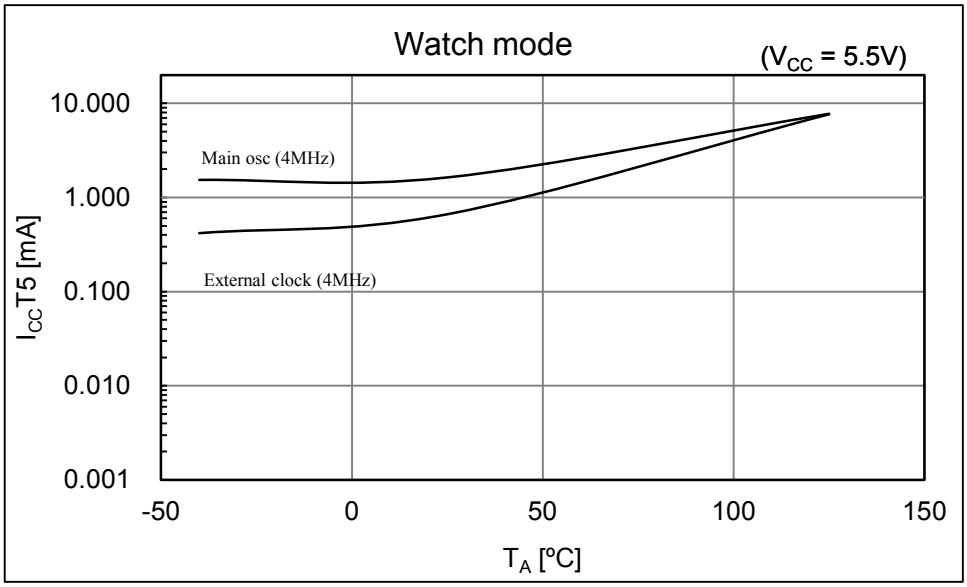
(12) External bus I/F (Asynchronous mode) timing

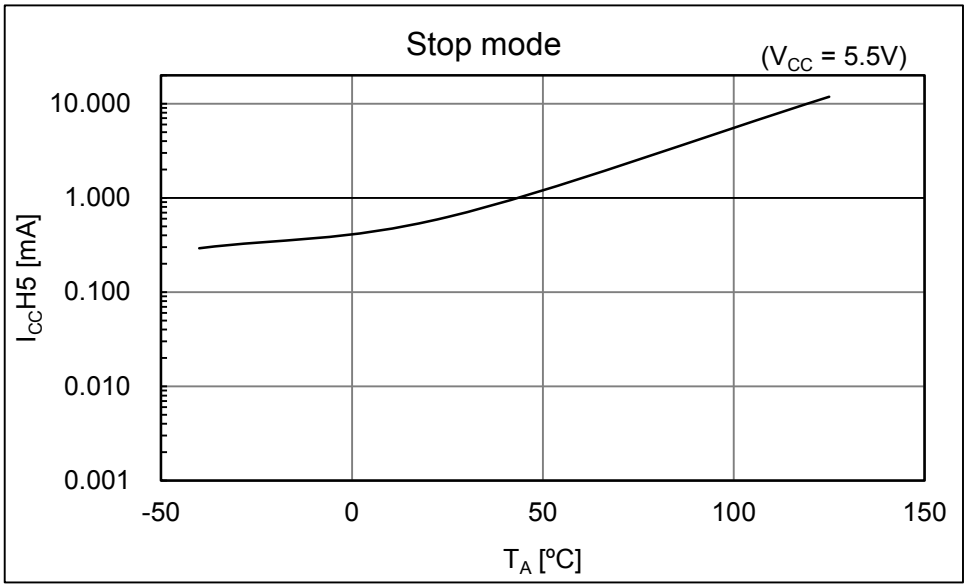
(T_A: Recommended operating conditions, V_{CC} = AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)
(External load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	
Address setup → RDX ↑ time	t_{ASRH}	RDX, A00 to A21	$2 \times t_{CYC} - 12$	$2 \times t_{CYC} + 12$	ns	RWT=1, set RWT to 1 or more.*
RDX ↑ → Address hold	t_{RHAH}		$t_{CYC} - 12$	$t_{CYC} + 12$	ns	Set RDCS to 1 or more.
Data setup → RDX ↑ time	t_{DSRH}	RDX, D16 to D31	$18 + t_{CYC}$	-	ns	RWT=1, set RWT to 1 or more.
RDX ↑ → Data hold	t_{RHDH}		0	-	ns	
Address setup → WRnX ↑ time	t_{ASWH}	WR0X to WR1X, A00 to A21	$t_{CYC} - 12$	$t_{CYC} + 12$	ns	WWT=0.*
WRnX ↑ → Address hold	t_{WHAH}		$t_{CYC} - 12$	$t_{CYC} + 12$	ns	Set WRCS to 1 or more.
Data setup → WRnX ↑ time	t_{DSWH}	WR0X to WR1X, D16 to D31	$t_{CYC} - 16$	$t_{CYC} + 16$	ns	WWT=0.*
WRnX ↑ → Data hold	t_{WHDH}		$t_{CYC} - 16$	$t_{CYC} + 16$	ns	Set WRCS to 1 or more.
Address setup → ASX ↑ time	t_{MASASH}	ASX, D16 to D31	$t_{CYC} - 16$	$t_{CYC} + 16$	ns	ASCY=0.
ASX ↑ → Address hold	t_{MASHAH}		$t_{CYC} - 16$	$t_{CYC} + 16$	ns	In multiplex mode, set as follows: • Set CSWR and CSRD to 2 or more. • Set to ADCY>ASCY. To prevent protocol violation, satisfy the following conditions: ADCY + 1 ≤ ACS + CSRD ADCY + 1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR For details, see Hardware Manual.

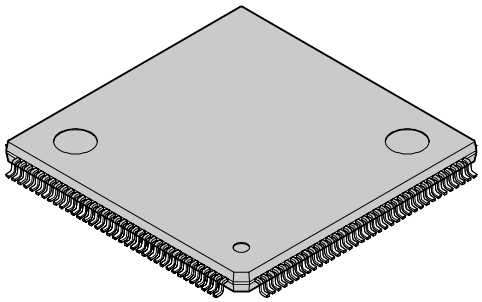
*: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

- MB91F585LA/F586LA/F587LA/F585LB/F586LB/F587LB/ F585LC/F586LC/F587LC/F585LD/F586LD/F587LD



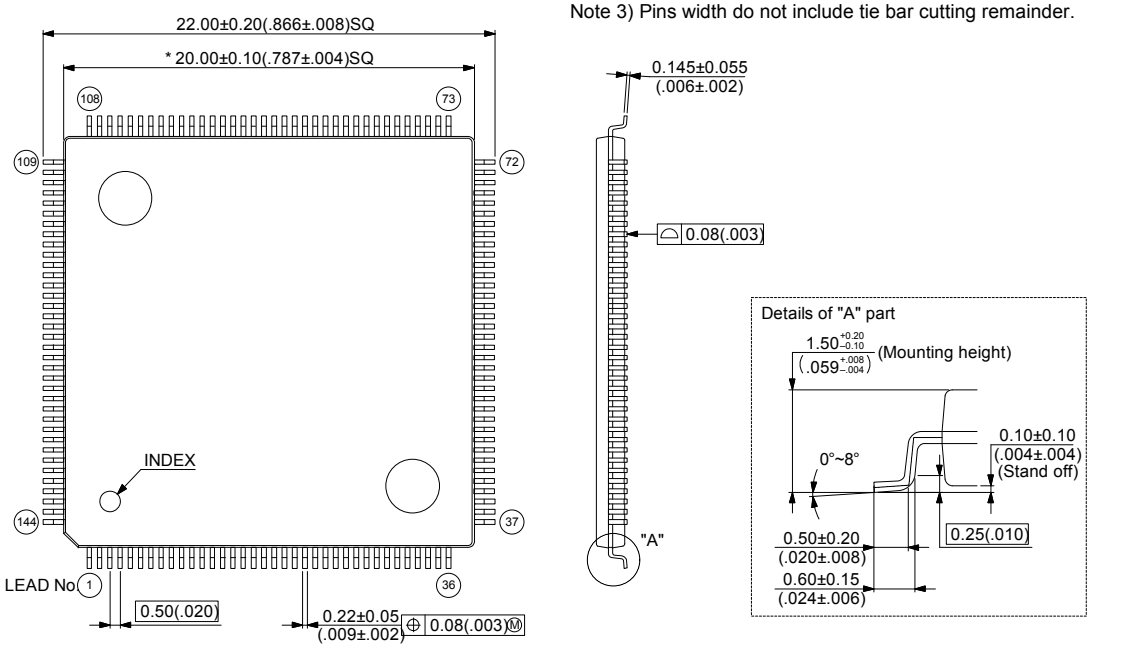


■ PACKAGE DIMENSIONS

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20 g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)

Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/