Infineon Technologies - MB91F585LBPMC-GTK5E1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f585lbpmc-gtk5e1

Notice On Data Sheet Designations

Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion Inc. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion Inc. therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or VIO range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

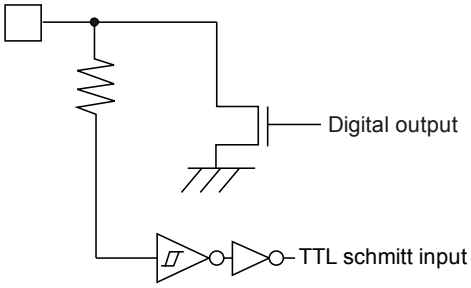
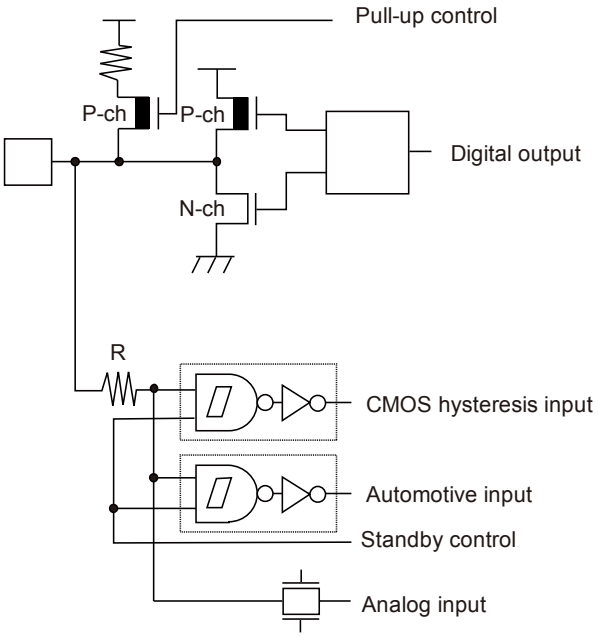
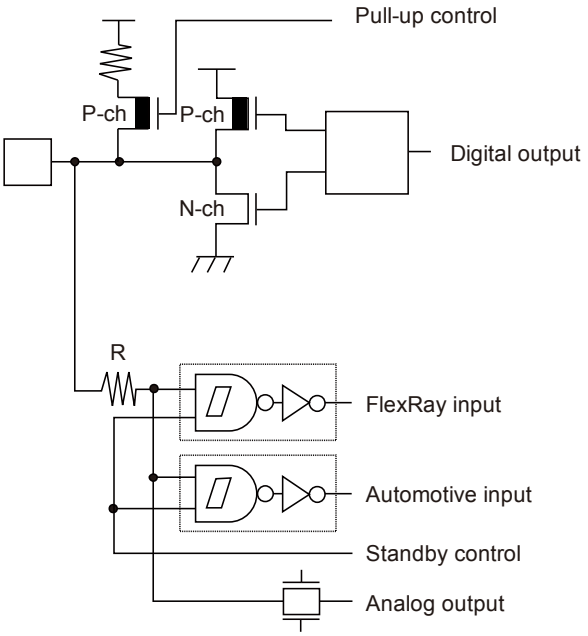
> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local sales office.

Pin No.	Pin name	I/O circuit type*	Function
4	P017	D	General-purpose I/O port
	TRG2		PPG ch.8 to ch.11 external trigger
5	P020	D	General-purpose I/O port
	TRG3		PPG ch.12 to ch.15 external trigger
	SIN3_1		Multi-function serial ch.3 serial data input pin (1)
6	P021	K	General-purpose I/O port
	TRG4		PPG16 to PPG19 external trigger
	SOT3_1		Multi-function serial ch.3 serial data output pin (1)/ I^2C ch.3 serial data I/O pin (1) (SDA)
7	P022	K	General-purpose I/O port
	TRG5		PPG ch.20 to ch.23 external trigger
	SCK3_1		Multi-function serial ch.3 clock I/O pin (1)/ I^2C ch.3 clock I/O pin (1) (SCL)
8	P023	D	General-purpose I/O port
	TIN0		Reload timer ch.0 event input pin
	SCS3_1		Multi-function serial ch.3 serial chip select I/O pin (1)
9	P024	D	General-purpose I/O port
	TIN1		Reload timer ch.1 event input pin
	SIN4_1		Multi-function serial ch.4 serial data input pin (1)
10	P025	K	General-purpose I/O port
	TIN2		Reload timer ch.2 event input pin
	SOT4_1		Multi-function serial ch.4 serial data output pin (1)/ I^2C ch.4 serial data I/O pin (1) (SDA)
11	P026	K	General-purpose I/O port
	TIN3		Reload timer ch.3 event input pin
	SCK4_1		Multi-function serial ch.4 clock I/O pin (1)/ I^2C ch.4 clock I/O pin (1) (SCL)
12	P027	D	General-purpose I/O port
	TOT0		Reload timer ch.0 output pin
	SCS40_1		Multi-function serial ch.4 serial chip select 0 I/O pin (1)
13	P030	D	General-purpose I/O port
	TOT1		Reload timer ch.1 output pin
	SCS41_1		Multi-function serial ch.4 serial chip select 1 output pin (1)
14	P031	D	General-purpose I/O port
	TOT2		Reload timer ch.2 output pin
	SCS42_1		Multi-function serial ch.4 serial chip select 2 output pin (1)
15	P032	D	General-purpose I/O port
	TOT3		Reload timer ch.3 output pin
	SCS43_1		Multi-function serial ch.4 serial chip select 3 output pin (1)
16	P033	D	General-purpose I/O port
17	P034	D	General-purpose I/O port
20	P035	D	General-purpose I/O port
	AIN0		Up/ down counter ch.0 AIN input pin
	RDC_U		RDC phase U output pin
21	P036	D	General-purpose I/O port
	BIN0		Up/ down counter ch.0 BIN input pin
	RDC_V		RDC phase V output pin

• MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD

Pin No.	Pin name	I/O circuit type*1	Function
118	X0	A	Main clock oscillation input pin
119	X1		Main clock oscillation output pin
95	NMIX	B	Interrupt input pin without mask
123	RSTX	B	External reset input pin
116	MD0	C	Mode pin 0 (with high-voltage control)
117	MD1	C	Mode pin 1 (with high-voltage control)
131	P000	E	General-purpose I/O port
	D16		External bus data bit16 I/O pin
	INT2		INT2 external interrupt input pin
	SIN1		Multi-function serial ch.1 serial data input pin
132	P001	K	General-purpose I/O port
	D17		External bus data bit17 I/O pin
	SOT1		Multi-function serial ch.1 serial data output pin/ I^2C ch.1 serial data I/O pin (SDA)
133	P002	K	General-purpose I/O port
	D18		External bus data bit18 I/O pin
	SCK1		Multi-function serial ch.1 clock I/O pin / I^2C ch.1 clock I/O pin (SCL)
134	P003	O	General-purpose I/O port
	D19		External bus data bit19 I/O pin
	TXENA		FlexRay ch.A operation enable output pin
	INT3		INT3 external interrupt input pin
	SIN2		Multi-function serial ch.2 serial data input pin
135	P004	N	General-purpose I/O port
	D20		External bus data bit20 I/O pin
	TXDA		FlexRay ch.A data output pin
	SOT2		Multi-function serial ch.2 serial data output pin
136	P005	N	General-purpose I/O port
	D21		External bus data bit21 I/O pin
	RXDA		FlexRay ch.A data input pin
	SCK2		Multi-function serial ch.2 clock I/O pin
137	P006	N	General-purpose I/O port
	D22		External bus data bit22 I/O pin
	TXENB		FlexRay ch.B operation enable output pin
	SCS2		Multi-function serial ch.2 serial chip select I/O pin
138	P007	N	General-purpose I/O port
	D23		External bus data bit23 I/O pin
	TXDB		FlexRay ch.B data output pin
139	P010	N	General-purpose I/O port
	D24		External bus data bit24 I/O pin
	RXDB		FlexRay ch.B data input pin
140	P011	D	General-purpose I/O port
	D25		External bus data bit25 I/O pin
	TIOA0		Base timer ch.0 TIOA I/O pin

Type	Circuit	Remarks
L		Open drain I/O
M		• With analog input, I^2C, general-purpose I/O port • CMOS level output I_{OH}=-3mA, I_{OL}=3mA (at I^2C output) I_{OH}=-2/-5mA, I_{OL}=2/5mA (other than above) • With 50 kΩ pull-up resistor control • CMOS hysteresis input (0.7Vcc/0.3Vcc) • Automotive input (0.8Vcc/0.5Vcc)
N		• With analog output, general-purpose I/O port • CMOS level output I_{OH}=-2/-4mA, I_{OL}=2/4mA • With 50 kΩ pull-up resistor control • FlexRay input (0.7Vcc/0.3Vcc) • Automotive input (0.8Vcc/0.5Vcc)

- Lead-Free Packaging
  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices
  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, Spansion Inc. packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking
  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

  Condition: 125°C/24 h

- Static Electricity
  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114_H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
$00311C_H$	-				
003120_H	BUSADR3[R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4[R] W 00000000 00000000 00000000 00000000				
003128_H | $003FFC_H$	-	-	-	-	Reserved
004000_H | $005FFC_H$	Backup RAM				Backup RAM area
006000_H | $00CFFC_H$	-	-	-	-	Reserved
$00D000_H$	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF
$00D004_H$	CIF1[R/W] W 00000000 -------0 -0000000 --------				
$00D008_H$ | $00D00C_H$	-	-	-	-	Reserved
$00D010_H$	-				FlexRay GIF
$00D014_H$	-				
$00D018_H$	-	-	-	-	
$00D01C_H$	LCK[R/W] W -------- -------- -------- 00000000				
$00D020_H$	EIR[R/W] W -----000 -----000 ----0000 00000000				FlexRay INT
$00D024_H$	SIR[R/W] W ------00 ------00 00000000 00000000				
$00D028_H$	EILS[R/W] W -----000 -----000 ----0000 00000000				
$00D02C_H$	SILS[R/W] W ------11 ------11 11111111 11111111				
$00D030_H$	EIES[R/W] W -----000 -----000 ----0000 00000000				
$00D034_H$	EIER[R/W] W -----000 -----000 ----0000 00000000				
$00D038_H$	SIES[R/W] W ------00 ------00 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D600_H$ | $00D6FC_H$	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF
$00D700_H$	RDHS1[R] W --000000 -0000000 -----000 00000000				
$00D704_H$	RDHS2[R] W -0000000 -0000000 -----000 00000000				
$00D708_H$	RDHS3[R] W --000000 --000000 -----000 00000000				
$00D70C_H$	MBS[R] W --000000 --000000 00-00000 00000000				
$00D710_H$	OBCM[R/W] W -------- ------00 -------- ------00				
$00D714_H$	OBCR[R/W] W -------- -0000000 0-----00 -0000000				
$00D718_H$ | $00D7FC_H$	-				Reserved
$00D800_H$ | $00EFFC_H$	-				Reserved
$00F000_H$ | $00FEFC_H$	-				Reserved [S]
$00FF00_H$	DSUCR[R/W] B,H,W -------- -------0		-	-	OCDU [S]
$00FF04_H$ | $00FF0C_H$	-	-	-	-	Reserved [S]
$00FF10_H$	PCSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ | $00FFF4_H$	-	-	-	-	Reserved [S]
$00FFF8_H$	EDIR1[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated when reading and writing to these registers in the user mode.

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0002E0_H$	-	GATEC0[R/W] B,H,W ------00	-	GATEC2[R/W] B,H,W ------00	PPG GATE Control
$0002E4_H$	-	GATEC4[R/W] B,H,W ------00	-	GATEC8[R/W] B,H,W ------00	
$0002E8_H$	-	GATEC10[R/W] B,H,W ------00	-	GATEC12[R/W] B,H,W ------00	
$0002EC_H$	-	-	-	-	Reserved
$0002F0_H$	RCRH0[W] H,W 00000000	RCRL0[W] B,H,W 00000000	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	U/D counter 0
$0002F4_H$	CCR0[R/W] B,H 00000000 -0001000		-	CSR0[R] B 00000000	
$0002F8_H$	RCRH1[W] H,W 00000000	RCRL1[W] B,H,W 00000000	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	U/D counter 1
$0002FC_H$	CCR1[R/W] B,H 00000000 -0001000		-	CSR1[R] B 00000000	
000300_H	-				Reserved
000304_H	-	-	-	-	Reserved
000308_H	-				Reserved
$00030C_H$	-	-	-	-	
000310_H	-	-	MPUCR[R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	-	-	-	-	
000318_H	-				
$00031C_H$	-	-	-		
000320_H	DPVAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	-	-	DPVSR[R/W] H -------- 00000--0		
000328_H	DEAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	-	-	DESR[R/W] H -------- 00000--0		
000330_H	PABR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	-	-	PACR0[R/W] H 000000-0 00000--0		
000338_H	PABR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	-	-	PACR1[R/W] H 000000-0 00000--0		
000340_H	PABR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	-	-	PACR2[R/W] H 000000-0 00000--0		
000348_H	PABR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	-	-	PACR3[R/W] H 000000-0 00000--0		
000350_H	PABR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000354_H	-	-	PACR4[R/W] H 000000-0 00000--0		MPU [S] (Only the CPU can access this area)
000358_H	PABR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	-	-	PACR5[R/W] H 000000-0 00000--0		
000360_H	PABR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	-	-	PACR6[R/W] H 000000-0 00000--0		
000368_H	PABR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	-	-	PACR7[R/W] H 000000-0 00000--0		
000370_H	-				Reserved [S]
000374_H	-	-	-		
000378_H	-				
$00037C_H$	-	-	-		
000380_H	-				
000384_H	-	-	-		
000388_H	-				
$00038C_H$	-	-	-		
000390_H	-				
000394_H	-	-	-		Reserved [S]
000398_H	-				
$00039C_H$	-	-	-		
$0003A0_H$	-				
$0003A4_H$	-	-	-		
$0003A8_H$	-				
$0003AC_H$	-	-	-		
$0003B0_H$ | $0003FC_H$	-	-	-	-	Reserved [S]
000400_H	ICSEL0[R/W] B,H,W -----000	ICSEL1[R/W] B,H,W -------0	ICSEL2[R/W] B,H,W -------0	ICSEL3[R/W] B,H,W -------0	Generation and clearing of DMA transfer requests
000404_H	ICSEL4[R/W] B,H,W -------0	ICSEL5[R/W] B,H,W -------0	ICSEL6[R/W] B,H,W -------0	ICSEL7[R/W] B,H,W -----000	
000408_H	ICSEL8[R/W] B,H,W -------0	ICSEL9[R/W] B,H,W -------0	ICSEL10[R/W] B,H,W -----000	ICSEL11[R/W] B,H,W -----000	
$00040C_H$	ICSEL12[R/W] B,H,W -----000	ICSEL13[R/W] B,H,W -----000	ICSEL14[R/W] B,H,W -----000	ICSEL15[R/W] B,H,W -------0	
000410_H	ICSEL16[R/W] B,H,W -------0	ICSEL17[R/W] B,H,W -------0	ICSEL18[R/W] B,H,W -------0	ICSEL19[R/W] B,H,W -------0	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000588_H | $00058C_H$	-	-	-	-	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H	ASR0[R/W] W 00000000 00000000 -------- 1111-001				External bus interface [S]
000604_H	ASR1[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608_H	ASR2[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
$00060C_H$	ASR3[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000610_H | $00063C_H$	-	-	-	-	Reserved[S]
000640_H	ACR0[R/W] W -------- -------- -------- 00--00--				External bus interface [S]
000644_H	ACR1[R/W] W -------- -------- -------- XX--XX--				
000648_H	ACR2[R/W] W -------- -------- -------- XX--XX--				
$00064C_H$	ACR3[R/W] W -------- -------- -------- XX--XX--				
000650_H | $00067C_H$	-	-	-	-	Reserved[S]
000680_H	AWR0[R/W] W ----1111 00000000 11110000 00000-0-				External bus interface [S]
000684_H	AWR1[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688_H	AWR2[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
$00068C_H$	AWR3[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690_H | $0006BC_H$	-	-	-	-	Reserved[S]
$0006C0_H$	DMAR0[R/W] W -------- -------- -------- ----0000				External bus interface [S]
$0006C4_H$	DMAR1[R/W] W -------- -------- -------- ----0000				
$0006C8_H$	DMAR2[R/W] W -------- -------- -------- ----0000				
$0006CC_H$	DMAR3[R/W] W -------- -------- -------- ----0000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0021B4_H$	MSGVAL41[R] B,H,W 00000000 00000000		MSGVAL31[R] B,H,W 00000000 00000000		CAN 1 64msb
$0021B8_H$	-		-		
$0021BC_H$	-		-		
$0021C0_H$ | $0021FC_H$	-		-		
002200_H	CTRLR2[R/W] B,H,W -------- 000-0001		STATR2[R/W] B,H,W -------- 00000000		CAN 2 64msb
002204_H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2[R/W] B,H,W -0100011 00000001		
002208_H	INTR2[R] B,H,W 00000000 00000000		TESTR2[R/W] B,H,W -------- X00000--		
$00220C_H$	BRPER2[R/W] B,H,W -------- ----0000		-		
002210_H	IF1CREQ2[R/W] B,H,W 0------- 00000001		IF1CMSK2[R/W] B,H,W -------- 00000000		
002214_H	IF1MSK22[R/W] B,H,W 11-11111 11111111		IF1MSK12[R/W] B,H,W 11111111 11111111		
002218_H	IF1ARB22[R/W] B,H,W 00000000 00000000		IF1ARB12[R/W] B,H,W 00000000 00000000		
$00221C_H$	IF1MCTR2[R/W] B,H,W 00000000 0---0000		-		
002220_H	IF1DTA12[R/W] B,H,W 00000000 00000000		IF1DTA22[R/W] B,H,W 00000000 00000000		
002224_H	IF1DTB12[R/W] B,H,W 00000000 00000000		IF1DTB22[R/W] B,H,W 00000000 00000000		
002228_H, $00222C_H$	-		-		
002230_H, 002234_H	Reserved (IF1 data mirror)				
002238_H, $00223C_H$	-		-		
002240_H	IF2CREQ2[R/W] B,H,W 0------- 00000001		IF2CMSK2[R/W] B,H,W -------- 00000000		
002244_H	IF2MSK22[R/W] B,H,W 11-11111 11111111		IF2MSK12[R/W] B,H,W 11111111 11111111		
002248_H	IF2ARB22[R/W] B,H,W 00000000 00000000		IF2ARB12[R/W] B,H,W 00000000 00000000		
$00224C_H$	IF2MCTR2[R/W] B,H,W 00000000 0---0000		-		
002250_H	IF2DTA12[R/W] B,H,W 00000000 00000000		IF2DTA22[R/W] B,H,W 00000000 00000000		
002254_H	IF2DTB12[R/W] B,H,W 00000000 00000000		IF2DTB22[R/W] B,H,W 00000000 00000000		
002258_H, $00225C_H$	-		-		
002260_H, 002264_H	Reserved (IF2 data mirror)				
002268_H | $00227C_H$	-		-		
002280_H	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		

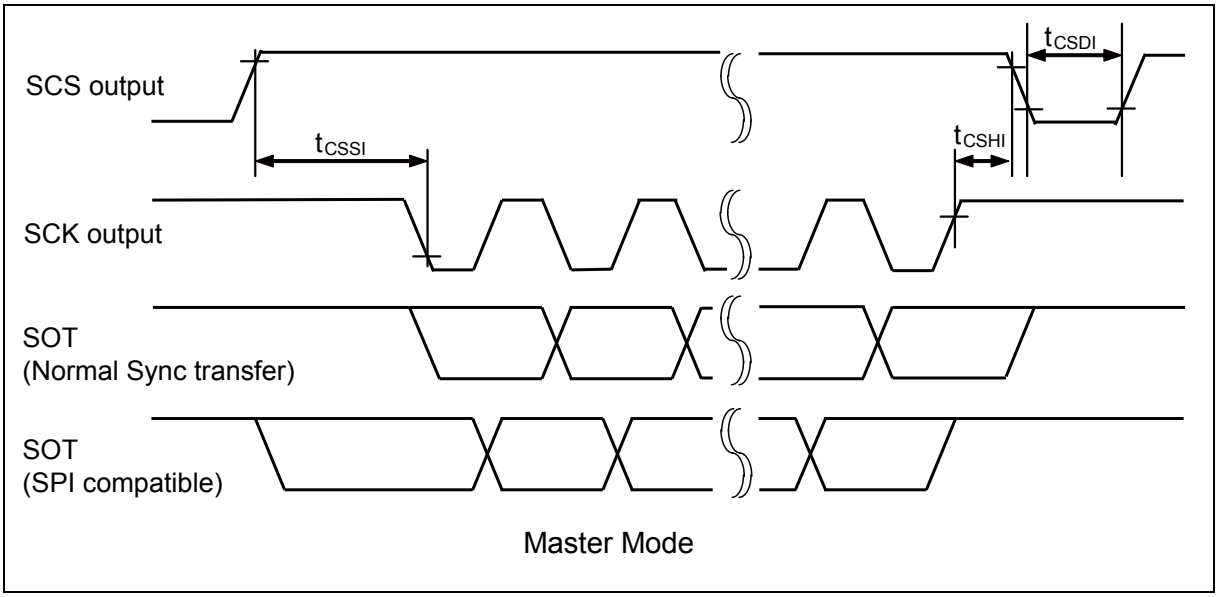
Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D120_H$	SFS[R] W -------- ----0000 00000000 00000000				FlexRay GTU
$00D124_H$	SWNIT[R] W -------- -------- ----0000 00000000				
$00D128_H$	ACS[R/W] W -------- -------- ---00000 ---00000				
$00D12C_H$	-				
$00D130_H$	ESID1[R] W -------- -------- 00----00 00000000				
$00D134_H$	ESID2[R] W -------- -------- 00----00 00000000				
$00D138_H$	ESID3[R] W -------- -------- 00----00 00000000				
$00D13C_H$	ESID4[R] W -------- -------- 00----00 00000000				
$00D140_H$	ESID5[R] W -------- -------- 00----00 00000000				
$00D144_H$	ESID6[R] W -------- -------- 00----00 00000000				
$00D148_H$	ESID7[R] W -------- -------- 00----00 00000000				
$00D14C_H$	ESID8[R] W -------- -------- 00----00 00000000				
$00D150_H$	ESID9[R] W -------- -------- 00----00 00000000				
$00D154_H$	ESID10[R] W -------- -------- 00----00 00000000				
$00D158_H$	ESID11[R] W -------- -------- 00----00 00000000				
$00D15C_H$	ESID12[R] W -------- -------- 00----00 00000000				
$00D160_H$	ESID13[R] W -------- -------- 00----00 00000000				
$00D164_H$	ESID14[R] W -------- -------- 00----00 00000000				
$00D168_H$	ESID15[R] W -------- -------- 00----00 00000000				
$00D16C_H$	-				
$00D170_H$	OSID1[R] W -------- -------- 00----00 00000000				
$00D174_H$	OSID2[R] W -------- -------- 00----00 00000000				
$00D178_H$	OSID3[R] W -------- -------- 00----00 00000000				
$00D17C_H$	OSID4[R] W -------- -------- 00----00 00000000				
$00D180_H$	OSID5[R] W -------- -------- 00----00 00000000				
$00D184_H$	OSID6[R] W -------- -------- 00----00 00000000				
$00D188_H$	OSID7[R] W -------- -------- 00----00 00000000				
$00D18C_H$	OSID8[R] W -------- -------- 00----00 00000000				

(4-1-4) SPI compatible (SCR:SPI=1) and serial clock output signal detect level "L"(SMR:SCINV=1)

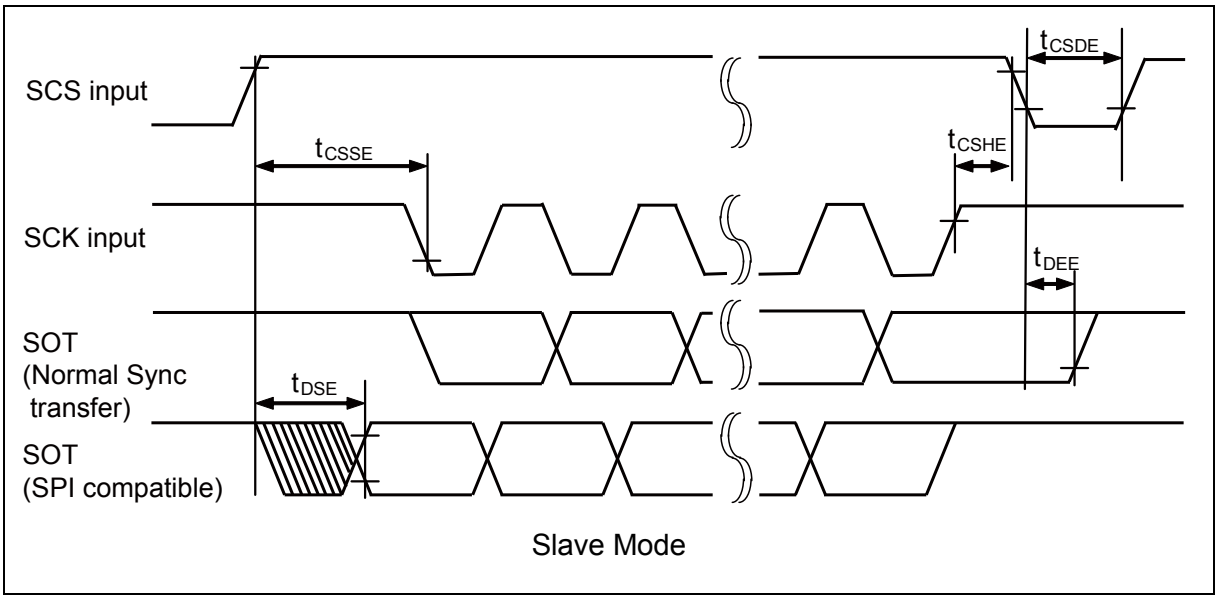
(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK3_1,SCK4_1	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVI}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-30	+30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		30	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXI}			0	-	ns	
SOT ⇒ SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		$2t_{CPP}$-30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVE}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		10	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4, SCK3_1, SCK4_1 SCK0 to SCK4, SCK3_1,SCK4_1		-	5	ns	
SCK rise time	t_R			-	5	ns	

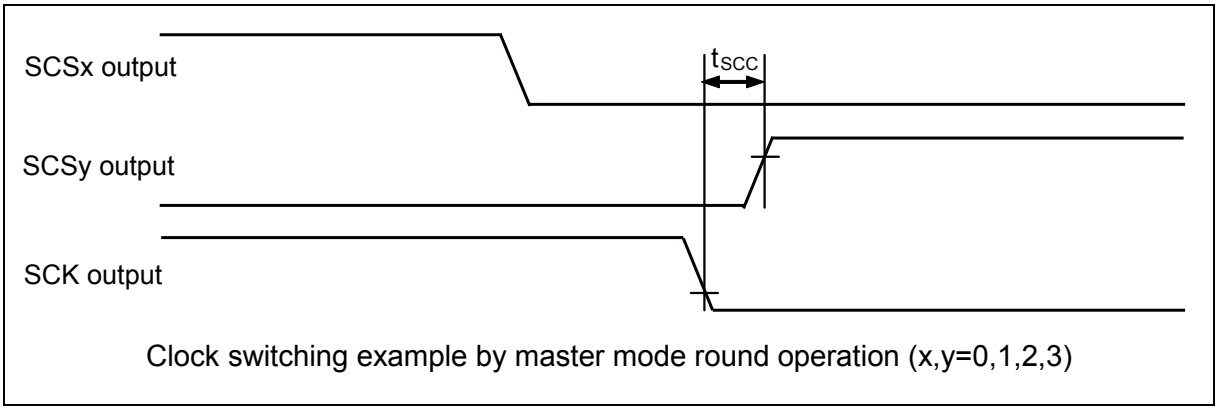
Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



Slave Mode



Clock switching example by master mode round operation (x,y=0,1,2,3)

(4-4) I²C timing (SMR:MD2-0="100"b)

(T_A: Recommended operating conditions, V_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Standard mode		High-speed mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK0,SCK1, SCK3,SCK4, SCK3_1,SCK4_1 (SCL)	C_L=50pF R=(V_P/I_{OL}) *1	0	100	0	400	kHz	
"Repeat START condition" hold time SDA↓ → SCL↓	t_{HDSTA}	SCK0,SCK1, SCK3,SCK4, SCK3_1,SCK4_1 (SCL) SOT0,SOT1, SOT3,SOT4, SOT3_1,SOT4_1 (SDA)		4.0	-	0.6	-	µs	
"L" width for SCL clock	t_{LOW}	SCK0,SCK1, SCK3,SCK4, SCK3_1,SCK4_1 (SCL)		4.7	-	1.3	-	µs	
"H" width for SCL clock	t_{HIGH}			4.0	-	0.6	-	µs	
"Repeat START condition" setup time SCL↑ → SDA↓	t_{SUSTA}	SCK0,SCK1, SCK3,SCK4, SCK3_1,SCK4_1 (SCL) SOT0,SOT1, SOT3,SOT4, SOT3_1,SOT4_1 (SDA)		4.7	-	0.6	-	µs	
Data hold time SCL↓ → SDA↓↑	t_{HDDAT}			0	3.45 *2	0	0.90 *3	µs	
Data setup time SDA↓↑ → SCL↑	t_{SUDAT}			250	-	100	-	ns	
"STOP condition" setup time SCL↑ → SDA↑	t_{SUSTO}			4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}	-		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-		$2t_{CPP}$ *4	-	$2t_{CPP}$ *4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. V_P shows that the power supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

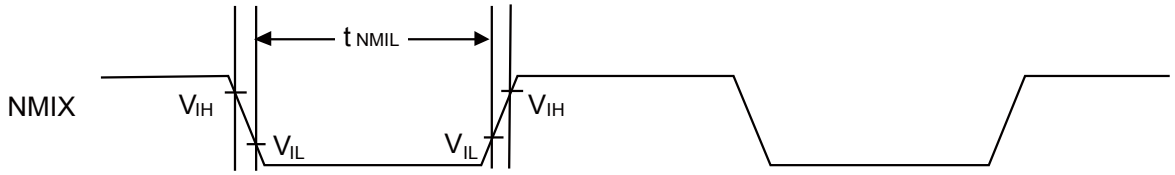
*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the peripheral bus to 8MHz or more when use I²C.

(7) NMI input timing

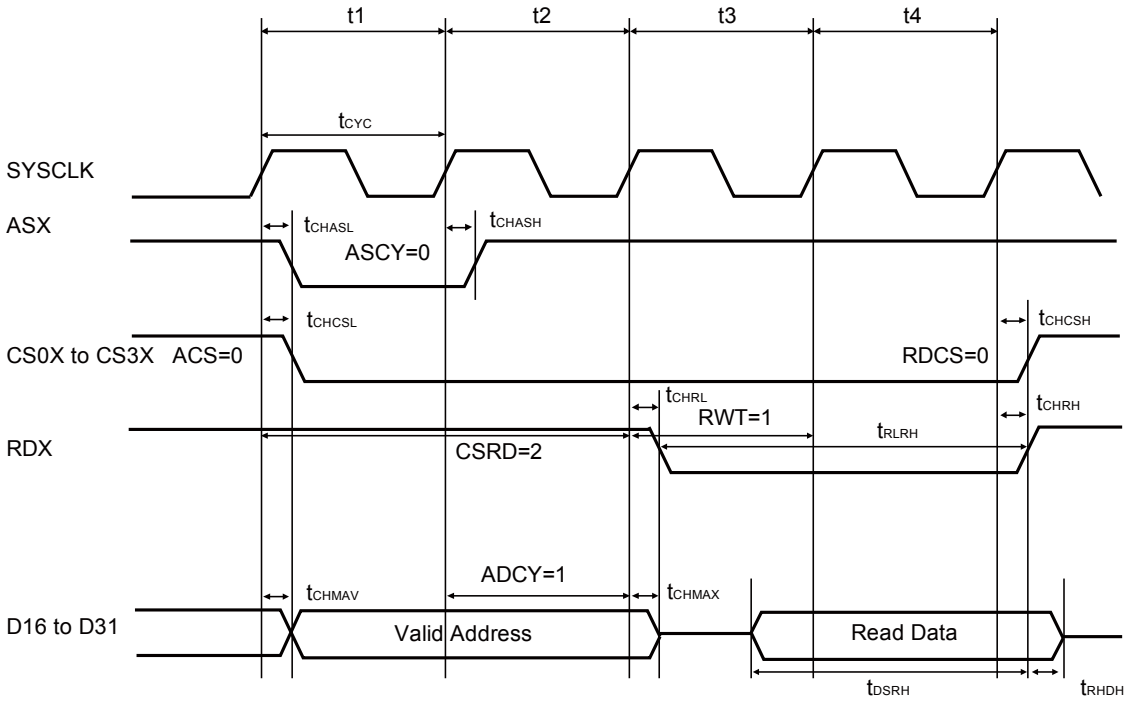
(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	$4t_{CPP}$	-	ns	

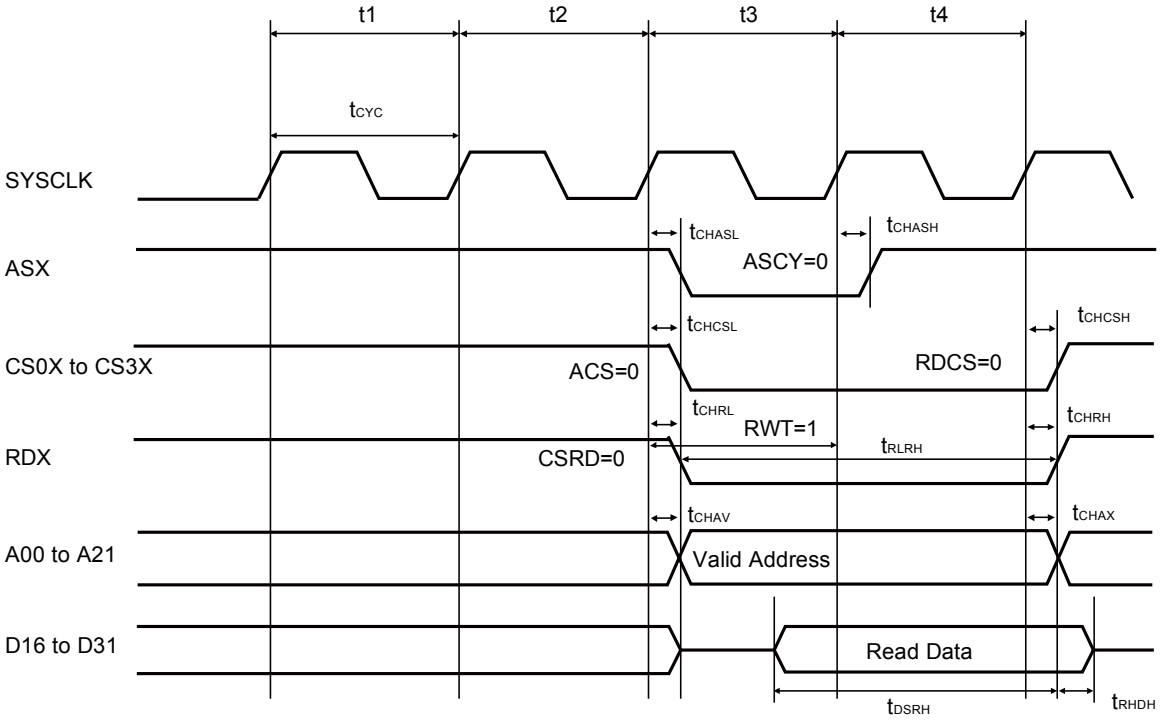
• NMIX input timing



External bus I/F (synchronous mode, read operation, and multiplex mode) timing



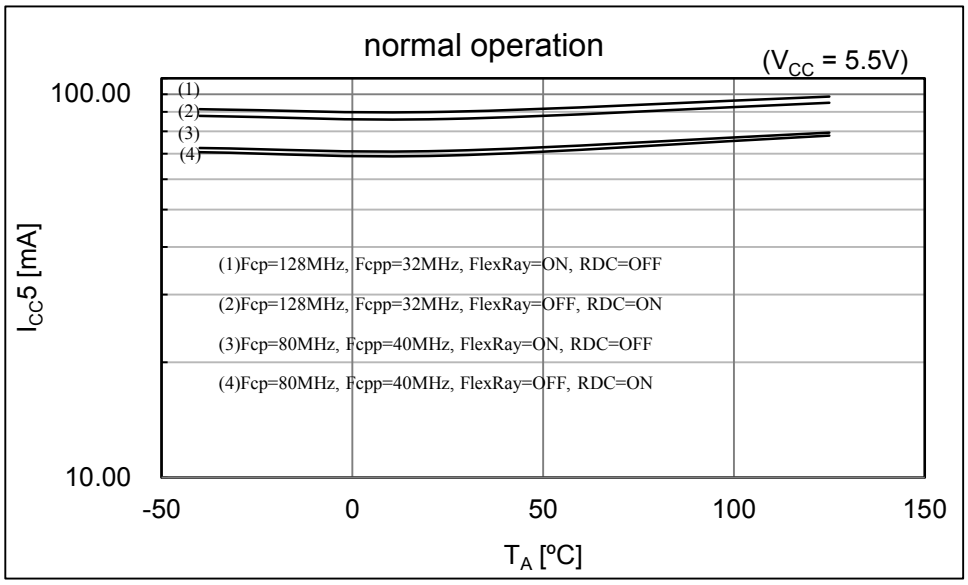
External bus I/F (synchronous mode, read operation, and split mode) timing



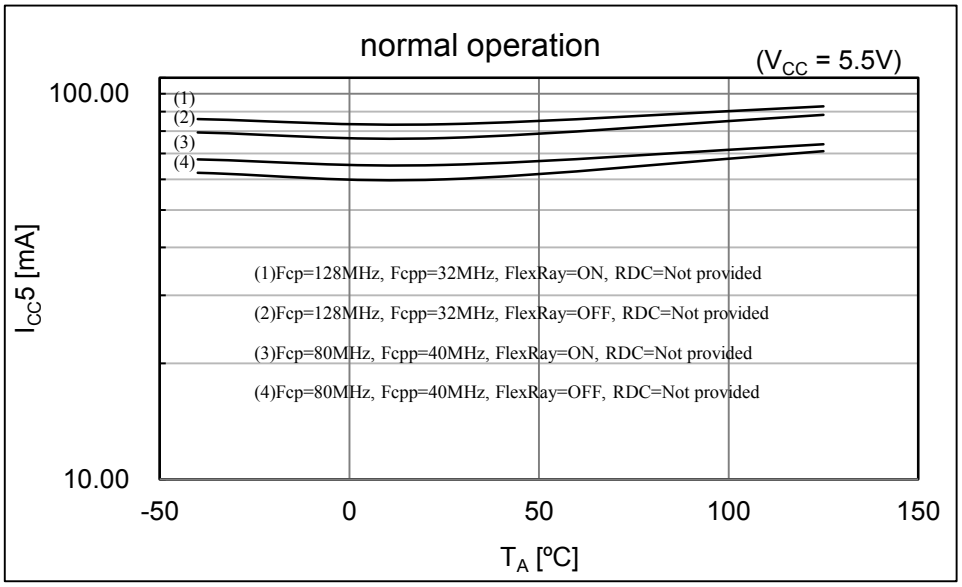
■ EXAMPLE CHARACTERISTICS

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

• MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC



• MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD

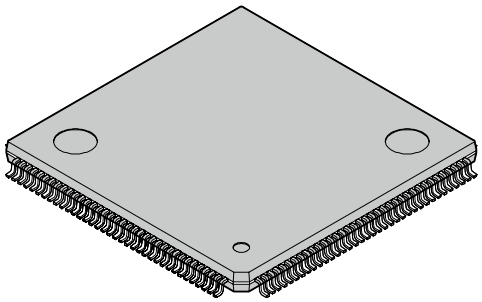


■ ORDERING INFORMATION

Part number	Package*
MB91F585LAPMC-GTE1 MB91F586LAPMC-GTE1 MB91F587LAPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F585LBPMC-GTE1 MB91F586LBPMC-GTE1 MB91F587LBPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F585LCPMC-GTE1 MB91F586LCPMC-GTE1 MB91F587LCPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F585LDPMC-GTE1 MB91F586LDPMC-GTE1 MB91F587LDPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)

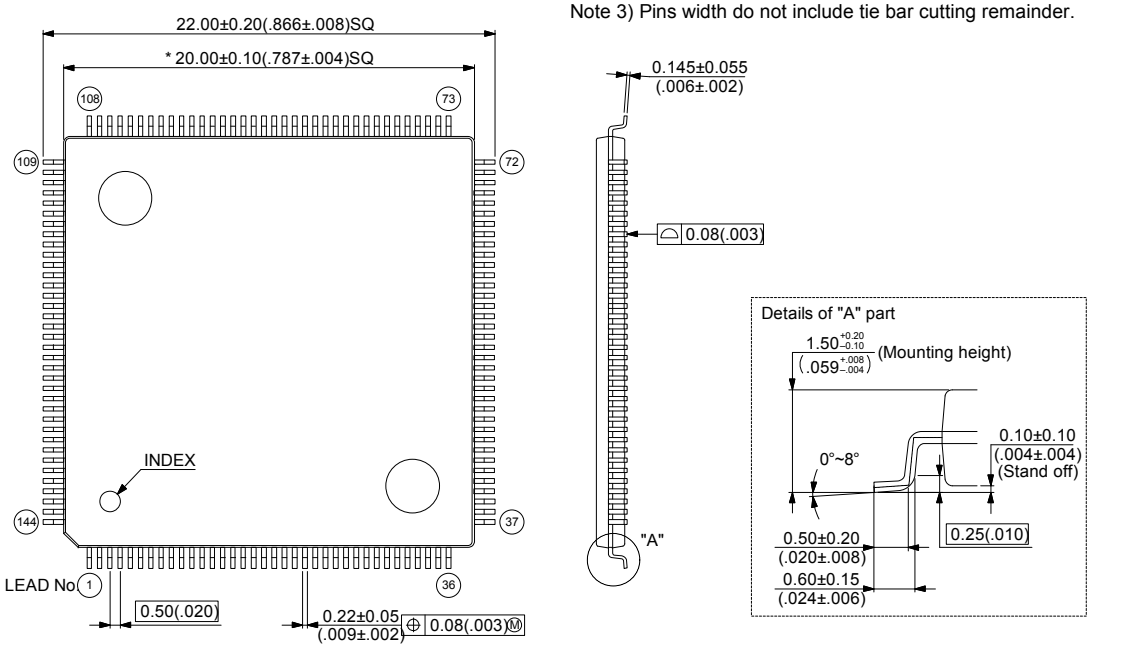
*: For details of the package, see "■ PACKAGE DIMENSIONS ".

■ PACKAGE DIMENSIONS

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20 g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)

Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/