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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f585ldpmc-gtk5e1

- Interrupt (PC/PS saving)
  6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and data.
  - Control access privilege in both privilege mode and user mode
- Built-in FPU (floating-point operation)
  - IEEE754 compliant
  - Floating-point register: 32 bits × 16 sets

Peripheral Functions

- Clock generation (SSCG function is available)
  - Main oscillation (4 to 20 MHz)
  - PLL multiplication rate:1 to 32 times
- CR oscillation
  - Oscillation frequency: 100kHz, with frequency accuracy ± 50% (pre-trimming)
  - Trimming is enabled
  - To be used as a count clock of hardware watchdog
  - MB91F585LC/F586LC/F587LC/F585LD/F586LD/F587LD: Oscillation stop feature during stand-by is not available
  - MB91F585LA/F586LA/F587LA/F585LB/F586LB/F587LB: Oscillation stop feature during stand-by is available
- Built-in program flash memory capacity
  MB91F585L: 512+64 Kbytes
  MB91F586L: 768+64 Kbytes
  MB91F587L: 1024+64 Kbytes
- Built-in data flash (WorkFlash) 64 Kbytes
- Built-in RAM capacity
  - Main RAM
    MB91F585L: 48 Kbytes
    MB91F586L: 64 Kbytes
    MB91F587L: 96 Kbytes
  - Backup RAM 8 Kbytes
- General-purpose ports:
  MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC 98 ports
  MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD 111 ports
  - Including eight I^2C pseudo open drain corresponding ports
- External bus interface (MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD)
  - Maximum operating frequency: 40MHz
  - 22-bit address, 16-bit data
- DMA controller
  - Up to 8 channels can be started simultaneously.
  - 2 transfer factors (Internal peripheral request and software)
- External interrupt input: 8 channels
  Level ("H" / "L") or edge detection (rising or falling) enabled
- Multi-function serial communication (built-in transmission/reception FIFO memory): 5 channels
  < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detection functions provided
  - DMA transfer supported

MB91580M Series Product Lineup Comparison

- Memory size

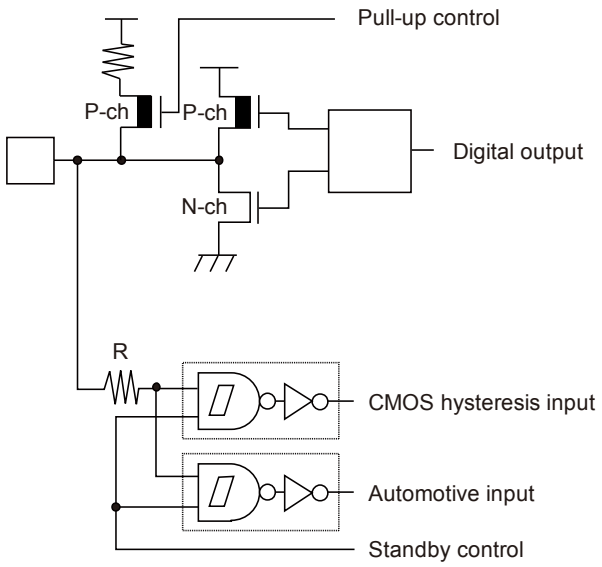
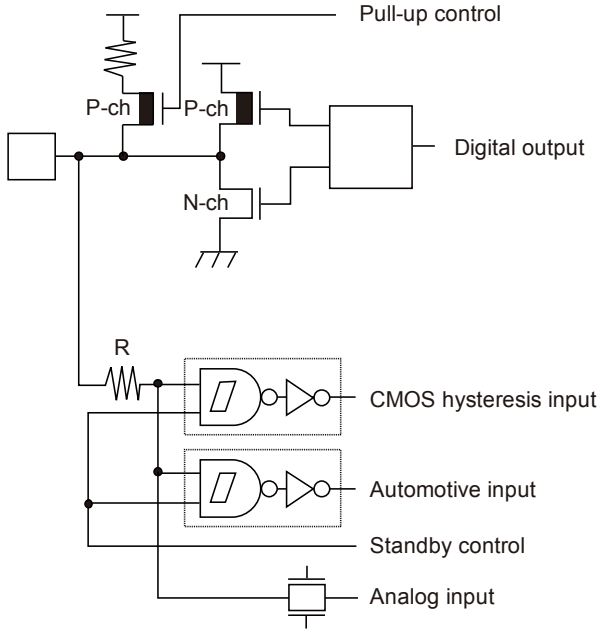
Items	MB91F583MG MB91F583MH MB91F583MJ MB91F583MK	MB91F584MG MB91F584MH MB91F584MJ MB91F584MK	MB91F585MG MB91F585MH MB91F585MJ MB91F585MK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

- Function

Items	MB91F583MG MB91F584MG MB91F585MG	MB91F583MH MB91F584MH MB91F585MH	MB91F583MJ MB91F584MJ MB91F585MJ	MB91F583MK MB91F584MK MB91F585MK
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during stand-by	Provided	Provided	Not provided	Not provided
External bus interface	Not provided			
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	4 channels			
Output compare	7 channels			
Waveform generator	2 unit (7channels)			
16-bit reload timer	4 channels			
PPG	6 channels			
External interrupt	8 channels			
A/D converter	3 units (23 channels)			
R/D converter	Not provided			
D/A converter	Provided			
Up/ down counter	2 channels			
Multi-function serial interface	4 channels			
CAN	64msb × 2 channels (ch.0/ch.1)			
FlexRay	128msb × 1 unit (ch.A / ch.B)	Not provided	128msb × 1 unit (ch.A / ch.B)	Not provided
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	2 channels			
Low-voltage detection reset (Internal low-voltage detection)	Provided			
Low-voltage detection reset (External low-voltage detection)	Provided			
Device package	LQFP-100			
Debug interface	Built-in OCD (On Chip Debug Unit)			

Note: For details on the MB91580M series, see the "MB91580M/S Series HARDWARE MANUAL".

Pin No.	Pin name	I/O circuit type*1	Function
96	P110	D	General-purpose I/O port
	TX1		CAN transmission data 1 output pin
97	P111	E	General-purpose I/O port
	RX1		CAN reception data 1 input pin
	INT1		INT1 external interrupt input pin
98	P112	D	General-purpose I/O port
	RTO0		Waveform generator ch.0 output pin
	PPG16		PPG ch.16 output pin
99	P113	D	General-purpose I/O port
	RTO1		Waveform generator ch.1 output pin
	PPG17		PPG ch.17 output pin
100	P114	D	General-purpose I/O port
	RTO2		Waveform generator ch.2 output pin
	PPG18		PPG ch.18 output pin
101	P115	D	General-purpose I/O port
	RTO3		Waveform generator ch.3 output pin
	PPG19		PPG ch.19 output pin
102	P116	D	General-purpose I/O port
	RTO4		Waveform generator ch.4 output pin
	PPG20		PPG ch.20 output pin
103	P117	D	General-purpose I/O port
	RTO5		Waveform generator ch.5 output pin
	PPG21		PPG ch.21 output pin
104	P120	D	General-purpose I/O port
	RTO6		Waveform generator ch.6 output pin
	PPG22		PPG ch.22 output pin
105	P121	D	General-purpose I/O port
	RTO7		Waveform generator ch.7 output pin
	PPG23		PPG ch.23 output pin
106	P122	D	General-purpose I/O port
	RTO8		Waveform generator ch.8 output pin
107	P123	D	General-purpose I/O port
	RTO9		Waveform generator ch.9 output pin
111	P124	D	General-purpose I/O port
	RTO10		Waveform generator ch.10 output pin
112	P125	D	General-purpose I/O port
	RTO11		Waveform generator ch.11 output pin
113	P126	E	General-purpose I/O port
	SIN0		Multi-function serial ch.0 serial data input pin
	INT6		INT6 external interrupt input pin
114	P127	K	General-purpose I/O port
	SOT0		Multi-function serial ch.0 serial data output pin/ I^2C ch.0 serial data I/O pin (SDA)
115	P130	K	General-purpose I/O port
	SCK0		Multi-function serial ch.0 clock I/O pin/ I^2C ch.0 clock I/O pin (SCL)

Type	Circuit	Remarks
E		• General-purpose I/O port • CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA • With 50 kΩ pull-up resistor control • CMOS hysteresis input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. • Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.
F		• With analog input, general-purpose I/O port • CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA • With 50 kΩ pull-up resistor control • CMOS hysteresis input (0.7Vcc/0.3Vcc) • Automotive input (0.8Vcc/0.5Vcc)

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0002E0_H$	-	GATEC0[R/W] B,H,W ------00	-	GATEC2[R/W] B,H,W ------00	PPG GATE Control
$0002E4_H$	-	GATEC4[R/W] B,H,W ------00	-	GATEC8[R/W] B,H,W ------00	
$0002E8_H$	-	GATEC10[R/W] B,H,W ------00	-	GATEC12[R/W] B,H,W ------00	
$0002EC_H$	-	-	-	-	Reserved
$0002F0_H$	RCRH0[W] H,W 00000000	RCRL0[W] B,H,W 00000000	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	U/D counter 0
$0002F4_H$	CCR0[R/W] B,H 00000000 -0001000		-	CSR0[R] B 00000000	
$0002F8_H$	RCRH1[W] H,W 00000000	RCRL1[W] B,H,W 00000000	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	U/D counter 1
$0002FC_H$	CCR1[R/W] B,H 00000000 -0001000		-	CSR1[R] B 00000000	
000300_H	-				Reserved
000304_H	-	-	-	-	Reserved
000308_H	-				Reserved
$00030C_H$	-	-	-	-	
000310_H	-	-	MPUCR[R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	-	-	-	-	
000318_H	-				
$00031C_H$	-	-	-		
000320_H	DPVAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	-	-	DPVSR[R/W] H -------- 00000--0		
000328_H	DEAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	-	-	DESR[R/W] H -------- 00000--0		
000330_H	PABR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	-	-	PACR0[R/W] H 000000-0 00000--0		
000338_H	PABR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	-	-	PACR1[R/W] H 000000-0 00000--0		
000340_H	PABR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	-	-	PACR2[R/W] H 000000-0 00000--0		
000348_H	PABR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	-	-	PACR3[R/W] H 000000-0 00000--0		
000350_H	PABR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000480_H	RSTRR[R] B,H,W XXXX--XX	RSTCR[R/W] B,H,W 111----0	STBCR[R/W] B,H,W* 000---11	-	Reset control [S] Power consumption control [S] * Writing to STBCR by DMA is disabled.
000484_H	-	-	-	-	Reserved [S]
000488_H	DIVR0[R/W] B,H,W 000-----	-	DIVR2[R/W] B,H,W 0011----	-	Clock control [S]
$00048C_H$	-	-	-	-	Reserved [S]
000490_H	IORR0[R/W] B,H,W -0000000	IORR1[R/W] B,H,W -0000000	IORR2[R/W] B,H,W -0000000	IORR3[R/W] B,H,W -0000000	DMA transfer request from a peripheral [S]
000494_H	IORR4[R/W] B,H,W -0000000	IORR5[R/W] B,H,W -0000000	IORR6[R/W] B,H,W -0000000	IORR7[R/W] B,H,W -0000000	
000498_H	-	-	-	-	
$00049C_H$	-	-	-	-	
$0004A0_H$	-	-	-	-	Reserved
$0004A4_H$	CANPRE[R/W] B,H,W ----0000	-	-	-	CAN prescaler
$0004A8_H$ | $0004AC_H$	-	-	-	-	Reserved
$0004B0_H$	-	-	-	-	Reserved
$0004B4_H$ | $0004C0_H$	-	-	-	-	Reserved
$0004C4_H$	CUCR1[R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		WDT1 calibration
$0004C8_H$	CUTR1[R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$ | $0004DC_H$	-	-	-	-	Reserved
$0004E0_H$	-	-	CSCFG[R/W] B,H,W ---0----	CMCFG[R/W] B,H,W 00000000	Clock monitor
$0004E4_H$	-	-	-	-	
$0004E8_H$	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	FlexRay/RDC clock control
$0004EC_H$	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -------0	CLKR2[R/W] B,H,W 000--000	-	
$0004F0_H$ | $0004FC_H$	-	-	-	-	Reserved
000500_H	-				Reserved
000504_H	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000720_H | $0007F8_H$	-	-	-	-	Reserved
$0007FC_H$	BMODR[R] B,H,W XXXXXXXX	-	-	-	Operation mode
000800_H | $00083C_H$	-	-	-	-	Reserved [S]
000840_H	FCTLR[R/W] H -0--1000 0--0----		-	FSTR[R/W] B -----001	Flash memory register [S]
000844_H	-	-	-	-	Reserved [S]
000848_H | 000854_H	-	-	-	-	Reserved [S]
000858_H	-	-	WREN[R/W] H 00000000 00000000		Wild register [S]
$00085C_H$ | $00087C_H$	-	-	-	-	Reserved [S]
000880_H	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884_H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A0_H$	WRAR04[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008A4_H$	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A8_H$	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B8_H$	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008BC_H$	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000C2C_H$	DDAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA controller [S]
$000C30_H$	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
$000C34_H$	DCSR3[R/W] H 0------- -----000		DTCR3[R/W] H 00000000 00000000		
$000C38_H$	DSAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C3C_H$	DDAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C40_H$	DCCR4[R/W] W 0----000 --00--00 00000000 0-000000				
$000C44_H$	DCSR4[R/W] H 0------- -----000		DTCR4[R/W] H 00000000 00000000		
$000C48_H$	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C4C_H$	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C50_H$	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000				
$000C54_H$	DCSR5[R/W] H 0------- -----000		DTCR5[R/W] H 00000000 00000000		
$000C58_H$	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6[R/W] H 0------- -----000		DTCR6[R/W] H 00000000 00000000		
$000C68_H$	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7[R/W] H 0------- -----000		DTCR7[R/W] H 00000000 00000000		
$000C78_H$	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$ | $000DF0_H$	-	-	-	-	
$000DF4_H$	-	-	DNMIR[R/W] B 0------0	DILVR[R/W] B ---11111	
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D174_H$	OSID2[R] W -------- -------- 00----00 00000000				FlexRay GTU
$00D178_H$	OSID3[R] W -------- -------- 00----00 00000000				
$00D17C_H$	OSID4[R] W -------- -------- 00----00 00000000				
$00D180_H$	OSID5[R] W -------- -------- 00----00 00000000				
$00D184_H$	OSID6[R] W -------- -------- 00----00 00000000				
$00D188_H$	OSID7[R] W -------- -------- 00----00 00000000				
$00D18C_H$	OSID8[R] W -------- -------- 00----00 00000000				
$00D190_H$	OSID9[R] W -------- -------- 00----00 00000000				
$00D194_H$	OSID10[R] W -------- -------- 00----00 00000000				
$00D198_H$	OSID11[R] W -------- -------- 00----00 00000000				
$00D19C_H$	OSID12[R] W -------- -------- 00----00 00000000				
$00D1A0_H$	OSID13[R] W -------- -------- 00----00 00000000				
$00D1A4_H$	OSID14[R] W -------- -------- 00----00 00000000				
$00D1A8_H$	OSID15[R] W -------- -------- 00----00 00000000				
$00D1AC_H$	-				Reserved
$00D1B0_H$	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM
$00D1B4_H$	NMV2[R] W 00000000 00000000 00000000 00000000				
$00D1B8_H$	NMV3[R] W 00000000 00000000 00000000 00000000				
$00D1BC_H$ | $00D2FC_H$	-				Reserved
$00D300_H$	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD
$00D304_H$	FRF[R/W] W -------1 10000000 ---00000 00000000				
$00D308_H$	FRFM[R/W] W -------- -------- ---00000 000000--				
$00D30C_H$	FCL[R/W] W -------- -------- -------- 10000000				
$00D310_H$	MHDS[R/W] W -0000000 -0000000 -0000000 00000000				
$00D314_H$	LDTS[R] W -----000 00000000 -----000 00000000				
$00D318_H$	FSR[R] W -------- -------- 00000000 -----000				
$00D31C_H$	MHDF[R/W] W -------- -------- -------0 00000000				

- MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000000_H	PDR00[R/W] B,H,W XXXXXXXX	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register
000004_H	PDR04[R/W] B,H,W XXXXXXXX	PDR05[R/W] B,H,W XXXXXXXX	PDR06[R/W] B,H,W XXXXXXXX	PDR07[R/W] B,H,W XXXXXXXX	
000008_H	PDR08[R/W] B,H,W XXXXXXXX	PDR09[R/W] B,H,W XXXXXXXX	PDR10[R/W] B,H,W XXXXXXXX	PDR11[R/W] B,H,W XXXXXXXX	
$00000C_H$	PDR12[R/W] B,H,W XXXXXXXX	PDR13[R/W] B,H,W XX-XXXXX	-	-	
000010_H | 000038_H	-	-	-	-	Reserved
$00003C_H$	WDTCR0[R/W] B,H,W -0--0000	WDTCPR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ----0010	WDTCPR1[W] B,H,W 00000000	Watchdog timer [S]
000040_H	-	-	-	-	Reserved
000044_H	DICR[R/W] B -------0	-	-	-	Delay interrupt
000048_H | $00005C_H$	-		-		Reserved
000060_H	TMRLRA0[R/W] H XXXXXXXX XXXXXXXX		TMR0[R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064_H	TMRLRB0[R/W] H XXXXXXXX XXXXXXXX		TMCSR0[R/W] B,H,W 00000000 0-000000		
000068_H | $00007C_H$	-	-	-	-	Reserved
000080_H	BT0TMR[R] H 00000000 00000000		BT0TMCR[R/W] H -0000000 00000000		Base timer 0
000084_H	BT0TMCR2 [R/W] B -------0	BT0STC [R/W] B -0-0-0-0	-	-	
000088_H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
$00008C_H$	-	-	-	-	
000090_H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W] H -0000000 00000000		Base timer 1
000094_H	BT1TMCR2 [R/W] B -------0	BT1STC [R/W] B -0-0-0-0	-	-	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL01[R/W] B ----0000	-	BTSSSR[W] B,H -------- ------11		Base timer 0, 1
$0000A0_H$ | $0000FC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000218_H	PCN3[R/W] B,H,W 00000000 000000-0		PCSR3[W] H,W XXXXXXXX XXXXXXXX		PPG3
$00021C_H$	PDUT3[W] H,W XXXXXXXX XXXXXXXX		PTMR3[R] H,W 11111111 11111111		
000220_H	PCN4[R/W] B,H,W 00000000 000000-0		PCSR4[W] H,W XXXXXXXX XXXXXXXX		PPG4
000224_H	PDUT4[W] H,W XXXXXXXX XXXXXXXX		PTMR4[R] H,W 11111111 11111111		
000228_H	PCN5[R/W] B,H,W 00000000 000000-0		PCSR5[W] H,W XXXXXXXX XXXXXXXX		PPG5
$00022C_H$	PDUT5[W] H,W XXXXXXXX XXXXXXXX		PTMR5[R] H,W 11111111 11111111		
000230_H	PCN6[R/W] B,H,W 00000000 000000-0		PCSR6[W] H,W XXXXXXXX XXXXXXXX		PPG6
000234_H	PDUT6[W] H,W XXXXXXXX XXXXXXXX		PTMR6[R] H,W 11111111 11111111		
000238_H	PCN7[R/W] B,H,W 00000000 000000-0		PCSR7[W] H,W XXXXXXXX XXXXXXXX		PPG7
$00023C_H$	PDUT7[W] H,W XXXXXXXX XXXXXXXX		PTMR7[R] H,W 11111111 11111111		
000240_H	PCN8[R/W] B,H,W 00000000 000000-0		PCSR8[W] H,W XXXXXXXX XXXXXXXX		PPG8
000244_H	PDUT8[W] H,W XXXXXXXX XXXXXXXX		PTMR8[R] H,W 11111111 11111111		
000248_H	PCN9[R/W] B,H,W 00000000 000000-0		PCSR9[W] H,W XXXXXXXX XXXXXXXX		PPG9
$00024C_H$	PDUT9[W] H,W XXXXXXXX XXXXXXXX		PTMR9[R] H,W 11111111 11111111		
000250_H	PCN10[R/W] B,H,W 00000000 000000-0		PCSR10[W] H,W XXXXXXXX XXXXXXXX		PPG10
000254_H	PDUT10[W] H,W XXXXXXXX XXXXXXXX		PTMR10[R] H,W 11111111 11111111		
000258_H	PCN11[R/W] B,H,W 00000000 000000-0		PCSR11[W] H,W XXXXXXXX XXXXXXXX		PPG11
$00025C_H$	PDUT11[W] H,W XXXXXXXX XXXXXXXX		PTMR11[R] H,W 11111111 11111111		
000260_H	PCN12[R/W] B,H,W 00000000 000000-0		PCSR12[W] H,W XXXXXXXX XXXXXXXX		PPG12
000264_H	PDUT12[W] H,W XXXXXXXX XXXXXXXX		PTMR12[R] H,W 11111111 11111111		
000268_H	PCN13[R/W] B,H,W 00000000 000000-0		PCSR13[W] H,W XXXXXXXX XXXXXXXX		PPG13
$00026C_H$	PDUT13[W] H,W XXXXXXXX XXXXXXXX		PTMR13[R] H,W 11111111 11111111		
000270_H	PCN14[R/W] B,H,W 00000000 000000-0		PCSR14[W] H,W XXXXXXXX XXXXXXXX		PPG14
000274_H	PDUT14[W] H,W XXXXXXXX XXXXXXXX		PTMR14[R] H,W 11111111 11111111		
000278_H	PCN15[R/W] B,H,W 00000000 000000-0		PCSR15[W] H,W XXXXXXXX XXXXXXXX		PPG15
$00027C_H$	PDUT15[W] H,W XXXXXXXX XXXXXXXX		PTMR15[R] H,W 11111111 11111111		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000414_H	ICSEL20[R/W] B,H,W -------0	ICSEL21[R/W] B,H,W -----000	ICSEL22[R/W] B,H,W -----000	ICSEL23[R/W] B,H,W -----000	Generation and clearing of DMA transfer requests
000418_H	ICSEL24[R/W] B,H,W -----000	ICSEL25[R/W] B,H,W -----000	ICSEL26[R/W] B,H,W -------0	ICSEL27[R/W] B,H,W -------0	
$00041C_H$	-	-	-	-	
000420_H	-	-	-	-	
000424_H | $00043C_H$	-	-	-	-	Reserved
000440_H	ICR00[R/W] B,H,W ---11111	ICR01[R/W] B,H,W ---11111	ICR02[R/W] B,H,W ---11111	ICR03[R/W] B,H,W ---11111	Interrupt controller [S]
000444_H	ICR04[R/W] B,H,W ---11111	ICR05[R/W] B,H,W ---11111	ICR06[R/W] B,H,W ---11111	ICR07[R/W] B,H,W ---11111	
000448_H	ICR08[R/W] B,H,W ---11111	ICR09[R/W] B,H,W ---11111	ICR10[R/W] B,H,W ---11111	ICR11[R/W] B,H,W ---11111	
$00044C_H$	ICR12[R/W] B,H,W ---11111	ICR13[R/W] B,H,W ---11111	ICR14[R/W] B,H,W ---11111	ICR15[R/W] B,H,W ---11111	
000450_H	ICR16[R/W] B,H,W ---11111	ICR17[R/W] B,H,W ---11111	ICR18[R/W] B,H,W ---11111	ICR19[R/W] B,H,W ---11111	
000454_H	ICR20[R/W] B,H,W ---11111	ICR21[R/W] B,H,W ---11111	ICR22[R/W] B,H,W ---11111	ICR23[R/W] B,H,W ---11111	
000458_H	ICR24[R/W] B,H,W ---11111	ICR25[R/W] B,H,W ---11111	ICR26[R/W] B,H,W ---11111	ICR27[R/W] B,H,W ---11111	
$00045C_H$	ICR28[R/W] B,H,W ---11111	ICR29[R/W] B,H,W ---11111	ICR30[R/W] B,H,W ---11111	ICR31[R/W] B,H,W ---11111	
000460_H	ICR32[R/W] B,H,W ---11111	ICR33[R/W] B,H,W ---11111	ICR34[R/W] B,H,W ---11111	ICR35[R/W] B,H,W ---11111	
000464_H	ICR36[R/W] B,H,W ---11111	ICR37[R/W] B,H,W ---11111	ICR38[R/W] B,H,W ---11111	ICR39[R/W] B,H,W ---11111	
000468_H	ICR40[R/W] B,H,W ---11111	ICR41[R/W] B,H,W ---11111	ICR42[R/W] B,H,W ---11111	ICR43[R/W] B,H,W ---11111	
$00046C_H$	ICR44[R/W] B,H,W ---11111	ICR45[R/W] B,H,W ---11111	ICR46[R/W] B,H,W ---11111	ICR47[R/W] B,H,W ---11111	
000470_H | $00047C_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000C6C_H$	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA controller [S]
$000C70_H$	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7[R/W] H 0------- -----000		DTCR7[R/W] H 00000000 00000000		
$000C78_H$	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$ | $000DF0_H$	-	-	-	-	
$000DF4_H$	-	-	DNMIR[R/W] B 0------0	DILVR[R/W] B ---11111	
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	-	-	-	-	Reserved [S]
$000E00_H$	DDR00[R/W] B,H 00000000	DDR01[R/W] B,H 00000000	DDR02[R/W] B,H 00000000	DDR03[R/W] B,H 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H 00000000	DDR05[R/W] B,H 00000000	DDR06[R/W] B,H 00000000	DDR07[R/W] B,H 00000000	
$000E08_H$	DDR08[R/W] B,H 00000000	DDR09[R/W] B,H 00000000	DDR10[R/W] B,H 00000000	DDR11[R/W] B,H 00000000	
$000E0C_H$	DDR12[R/W] B,H 00000000	DDR13[R/W] B,H 00-00000	-	-	
$000E10_H$ | $000E1C_H$	-	-	-	-	Reserved
$000E20_H$	PFR00[R/W] B,H 00000000	PFR01[R/W] B,H 00000000	PFR02[R/W] B,H 00000000	PFR03[R/W] B,H 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H 00000000	PFR05[R/W] B,H 00000000	PFR06[R/W] B,H 00000000	PFR07[R/W] B,H 00000000	
$000E28_H$	PFR08[R/W] B,H 00000000	PFR09[R/W] B,H 00000000	PFR10[R/W] B,H 00000000	PFR11[R/W] B,H 00000000	
$000E2C_H$	PFR12[R/W] B,H 00000000	PFR13[R/W] B,H 00-00000	-	-	
$000E30_H$ | $000E3C_H$	-	-	-	-	Reserved
$000E40_H$	PDDR00[R] B,H,W XXXXXXXX	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
$000E44_H$	PDDR04[R] B,H,W XXXXXXXX	PDDR05[R] B,H,W XXXXXXXX	PDDR06[R] B,H,W XXXXXXXX	PDDR07[R] B,H,W XXXXXXXX	
$000E48_H$	PDDR08[R] B,H,W XXXXXXXX	PDDR09[R] B,H,W XXXXXXXX	PDDR10[R] B,H,W XXXXXXXX	PDDR11[R] B,H,W XXXXXXXX	
$000E4C_H$	PDDR12[R] B,H,W XXXXXXXX	PDDR13[R] B,H,W XX-XXXXX	-	-	
$000E50_H$ | $000E5C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0021B4_H$	MSGVAL41[R] B,H,W 00000000 00000000		MSGVAL31[R] B,H,W 00000000 00000000		CAN 1 64msb
$0021B8_H$	-		-		
$0021BC_H$	-		-		
$0021C0_H$ | $0021FC_H$	-		-		
002200_H	CTRLR2[R/W] B,H,W -------- 000-0001		STATR2[R/W] B,H,W -------- 00000000		CAN 2 64msb
002204_H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2[R/W] B,H,W -0100011 00000001		
002208_H	INTR2[R] B,H,W 00000000 00000000		TESTR2[R/W] B,H,W -------- X00000--		
$00220C_H$	BRPER2[R/W] B,H,W -------- ----0000		-		
002210_H	IF1CREQ2[R/W] B,H,W 0------- 00000001		IF1CMSK2[R/W] B,H,W -------- 00000000		
002214_H	IF1MSK22[R/W] B,H,W 11-11111 11111111		IF1MSK12[R/W] B,H,W 11111111 11111111		
002218_H	IF1ARB22[R/W] B,H,W 00000000 00000000		IF1ARB12[R/W] B,H,W 00000000 00000000		
$00221C_H$	IF1MCTR2[R/W] B,H,W 00000000 0---0000		-		
002220_H	IF1DTA12[R/W] B,H,W 00000000 00000000		IF1DTA22[R/W] B,H,W 00000000 00000000		
002224_H	IF1DTB12[R/W] B,H,W 00000000 00000000		IF1DTB22[R/W] B,H,W 00000000 00000000		
002228_H, $00222C_H$	-		-		
002230_H, 002234_H	Reserved (IF1 data mirror)				
002238_H, $00223C_H$	-		-		
002240_H	IF2CREQ2[R/W] B,H,W 0------- 00000001		IF2CMSK2[R/W] B,H,W -------- 00000000		
002244_H	IF2MSK22[R/W] B,H,W 11-11111 11111111		IF2MSK12[R/W] B,H,W 11111111 11111111		
002248_H	IF2ARB22[R/W] B,H,W 00000000 00000000		IF2ARB12[R/W] B,H,W 00000000 00000000		
$00224C_H$	IF2MCTR2[R/W] B,H,W 00000000 0---0000		-		
002250_H	IF2DTA12[R/W] B,H,W 00000000 00000000		IF2DTA22[R/W] B,H,W 00000000 00000000		
002254_H	IF2DTB12[R/W] B,H,W 00000000 00000000		IF2DTB22[R/W] B,H,W 00000000 00000000		
002258_H, $00225C_H$	-		-		
002260_H, 002264_H	Reserved (IF2 data mirror)				
002268_H | $00227C_H$	-		-		
002280_H	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D190_H$	OSID9[R] W -------- -------- 00----00 00000000				FlexRay GTU
$00D194_H$	OSID10[R] W -------- -------- 00----00 00000000				
$00D198_H$	OSID11[R] W -------- -------- 00----00 00000000				
$00D19C_H$	OSID12[R] W -------- -------- 00----00 00000000				
$00D1A0_H$	OSID13[R] W -------- -------- 00----00 00000000				
$00D1A4_H$	OSID14[R] W -------- -------- 00----00 00000000				
$00D1A8_H$	OSID15[R] W -------- -------- 00----00 00000000				
$00D1AC_H$	-				Reserved
$00D1B0_H$	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM
$00D1B4_H$	NMV2[R] W 00000000 00000000 00000000 00000000				
$00D1B8_H$	NMV3[R] W 00000000 00000000 00000000 00000000				
$00D1BC_H$ | $00D2FC_H$	-				Reserved
$00D300_H$	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD
$00D304_H$	FRF[R/W] W -------1 10000000 ---00000 00000000				
$00D308_H$	FRFM[R/W] W -------- -------- ---00000 000000--				
$00D30C_H$	FCL[R/W] W -------- -------- -------- 10000000				
$00D310_H$	MHDS[R/W] W -0000000 -0000000 -0000000 00000000				
$00D314_H$	LDTS[R] W -----000 00000000 -----000 00000000				
$00D318_H$	FSR[R] W -------- -------- 00000000 -----000				
$00D31C_H$	MHDF[R/W] W -------- -------- -------0 00000000				
$00D320_H$	TXRQ1[R] W 00000000 00000000 00000000 00000000				
$00D324_H$	TXRQ2[R] W 00000000 00000000 00000000 00000000				
$00D328_H$	TXRQ3[R] W 00000000 00000000 00000000 00000000				
$00D32C_H$	TXRQ4[R] W 00000000 00000000 00000000 00000000				
$00D330_H$	NDAT1[R] W 00000000 00000000 00000000 00000000				
$00D334_H$	NDAT2[R] W 00000000 00000000 00000000 00000000				
$00D338_H$	NDAT3[R] W 00000000 00000000 00000000 00000000				

(T_A: Recommended operating conditions, Vcc=5.0V±10%,V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OH}=-2.0mA	Vcc-0.5	-	Vcc	V	
	V_{OH2}	P003 to P007, P010	Vcc=4.5V I_{OH}=-4.0mA	Vcc-0.5	-	Vcc	V	When FlexRay is selected
	V_{OH3}	P000 to P002, P011 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OH}=-5.0mA	Vcc-0.5	-	Vcc	V	

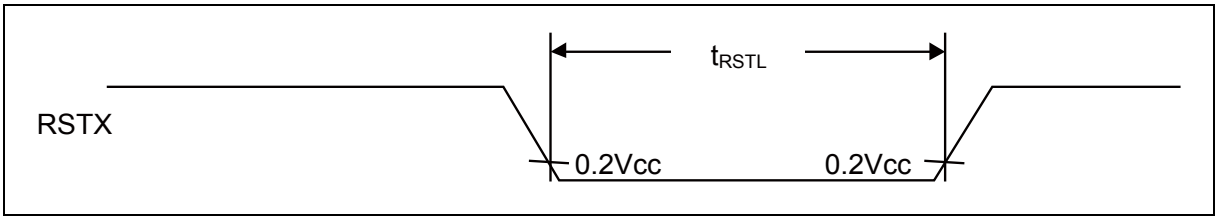
*: Only available with MB91F585LB/F586LB/F587LB, MB91F585LD/F586LD/F587LD

(2) Reset input

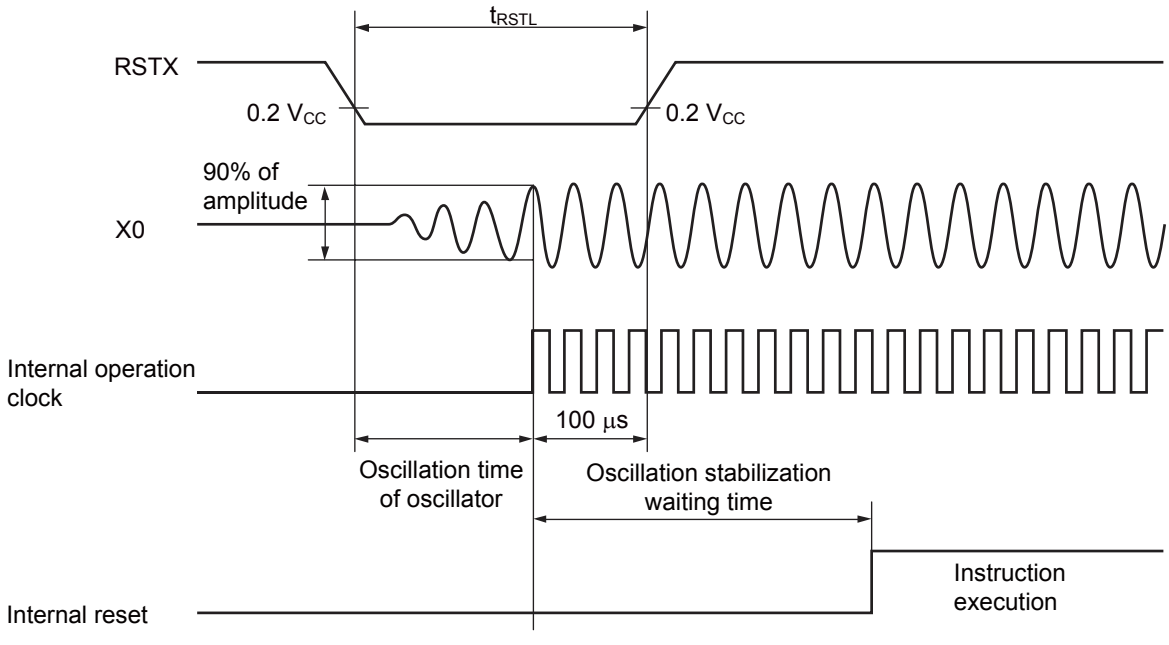
(T_A: Recommended operating conditions, Vcc =5.0V±10%, Vss=AVss=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	-	10	-	µs	During normal operation
				Oscillation time of oscillator * +0.1	-	ms	At Stop mode
				100	-	µs	At Clock mode
Width for reset input removal				1	-	µs	

*: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.



- In Stop mode

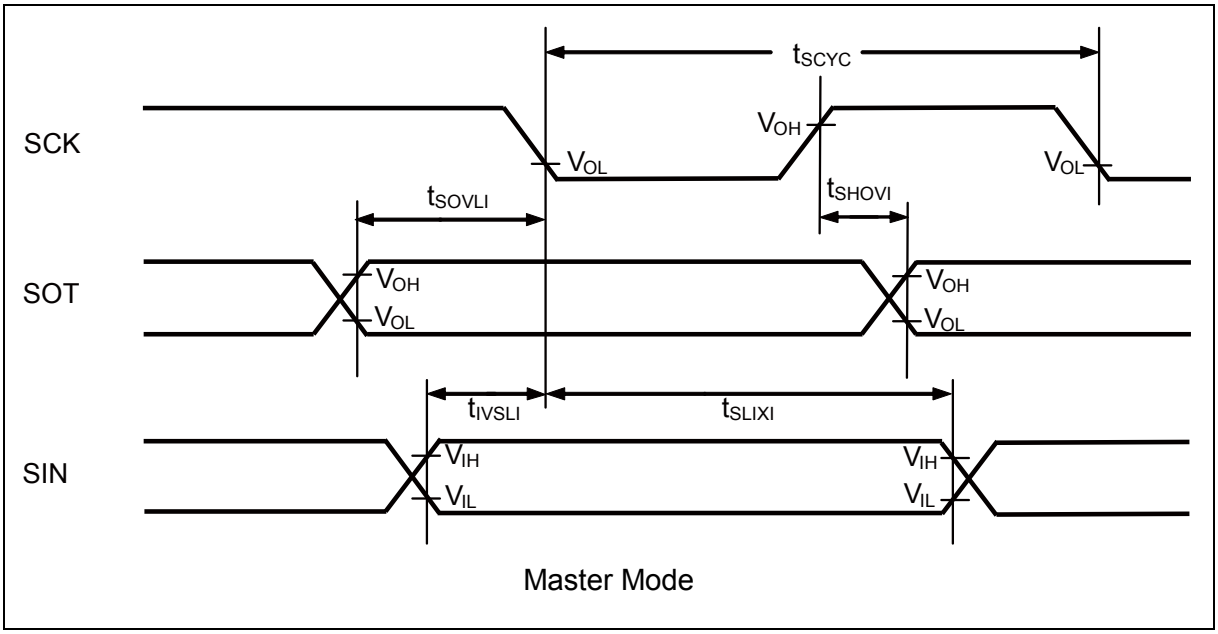


(4-1-2) Normal synchronous transfer (SCR:SPI=0) and serial clock output signal detect level "L"(SMR:SCINV=1)

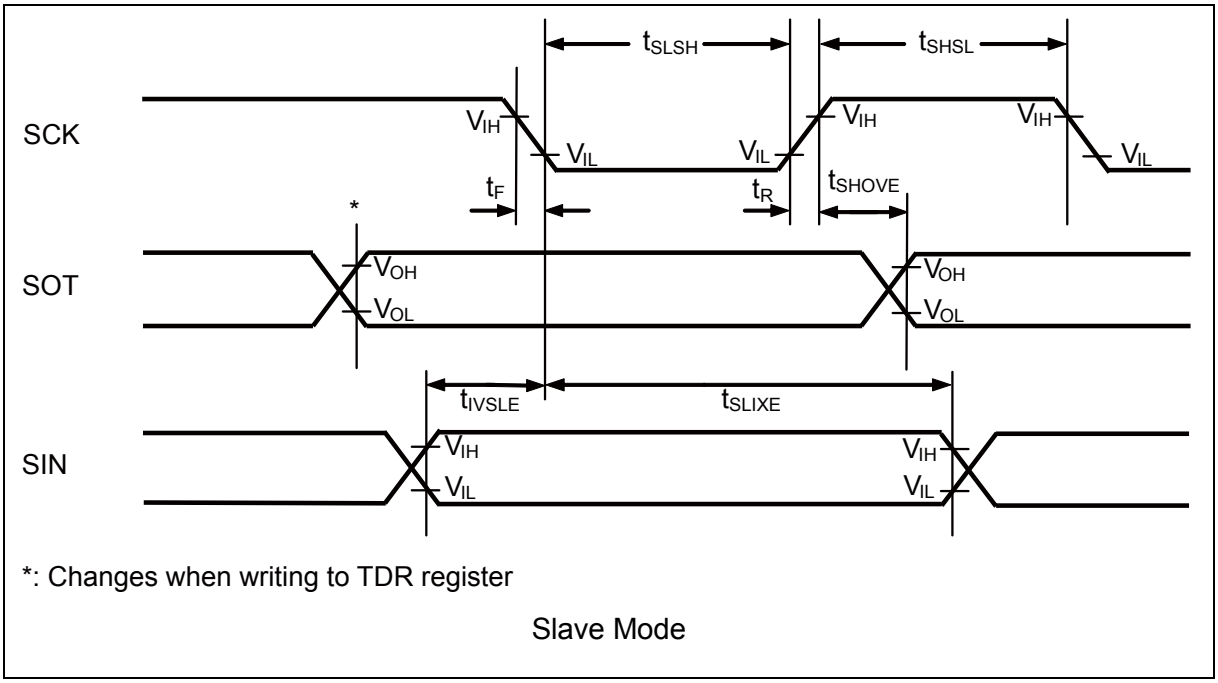
(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK3_1,SCK4_1	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVI}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-30	+30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		30	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXI}			0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK3_1, SCK4_1	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVE}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		10	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4, SCK3_1, SCK4_1		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4, SCK3_1, SCK4_1		-	5	ns	

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



*: Changes when writing to TDR register

Slave Mode

(8) Low-voltage detection (External low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC5	-	-	-	5.5	V	
Detection voltage	V_{DL}	VCC5	*1	3.7	3.9	4.1	V	When power supply voltage falls and detection level is set initially
Hysteresis width	V_{HYS}	VCC5	-	-	-	125	mV	When power supply voltage rises
Low-voltage detection time	Td	-	-	-	-	30	µs	
Power supply voltage fluctuation rate	-	VCC5	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (Td), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: In order to perform the low-voltage detection at the detection voltage (V_{DL}), be sure to suppress fluctuation of the power supply within the limits of the power supply voltage fluctuation rate.

(9) Low-voltage detection (Internal low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	-	-	-	-	1.3	V	
Detection voltage	V_{RDL}	-	*	0.8	0.9	1.0	V	When power supply voltage falls
Hysteresis width	V_{RHYS}	-	-	-	-	50	mV	When power supply voltage rises
Low-voltage detection time	-	-	-	-	-	30	µs	

*: If the fluctuation of the power supply is faster than the low-voltage detection time (Td), there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.