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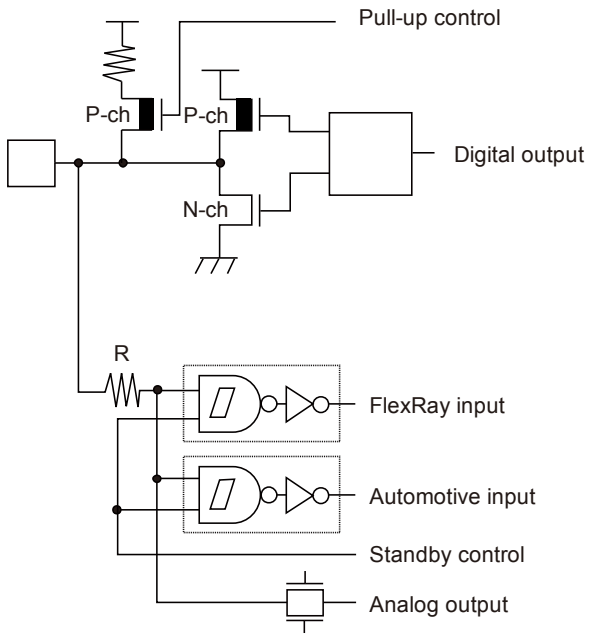
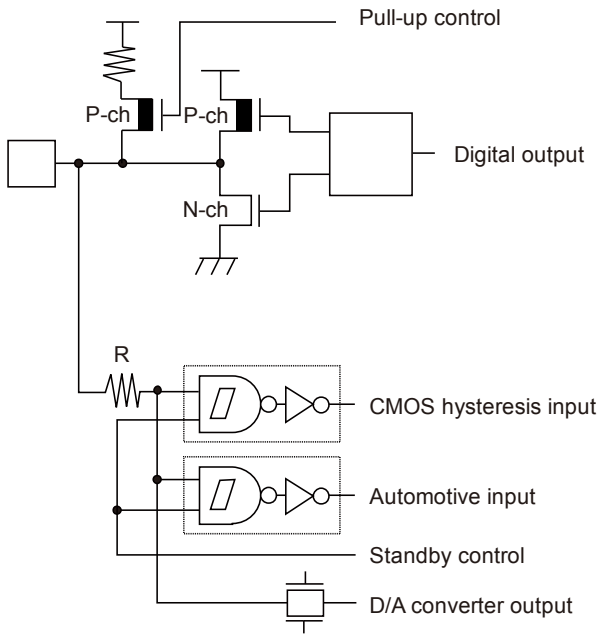
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f586lbpmc-gtk5e1

Type	Circuit	Remarks
O		• With analog output, general-purpose I/O port • CMOS level output I_{OH}=-2/-4mA, I_{OL}=2/4mA • With 50 kΩ pull-up resistor control • FlexRay input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. • Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.
P		• With D/A converter output, general-purpose I/O port • CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA • With 50 kΩ pull-up resistor control • CMOS hysteresis input (0.7Vcc/0.3Vcc) • Automotive input (0.8Vcc/0.5Vcc)

*: MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC only

■ HANDLING DEVICES

The latch-up prevention and pin processing are explained below.

- For latch-up prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.
Also, the analog power supplies (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3) and analog input must not exceed the digital power supply (VCC5) when the power supply to the analog system is turned on or off.
In the correct power-on sequence, turn on the digital power supply voltage (VCC5) and analog power supply voltages (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3) simultaneously. Alternatively, turn on the digital power supply voltage (VCC5) first, and then turn on the analog power supplies (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3).

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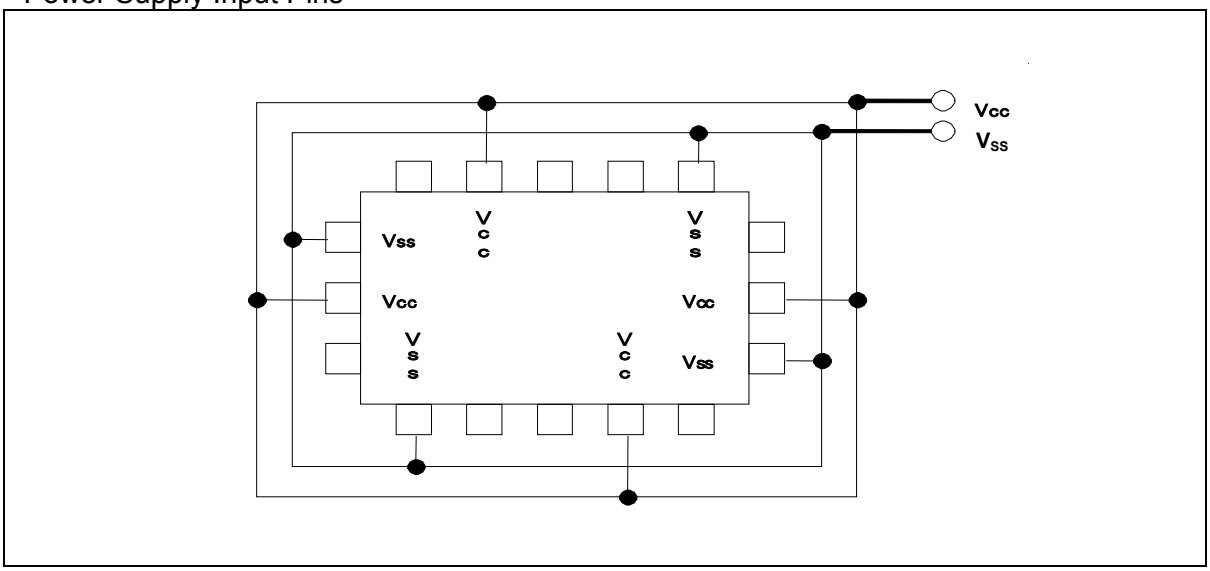
- Treatment of unused pins

If unused input pins are left open, they may cause a permanent damage to the device due to device malfunction or latch-up. Connect a 2kΩ or higher resistor to each of unused input pins for pull-up or pull-down processing.
Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

- Power supply pins

The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown below, all VSS power supply pins must be treated in the similar way. If multiple VCC or VSS systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Power Supply Input Pins

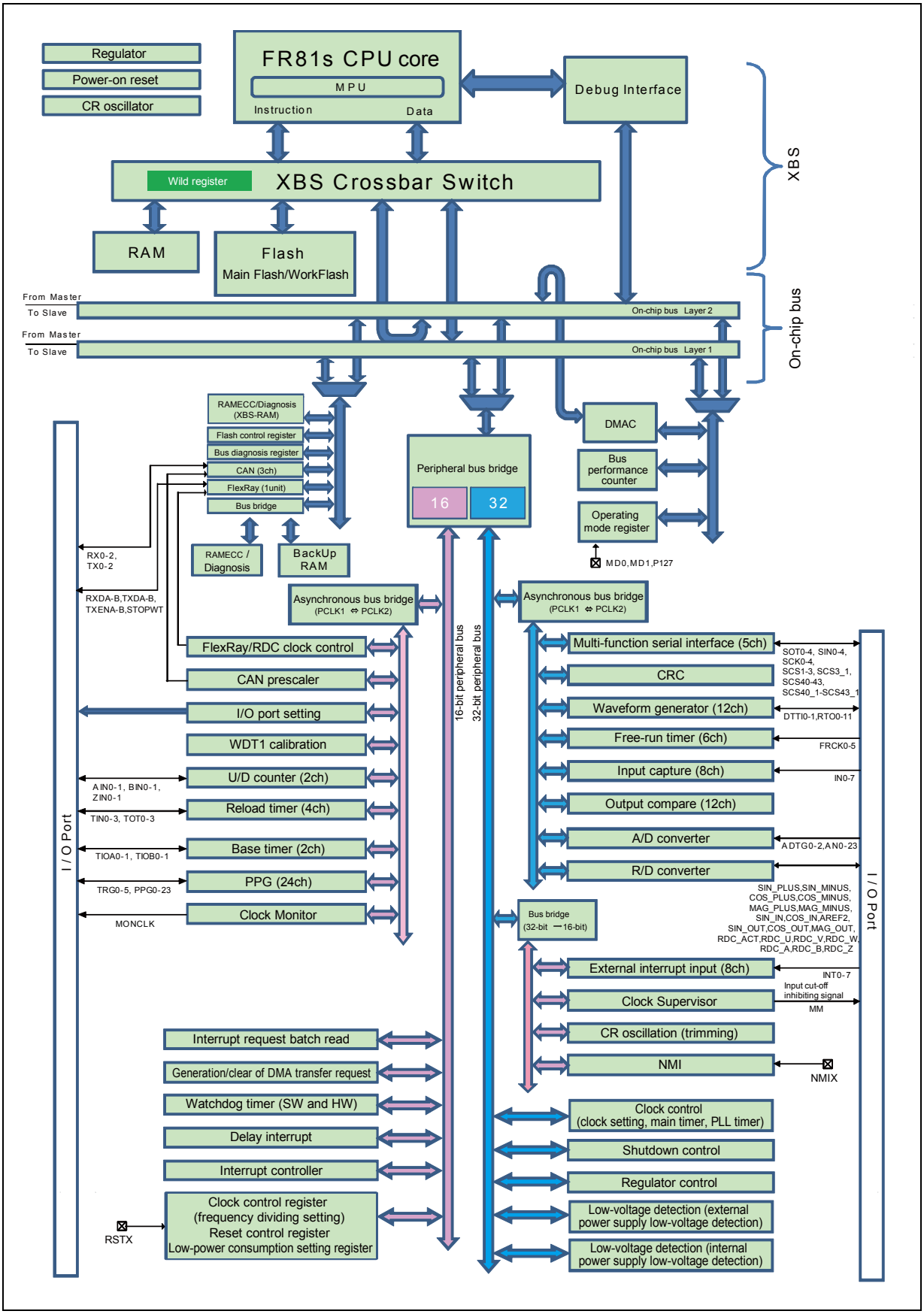


The power supply pins should be connected to VCC and VSS of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

■ BLOCK DIAGRAM

• MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC



Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000278_H	PCN15[R/W] B,H,W 00000000 000000-0		PCSR15[W] H,W XXXXXXXX XXXXXXXX		PPG15
$00027C_H$	PDUT15[W] H,W XXXXXXXX XXXXXXXX		PTMR15[R] H,W 11111111 11111111		
000280_H	PCN16[R/W] B,H,W 00000000 000000-0		PCSR16[W] H,W XXXXXXXX XXXXXXXX		PPG16
000284_H	PDUT16[W] H,W XXXXXXXX XXXXXXXX		PTMR16[R] H,W 11111111 11111111		
000288_H	PCN17[R/W] B,H,W 00000000 000000-0		PCSR17[W] H,W XXXXXXXX XXXXXXXX		PPG17
$00028C_H$	PDUT17[W] H,W XXXXXXXX XXXXXXXX		PTMR17[R] H,W 11111111 11111111		
000290_H	PCN18[R/W] B,H,W 00000000 000000-0		PCSR18[W] H,W XXXXXXXX XXXXXXXX		PPG18
000294_H	PDUT18[W] H,W XXXXXXXX XXXXXXXX		PTMR18[R] H,W 11111111 11111111		
000298_H	PCN19[R/W] B,H,W 00000000 000000-0		PCSR19[W] H,W XXXXXXXX XXXXXXXX		PPG19
$00029C_H$	PDUT19[W] H,W XXXXXXXX XXXXXXXX		PTMR19[R] H,W 11111111 11111111		
$0002A0_H$	PCN20[R/W] B,H,W 00000000 000000-0		PCSR20[W] H,W XXXXXXXX XXXXXXXX		PPG20
$0002A4_H$	PDUT20[W] H,W XXXXXXXX XXXXXXXX		PTMR20[R] H,W 11111111 11111111		
$0002A8_H$	PCN21[R/W] B,H,W 00000000 000000-0		PCSR21[W] H,W XXXXXXXX XXXXXXXX		PPG21
$0002AC_H$	PDUT21[W] H,W XXXXXXXX XXXXXXXX		PTMR21[R] H,W 11111111 11111111		
$0002B0_H$	PCN22[R/W] B,H,W 00000000 000000-0		PCSR22[W] H,W XXXXXXXX XXXXXXXX		PPG22
$0002B4_H$	PDUT22[W] H,W XXXXXXXX XXXXXXXX		PTMR22[R] H,W 11111111 11111111		
$0002B8_H$	PCN23[R/W] B,H,W 00000000 000000-0		PCSR23[W] H,W XXXXXXXX XXXXXXXX		PPG23
$0002BC_H$	PDUT23[W] H,W XXXXXXXX XXXXXXXX		PTMR23[R] H,W 11111111 11111111		
$0002C0_H$	GTRS0[R/W] B,H,W -0000000 -0000000		GTRS1[R/W] B,H,W -0000000 -0000000		PPG Control
$0002C4_H$	GTRS2[R/W] B,H,W -0000000 -0000000		GTRS3[R/W] B,H,W -0000000 -0000000		
$0002C8_H$	GTRS4[R/W] B,H,W -0000000 -0000000		GTRS5[R/W] B,H,W -0000000 -0000000		
$0002CC_H$	GTRS6[R/W] B,H,W -0000000 -0000000		GTRS7[R/W] B,H,W -0000000 -0000000		
$0002D0_H$	GTRS8[R/W] B,H,W -0000000 -0000000		GTRS9[R/W] B,H,W -0000000 -0000000		
$0002D4_H$	GTRS10[R/W] B,H,W -0000000 -0000000		GTRS11[R/W] B,H,W -0000000 -0000000		
$0002D8_H$	GTREN0[R/W] H,W 00000000 00000000		GTREN1[R/W] H,W -------- 00000000		
$0002DC_H$	-		-		Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000588_H | $00058C_H$	-	-	-	-	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H | $00060C_H$	-	-	-	-	Reserved [S]
000610_H | $00063C_H$	-	-	-	-	Reserved [S]
000640_H | $00064C_H$	-	-	-	-	Reserved [S]
000650_H | $00067C_H$	-	-	-	-	Reserved [S]
000680_H | $00068C_H$	-	-	-	-	Reserved [S]
000690_H | $0006BC_H$	-	-	-	-	Reserved [S]
$0006C0_H$ | $0006CC_H$	-	-	-	-	Reserved [S]
$0006D0_H$ | $0006F0_H$	-	-	-	-	Reserved
$0006F4_H$	-				Reserved
$0006F8_H$ | $0006FC_H$	-	-	-	-	Reserved
000700_H	-				Reserved
000704_H | $00070C_H$	-	-	-	-	Reserved
000710_H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	-	Bus performance counter
000714_H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00126C_H$	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		12-bit A/D converter
001270_H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
001274_H	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
001278_H	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
$00127C_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
001280_H	ADTCD14[R] B,H,W 10--0000 00000000		ADTCD15[R] B,H,W 10--0000 00000000		
001284_H	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
001288_H	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
$00128C_H$	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
001290_H	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
001294_H	-	-	-	-	
001298_H	-	-	-	-	
$00129C_H$	-	-	-	-	
$0012A0_H$	-	-	-	-	
$0012A4_H$	ADCS0[R/W] B,H,W 0------- --------		ADCH0[R] B,H,W -----000	ADMD0[R/W] B,H,W ----0000	
$0012A8_H$	ADCS1[R/W] B,H,W 0------- --------		ADCH1[R] B,H,W -----000	ADMD1[R/W] B,H,W ----0000	
$0012AC_H$	ADCS2[R/W] B,H,W 0------- --------		ADCH2[R] B,H,W -----000	ADMD2[R/W] B,H,W ----0000	
$0012B0_H$ | $0012FC_H$	-	-	-	-	Reserved
001300_H	RDCCTR0[R/W] B,H,W 0----000	RDCCTR1[R/W] B,H,W -0000000	RDCINTR[R] B,H,W -0000000	RDCICER[R/W] B,H,W ------00	RDC
001304_H	-	RDCCTR2[R/W] B,H,W ---00000	RDCIPR[R/W] H,W ----0000 00000000		
001308_H	RDCCPR1[R/W] H,W ----0000 00000000		RDCCPR2[R/W] H,W ----0000 00000000		
$00130C_H$	RDCCPR3[R/W] H,W ------00 00000000		RDCCPR4[R/W] H,W ------00 00000000		
001310_H	AGLDR[R] H,W 1---XXXX XXXXXXXX		AGVLDR[R] H,W XXXXXXXX XXXXXXXX		
001314_H	AGLDBR[R] H,W 1---XXXX XXXXXXXX		AGVLDBR[R] H,W XXXXXXXX XXXXXXXX		
001318_H	SCCIR[R/W] H,W 1---0000 00000000		-	-	
$00131C_H$	SINDR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0002E0_H$	-	GATEC0[R/W] B,H,W ------00	-	GATEC2[R/W] B,H,W ------00	PPG GATE Control
$0002E4_H$	-	GATEC4[R/W] B,H,W ------00	-	GATEC8[R/W] B,H,W ------00	
$0002E8_H$	-	GATEC10[R/W] B,H,W ------00	-	GATEC12[R/W] B,H,W ------00	
$0002EC_H$	-	-	-	-	Reserved
$0002F0_H$	RCRH0[W] H,W 00000000	RCRL0[W] B,H,W 00000000	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	U/D counter 0
$0002F4_H$	CCR0[R/W] B,H 00000000 -0001000		-	CSR0[R] B 00000000	
$0002F8_H$	RCRH1[W] H,W 00000000	RCRL1[W] B,H,W 00000000	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	U/D counter 1
$0002FC_H$	CCR1[R/W] B,H 00000000 -0001000		-	CSR1[R] B 00000000	
000300_H	-				Reserved
000304_H	-	-	-	-	Reserved
000308_H	-				Reserved
$00030C_H$	-	-	-	-	
000310_H	-	-	MPUCR[R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	-	-	-	-	
000318_H	-				
$00031C_H$	-	-	-		
000320_H	DPVAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	-	-	DPVSR[R/W] H -------- 00000--0		
000328_H	DEAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	-	-	DESR[R/W] H -------- 00000--0		
000330_H	PABR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	-	-	PACR0[R/W] H 000000-0 00000--0		
000338_H	PABR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	-	-	PACR1[R/W] H 000000-0 00000--0		
000340_H	PABR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	-	-	PACR2[R/W] H 000000-0 00000--0		
000348_H	PABR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	-	-	PACR3[R/W] H 000000-0 00000--0		
000350_H	PABR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000354_H	-	-	PACR4[R/W] H 000000-0 00000--0		MPU [S] (Only the CPU can access this area)
000358_H	PABR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	-	-	PACR5[R/W] H 000000-0 00000--0		
000360_H	PABR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	-	-	PACR6[R/W] H 000000-0 00000--0		
000368_H	PABR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	-	-	PACR7[R/W] H 000000-0 00000--0		
000370_H	-				Reserved [S]
000374_H	-	-	-		
000378_H	-				
$00037C_H$	-	-	-		
000380_H	-				
000384_H	-	-	-		
000388_H	-				
$00038C_H$	-	-	-		
000390_H	-				
000394_H	-	-	-		Reserved [S]
000398_H	-				
$00039C_H$	-	-	-		
$0003A0_H$	-				
$0003A4_H$	-	-	-		
$0003A8_H$	-				
$0003AC_H$	-	-	-		
$0003B0_H$ | $0003FC_H$	-	-	-	-	Reserved [S]
000400_H	ICSEL0[R/W] B,H,W -----000	ICSEL1[R/W] B,H,W -------0	ICSEL2[R/W] B,H,W -------0	ICSEL3[R/W] B,H,W -------0	Generation and clearing of DMA transfer requests
000404_H	ICSEL4[R/W] B,H,W -------0	ICSEL5[R/W] B,H,W -------0	ICSEL6[R/W] B,H,W -------0	ICSEL7[R/W] B,H,W -----000	
000408_H	ICSEL8[R/W] B,H,W -------0	ICSEL9[R/W] B,H,W -------0	ICSEL10[R/W] B,H,W -----000	ICSEL11[R/W] B,H,W -----000	
$00040C_H$	ICSEL12[R/W] B,H,W -----000	ICSEL13[R/W] B,H,W -----000	ICSEL14[R/W] B,H,W -----000	ICSEL15[R/W] B,H,W -------0	
000410_H	ICSEL16[R/W] B,H,W -------0	ICSEL17[R/W] B,H,W -------0	ICSEL18[R/W] B,H,W -------0	ICSEL19[R/W] B,H,W -------0	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0006D0_H$ | $0006F0_H$	-	-	-	-	Reserved
$0006F4_H$	-				Reserved
$0006F8_H$ | $0006FC_H$	-	-	-	-	Reserved
000700_H	-				Reserved
000704_H | $00070C_H$	-	-	-	-	Reserved
000710_H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	-	Bus performance counter
000714_H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720_H | $0007F8_H$	-	-	-	-	Reserved
$0007FC_H$	BMODR[R] B,H,W XXXXXXXX	-	-	-	Operation mode
000800_H | $00083C_H$	-	-	-	-	Reserved [S]
000840_H	FCTLR[R/W] H -0--1000 0--0----		-	FSTR[R/W] B -----001	Flash memory register [S]
000844_H	-	-	-	-	Reserved [S]
000848_H | 000854_H	-	-	-	-	Reserved [S]
000858_H	-	-	WREN[R/W] H 00000000 00000000		Wild register [S]
$00085C_H$ | $00087C_H$	-	-	-	-	Reserved [S]
000880_H	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884_H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00110C_H$	CPCLRB1/CPCLR1[R/W] H,W 11111111 11111111		TCDT1[R/W] H,W 00000000 00000000		Free-run timer 1
001110_H	TCCS1[R/W] B,H,W 00000000 01000000 ----0000 --------				
001114_H	CPCLRB2/CPCLR2[R/W] H,W 11111111 11111111		TCDT2[R/W] H,W 00000000 00000000		Free-run timer 2
001118_H	TCCS2[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00111C_H$	CPCLRB3/CPCLR3[R/W] H,W 11111111 11111111		TCDT3[R/W] H,W 00000000 00000000		Free-run timer 3
001120_H	TCCS3[R/W] B,H,W 00000000 01000000 ----0000 --------				
001124_H	CPCLRB4/CPCLR4[R/W] H,W 11111111 11111111		TCDT4[R/W] H,W 00000000 00000000		Free-run timer 4
001128_H	TCCS4[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00112C_H$	CPCLRB5/CPCLR5[R/W] H,W 11111111 11111111		TCDT5[R/W] H,W 00000000 00000000		Free-run timer 5
001130_H	TCCS5[R/W] B,H,W 00000000 01000000 ----0000 --------				
001134_H	FRS0[R/W] B,H,W -------- -000-000 -000-000 -000-000				Free-run timer selection
001138_H	FRS1[R/W] B,H,W -------- -------- -000-000 -000-000				
$00113C_H$	FRS2[R/W] B,H,W -------- -000-000 -000-000 -000-000				
001140_H	FRS3[R/W] B,H,W -------- -------- -000-000 -000-000				
001144_H	FRS4[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001148_H	FRS5[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
$00114C_H$	FRS6[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001150_H	-				
001154_H	OCCPB0/OCCP0[R/W] H,W 00000000 00000000		OCCPB1/OCCP1[R/W] H,W 00000000 00000000		Output compare 0/1
001158_H	OCS01[R/W] B,H,W -110--00 00001100		-	OCMOD01[R/W] B,H,W ------00	
$00115C_H$	OCCPB2/OCCP2[R/W] H,W 00000000 00000000		OCCPB3/OCCP3[R/W] H,W 00000000 00000000		Output compare 2/3
001160_H	OCS23[R/W] B,H,W -110--00 00001100		-	OCMOD23[R/W] B,H,W ------00	
001164_H	OCCPB4/OCCP4[R/W] H,W 00000000 00000000		OCCPB5/OCCP5[R/W] H,W 00000000 00000000		Output compare 4/5
001168_H	OCS45[R/W] B,H,W -110--00 00001100		-	OCMOD45[R/W] B,H,W ------00	
$00116C_H$	OCCPB6/OCCP6[R/W] H,W 00000000 00000000		OCCPB7/OCCP7[R/W] H,W 00000000 00000000		Output compare 6/7
001170_H	OCS67[R/W] B,H,W -110--00 00001100		-	OCMOD67[R/W] B,H,W ------00	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00300C_H$	TEAR0X[R] B,H,W 000----- -------- -0000000 00000000				XBS RAM diagnosis register
003010_H	TEAR1X[R] B,H,W 000----- -------- -0000000 00000000				
003014_H	TEAR2X[R] B,H,W 000----- -------- -0000000 00000000				
003018_H	TAEARX[R/W] B,H,W -1011111 11111111		TASARX[R/W] B,H,W -0000000 00000000		
$00301C_H$	TFECRX[R/W] B,H,W ----0000	TICRX[R/W] B,H,W ----0000	TTCRX[R/W] B,H,W ------00 00001100		
003020_H	TSRCRX[R/W] B,H,W 0-------	-	-	TKCCRX[R/W] B,H,W 00----00	
003024_H	SEEARA[R] B,H,W --000000 00000000		DEEARA[R] B,H,W --000000 00000000		Backup RAM ECC control register
003028_H	EECSRA[R/W] B,H,W ----00-0	-	EFEARA[R/W] B,H,W --000000 00000000		
$00302C_H$	-	EFECRA[R/W] B,H,W -------0 00000000 00000000			
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				Backup RAM diagnosis register
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA[R/W] B,H,W ----0000	TICRA[R/W] B,H,W ----0000	TTCRA[R/W] B,H,W ------00 00001100		
003044_H	TSRCRA[R/W] B,H,W 0-------	-	-	TKCCRA[R/W] B,H,W 00----00	
003048_H | $0030FC_H$	-	-	-	-	Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114_H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
$00311C_H$	-				
003120_H	BUSADR3[R] W 00000000 00000000 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003124_H	BUSADR4[R] W 00000000 00000000 00000000 00000000				Bus diagnosis
003128_H | $003FFC_H$	-	-	-	-	Reserved
004000_H | $005FFC_H$	Backup RAM				Backup RAM area
006000_H | $00CFFC_H$	-	-	-	-	Reserved
$00D000_H$	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF
$00D004_H$	CIF1[R/W] W 00000000 -------0 -0000000 --------				
$00D008_H$ | $00D00C_H$	-	-	-	-	Reserved
$00D010_H$	-				FlexRay GIF
$00D014_H$	-				
$00D018_H$	-	-	-	-	
$00D01C_H$	LCK[R/W] W -------- -------- -------- 00000000				
$00D020_H$	EIR[R/W] W -----000 -----000 ----0000 00000000				FlexRay INT
$00D024_H$	SIR[R/W] W ------00 ------00 00000000 00000000				
$00D028_H$	EILS[R/W] W -----000 -----000 ----0000 00000000				
$00D02C_H$	SILS[R/W] W ------11 ------11 11111111 11111111				
$00D030_H$	EIES[R/W] W -----000 -----000 ----0000 00000000				
$00D034_H$	EIER[R/W] W -----000 -----000 ----0000 00000000				
$00D038_H$	SIES[R/W] W ------00 ------00 00000000 00000000				
$00D03C_H$	SIER[R/W] W ------00 ------00 00000000 00000000				
$00D040_H$	ILE[R/W] W -------- -------- -------- ------00				
$00D044_H$	T0C[R/W] W --000000 00000000 -0000000 ------00				
$00D048_H$	T1C[R/W] W --000000 00000010 -------- ------00				
$00D04C_H$	STPW1[R/W] W --000000 00000000 --000000 -0000000				
$00D050_H$	STPW2[R] W -----000 00000000 -----000 00000000				
$00D054_H$ | $00D07C_H$	-	-	-	-	Reserved

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OL}=2.0mA	0	-	0.4	V	
	V_{OL2}	P003 to P007, P010	Vcc=4.5V I_{OL}=4.0mA	0	-	0.4	V	When FlexRay is selected
	V_{OL3}	P000 to P002, P011 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OL}=5.0mA	0	-	0.4	V	
	V_{OL4}	P001,P002, P021,P022, P025,P026, P073,P074, P076,P077, P127,P130	Vcc=4.5V I_{OL}=3.0mA	0	-	0.4	V	I^2C shared pin (when I^2C is selected)
	V_{OL5}	DEBUGIF	Vcc=2.7V I_{OL}=25.0mA	0	-	0.25	V	

*: Only available with MB91F585LB/F586LB/F587LB, MB91F585LD/F586LD/F587LD

(3) Power-on Conditions

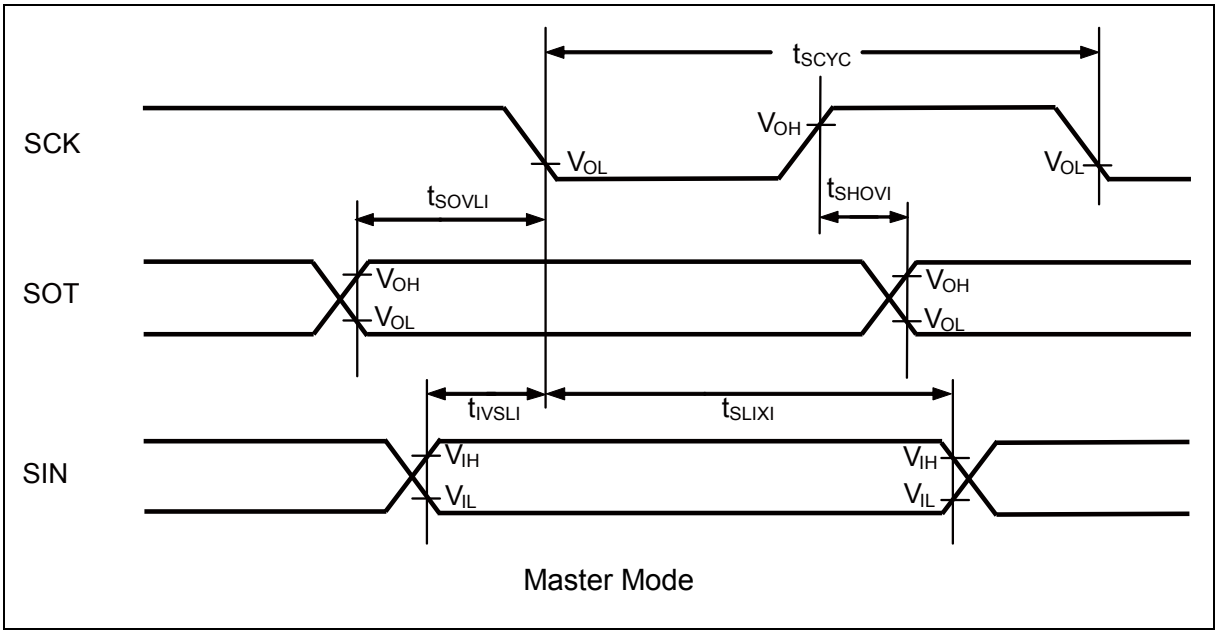
(T_A: Recommended operating conditions, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC5	-	2.1	2.3	2.5	V	When turning on power
Level detection hysteresis width	-	VCC5	-	-	-	125	mV	During voltage drop
Level detection time	-	-	-	-	-	30	µs	*1
Slope detection undetected standard	-	VCC5	V_{CC}= at level detection release level	-	-	4	mV/µs	*2
Power off time	t_{OFF}	VCC5	-	50	-	-	ms	*3

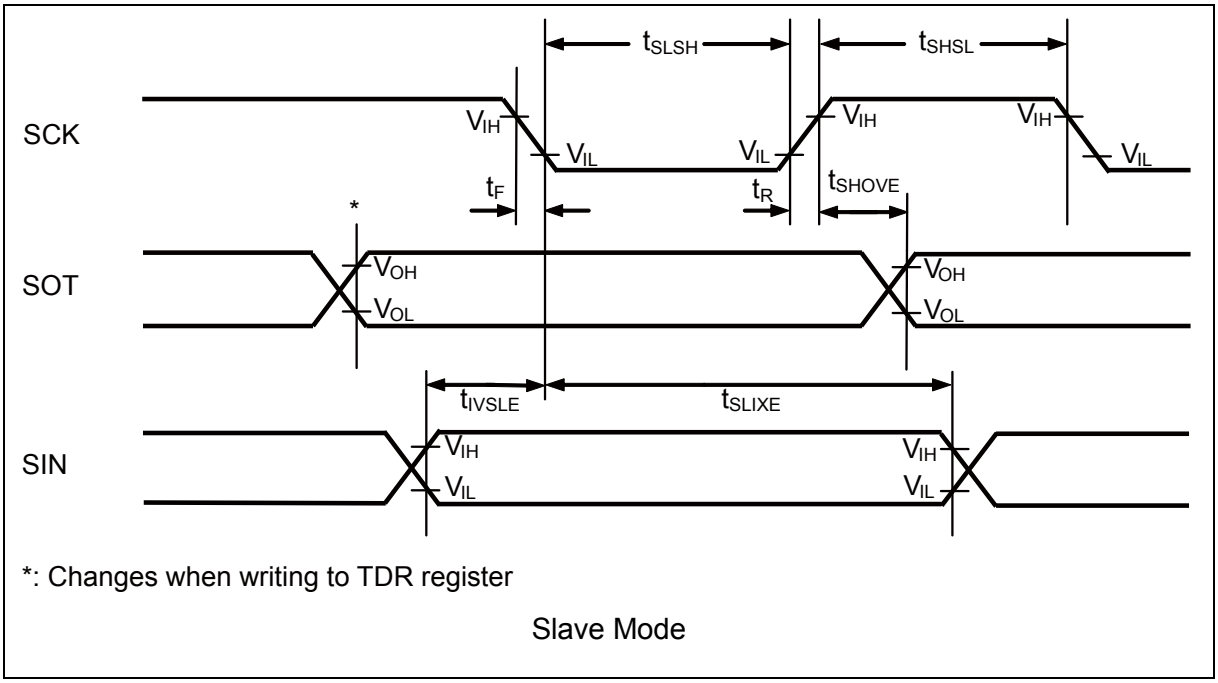
*1: If the fluctuation of the power supply is faster than the low-voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.

*3: This time is to start the slope detection at next power on after power down and internal charge loss.

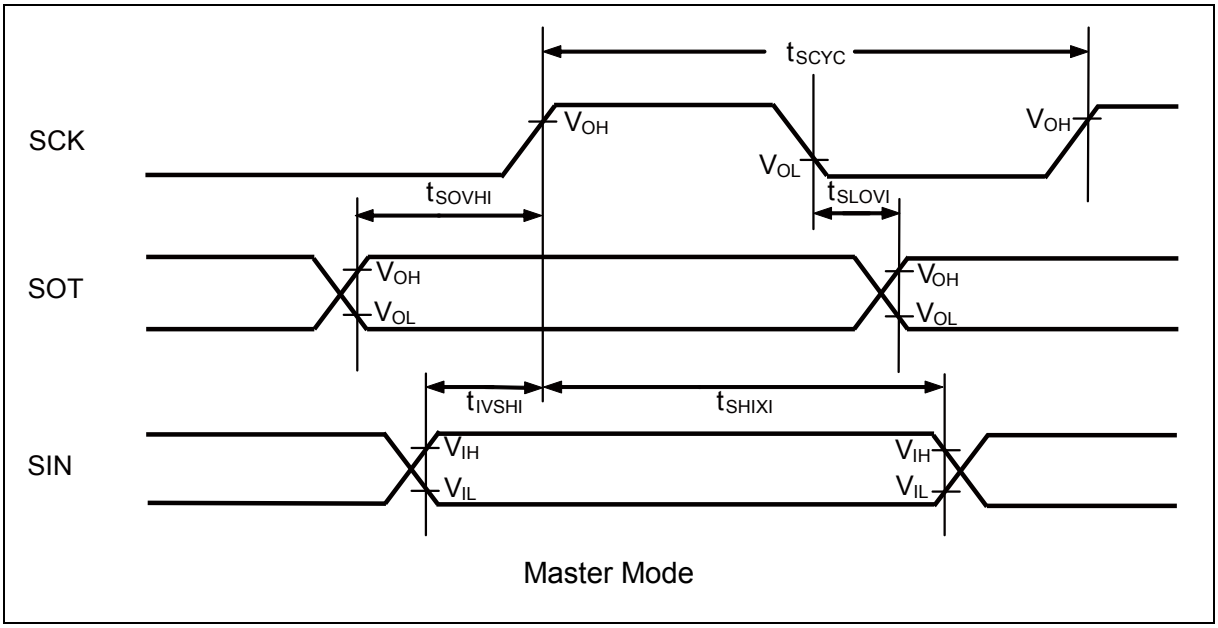


Master Mode

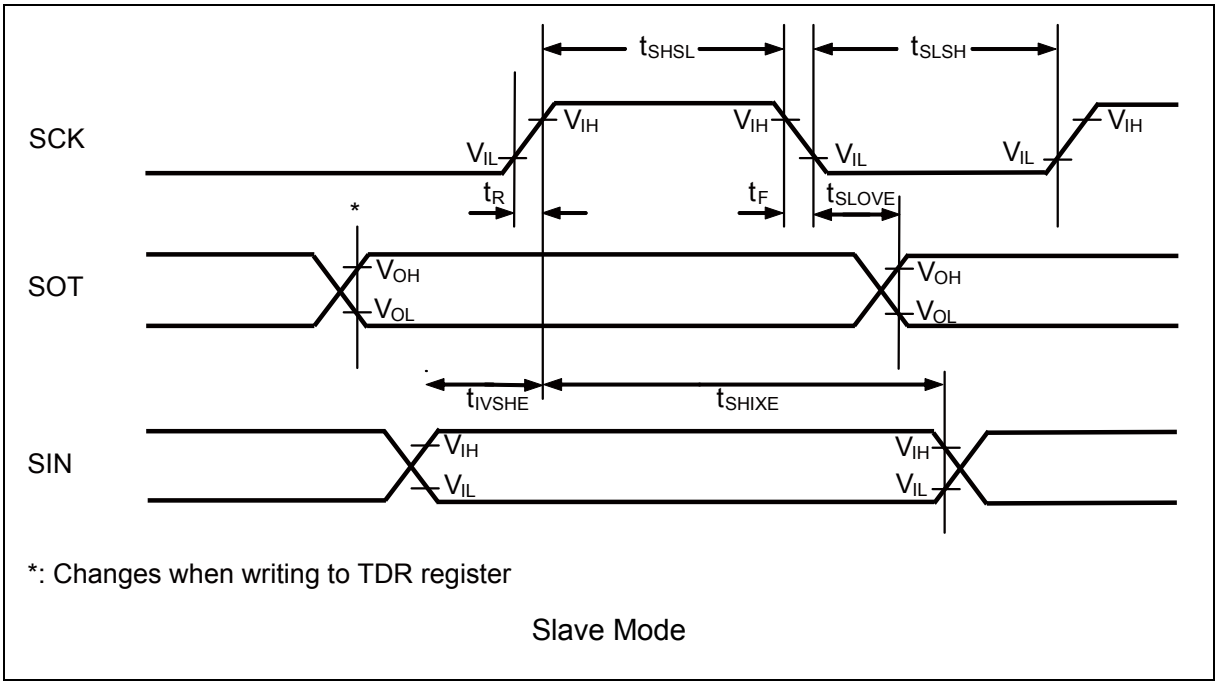


*: Changes when writing to TDR register

Slave Mode



Master Mode



*: Changes when writing to TDR register

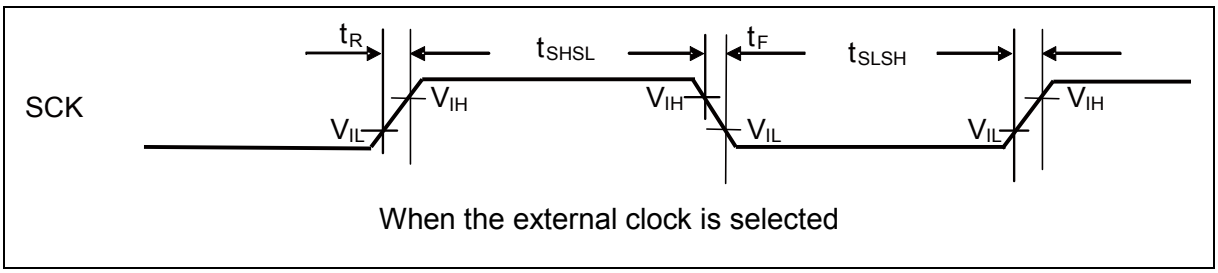
Slave Mode

(4-2) UART (Async Serial Interface) timing (SMR:MD2-0="000"b, "001"b)

(4-2-1) When the external clock is selected (BGR:EXT=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK3_1,SCK4_1	C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



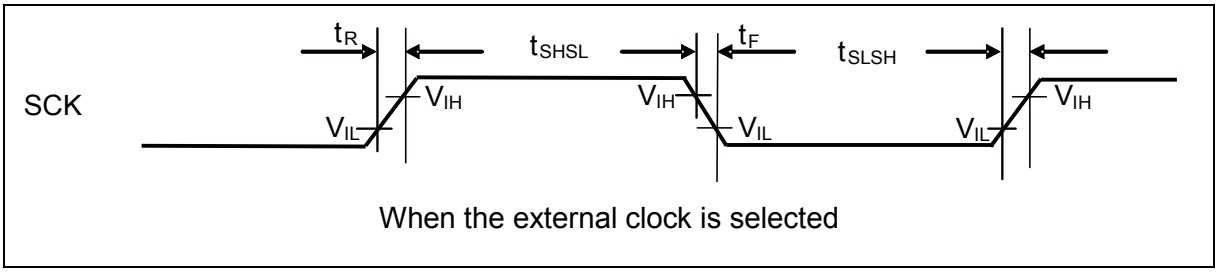
When the external clock is selected

(4-3) LIN interface (v2.1) (LIN Communication Control Interface (v2.1)) timing (SMR:MD2-0="011"b)

(4-3-1) When the external clock is selected (BGR:EXT=1)

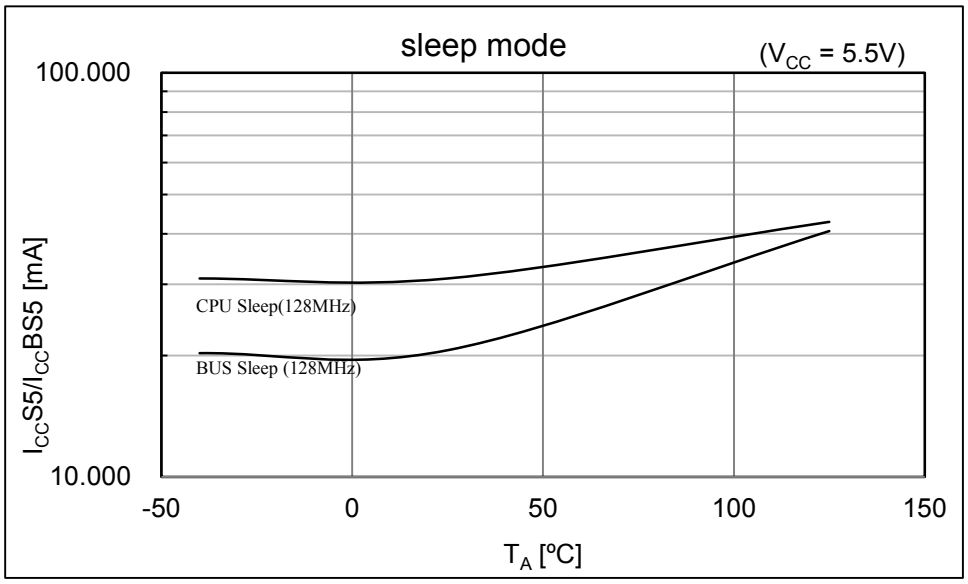
(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK3_1,SCK4_1	C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When the external clock is selected

- MB91F585LA/F586LA/F587LA/F585LB/F586LB/F587LB/ F585LC/F586LC/F587LC/F585LD/F586LD/F587LD



■ ORDERING INFORMATION

Part number	Package*
MB91F585LAPMC-GTE1 MB91F586LAPMC-GTE1 MB91F587LAPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F585LBPMC-GTE1 MB91F586LBPMC-GTE1 MB91F587LBPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F585LCPMC-GTE1 MB91F586LCPMC-GTE1 MB91F587LCPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F585LDPMC-GTE1 MB91F586LDPMC-GTE1 MB91F587LDPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)

*: For details of the package, see "■ PACKAGE DIMENSIONS ".

Colophon

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