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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	98
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f586lcpmc-gtk5e1

Notice On Data Sheet Designations

Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

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> "This document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or VIO range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local sales office.

MB91580L Series

32-bit Microcontroller
FR Family FR81S
MB91F585LA/F585LB/F585LC/F585LD/
MB91F586LA/F586LB/F586LC/F586LD/
MB91F587LA/F587LB/F587LC/F587LD

Data Sheet (Full Production)

■ DESCRIPTION

This series has Spansion 32-bit microcontrollers for automobile motor control. They use the FR81S CPU that is compatible with the FR family.

Note: FR is a line of products of Spansion Inc.

■ FEATURES

- FR81S CPU Core
  - 32-bit RISC, load/store architecture, pipeline 5-stage structure
  - Maximum operating frequency: 128MHz (Source oscillation= 4.0MHz, 32 multiplied (PLL clock multiplication system))
  - General-purpose register: 32 bits, 16 sets
  - 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
  - Instructions appropriate to embedded applications
    - Memory-to-memory transfer instructions
    - Bit manipulation instructions
    - Barrel shift instructions
  - High-level language support instructions
    - Function entry/exit instructions
    - Register content multi-load and store instructions
  - Bit search instructions
    Logical 1 detection, 0 detection, and change-point detection
  - Branch instructions with delay slot
    Overhead decrement during branch process
  - Register interlock function
    Easy assembler writing
  - Built-in multiplier and instruction level support
    - Signed 32-bit multiplication: 5 cycles
    - Signed 16-bit multiplication: 3 cycles

Spansion provides information facilitating product development via the following website.
The website contains information useful for customers.

http://www.spansion.com/Support/microcontrollers/

Publication Number MB91F587LA_DS705-00012 Revision 2.0 Issue Date August 22, 2014

This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur.

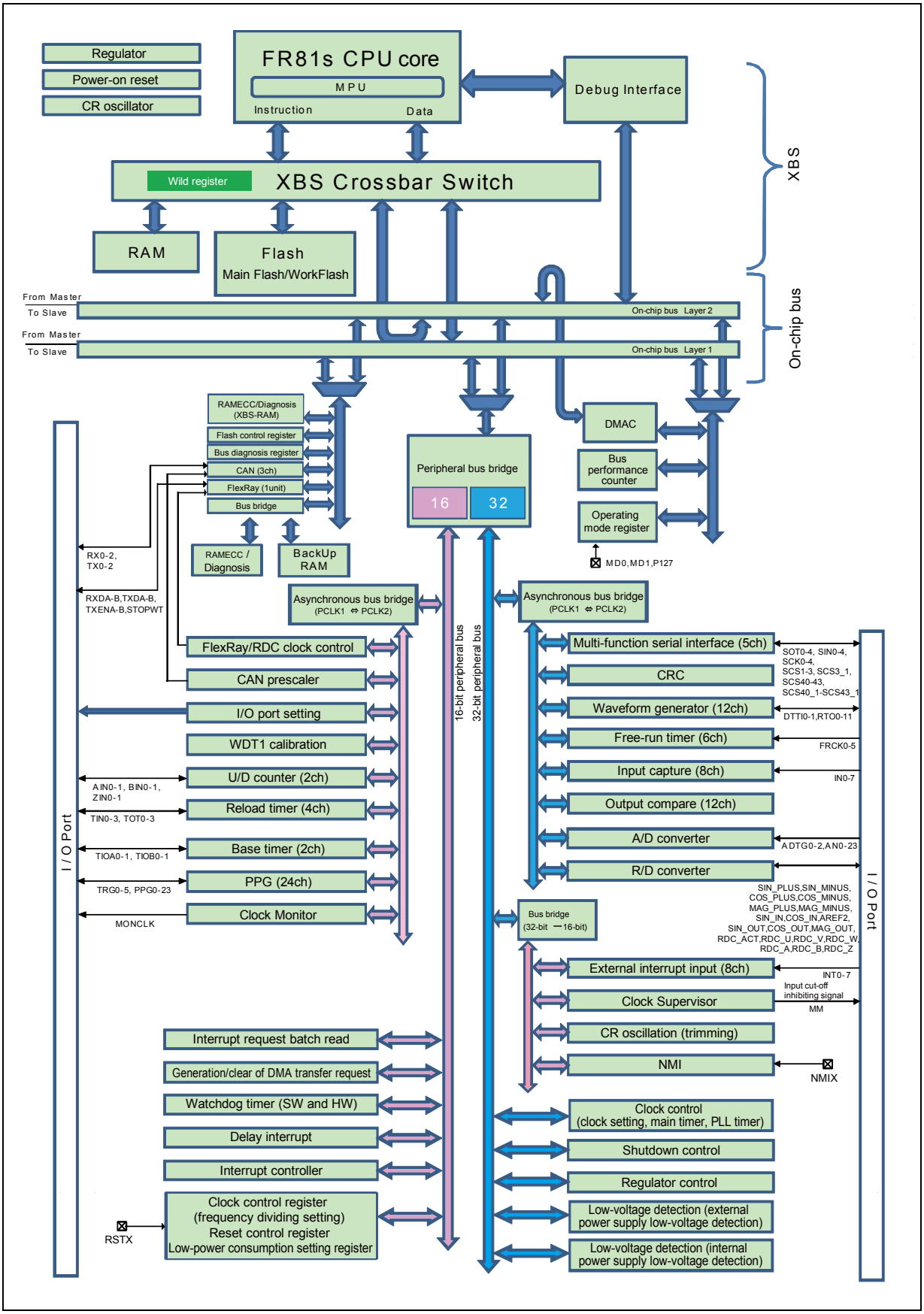
Pin No.	Pin name	I/O circuit type*	Function
96	P110	D	General-purpose I/O port
	TX1		CAN transmission data 1 output pin
97	P111	E	General-purpose I/O port
	RX1		CAN reception data 1 input pin
	INT1		INT1 external interrupt input pin
98	P112	D	General-purpose I/O port
	RTO0		Waveform generator ch.0 output pin
	PPG16		PPG ch.16 output pin
99	P113	D	General-purpose I/O port
	RTO1		Waveform generator ch.1 output pin
	PPG17		PPG ch.17 output pin
100	P114	D	General-purpose I/O port
	RTO2		Waveform generator ch.2 output pin
	PPG18		PPG ch.18 output pin
101	P115	D	General-purpose I/O port
	RTO3		Waveform generator ch.3 output pin
	PPG19		PPG ch.19 output pin
102	P116	D	General-purpose I/O port
	RTO4		Waveform generator ch.4 output pin
	PPG20		PPG ch.20 output pin
103	P117	D	General-purpose I/O port
	RTO5		Waveform generator ch.5 output pin
	PPG21		PPG ch.21 output pin
104	P120	D	General-purpose I/O port
	RTO6		Waveform generator ch.6 output pin
	PPG22		PPG ch.22 output pin
105	P121	D	General-purpose I/O port
	RTO7		Waveform generator ch.7 output pin
	PPG23		PPG ch.23 output pin
106	P122	D	General-purpose I/O port
	RTO8		Waveform generator ch.8 output pin
107	P123	D	General-purpose I/O port
	RTO9		Waveform generator ch.9 output pin
111	P124	D	General-purpose I/O port
	RTO10		Waveform generator ch.10 output pin
112	P125	D	General-purpose I/O port
	RTO11		Waveform generator ch.11 output pin
113	P126	E	General-purpose I/O port
	SIN0		Multi-function serial ch.0 serial data input pin
	INT6		INT6 external interrupt input pin
114	P127	K	General-purpose I/O port
	SOT0		Multi-function serial ch.0 serial data output pin/ I^2C ch.0 serial data I/O pin (SDA)
115	P130	K	General-purpose I/O port
	SCK0		Multi-function serial ch.0 clock I/O pin/ I^2C ch.0 clock I/O pin (SCL)

Pin No.	Pin name	I/O circuit type*1	Function
124	P131	D	General-purpose I/O port
	ADTG0		A/D converter ch.0 to ch.7 external trigger input pin
125	P132	D	General-purpose I/O port
	ADTG1		A/D converter ch.8 to ch.15 external trigger input pin
	SCS1		Multi-function serial ch.1 serial chip select I/O pin
126	P133	D	General-purpose I/O port
	ADTG2		A/D converter ch.16 to ch.23 external trigger input pin
	TX2		CAN transmission data 2 output pin
127	P134	E	General-purpose I/O port
	STOPWT		FlexRay Stopwatch input pin
	RX2		CAN reception data 2 input pin
	INT7		INT7 external interrupt input pin
	IN7		16-bit input capture ch.7 external pulse input pin
110	DEBUGIF	L	DEBUG I/F pin
121	P136	D	General-purpose I/O port
	DTTI0		Waveform generator output stop signal input pin 0
	MONCLK		Clock monitor output pin
122	P137	D	General-purpose I/O port
	DTTI1		Waveform generator output stop signal input pin 1
40	AVCC0	-	*2
84	AVCC3	-	A/D converter analog power supply
42	AVRH0	-	*2
52	AVRH1	-	A/D converter upper limit reference voltage
62	AVRH2	-	A/D converter upper limit reference voltage
83	AVRH3	-	A/D converter upper limit reference voltage
43	AVSS0	-	*3
	AVRL0		*3
53	AVSS1	-	A/D converter GND
	AVRL1		A/D converter lower limit reference voltage
63	AVSS2	-	A/D converter GND
	AVRL2		A/D converter lower limit reference voltage
82	AVSS3	-	A/D converter GND
	AVRL3		A/D converter lower limit reference voltage
130	C	-	External capacity connection output pin
18, 36, 93, 72, 109, 128, 144	VCC5	-	+5.0V power supply
1, 19, 37, 73, 94, 108, 120, 129	VSS	-	GND

*1: For the I/O circuit types, see "■ I/O circuit type".
*2: The MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD do not use this pin. Connect it with the VCC5 pin.
*3: The MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD do not use this pin. Connect it with the VSS pin.

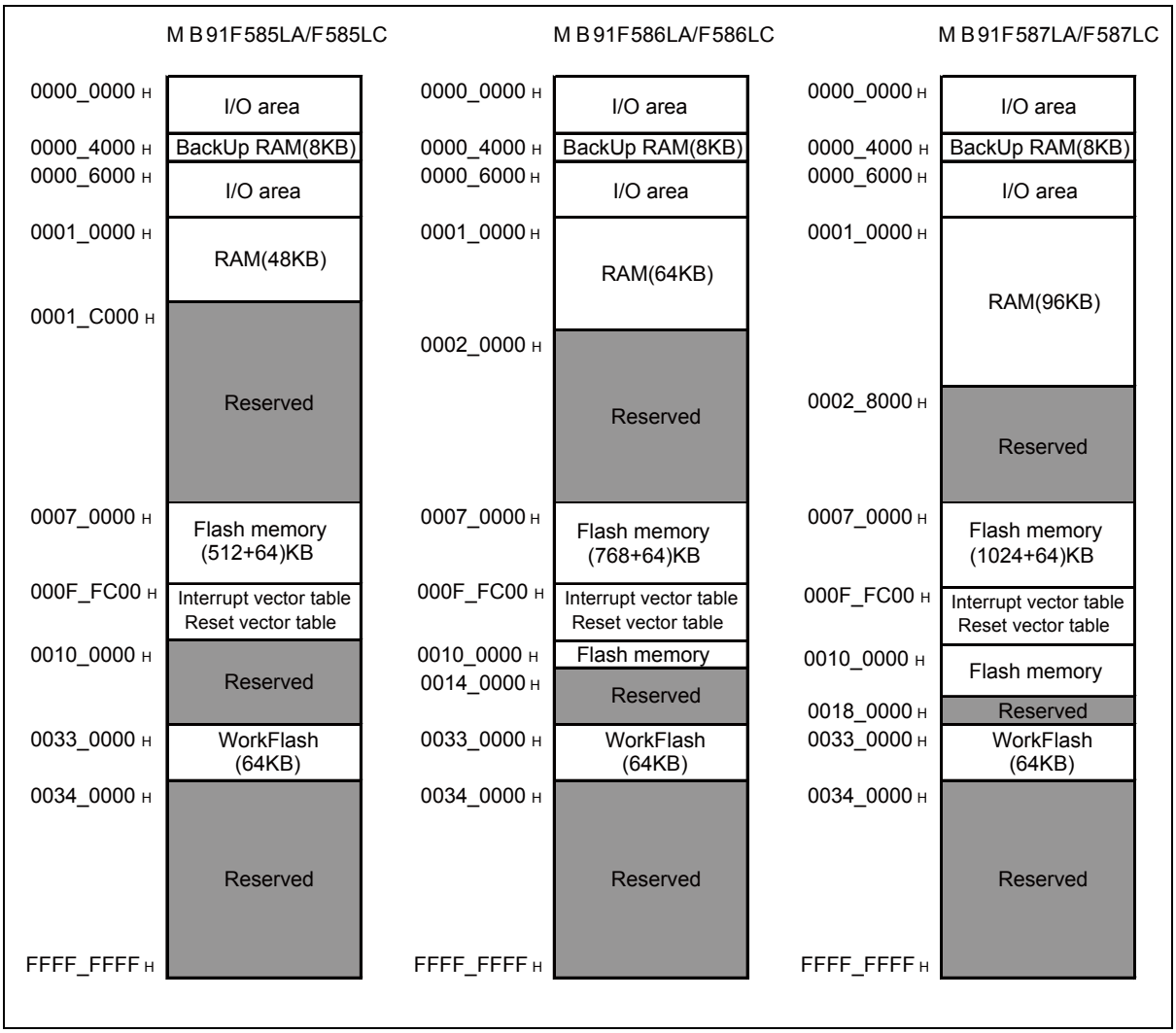
■ BLOCK DIAGRAM

• MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC



■ MEMORY MAP

- MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC



- MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000000_H	PDR00[R/W] B,H,W XXXXXXXX	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register
000004_H	PDR04[R/W] B,H,W -----XXX	-	PDR06[R/W] B,H,W XXXXXXXX	PDR07[R/W] B,H,W XXXXXXXX	
000008_H	PDR08[R/W] B,H,W XXXXXXXX	PDR09[R/W] B,H,W XXXXXXXX	PDR10[R/W] B,H,W XXXXXXXX	PDR11[R/W] B,H,W XXXXXXXX	
$00000C_H$	PDR12[R/W] B,H,W XXXXXXXX	PDR13[R/W] B,H,W XX-XXXXX	-	-	
000010_H | 000038_H	-	-	-	-	Reserved
$00003C_H$	WDTCR0[R/W] B,H,W -0--0000	WDTCPR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ----0010	WDTCPR1[W] B,H,W 00000000	Watchdog timer [S]
000040_H	-	-	-		Reserved
000044_H	DICR[R/W] B -------0	-	-	-	Delay interrupt
000048_H | $00005C_H$	-		-		Reserved
000060_H	TMRLRA0[R/W] H XXXXXXXX XXXXXXXX		TMR0[R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064_H	TMRLRB0[R/W] H XXXXXXXX XXXXXXXX		TMCSR0[R/W] B,H,W 00000000 0-000000		
000068_H | $00007C_H$	-	-	-	-	Reserved
000080_H	BT0TMR[R] H 00000000 00000000		BT0TMCR[R/W] H -0000000 00000000		Base timer 0
000084_H	BT0TMCR2[R/W] B -------0	BT0STC[R/W] B -0-0-0-0	-	-	
000088_H	BT0PCSR/BT0PRLL[R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
$00008C_H$	-	-	-	-	
000090_H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W] H -0000000 00000000		Base timer 1
000094_H	BT1TMCR2[R/W] B -------0	BT1STC[R/W] B -0-0-0-0	-	-	
000098_H	BT1PCSR/BT1PRLL[R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF[R/W] H 00000000 00000000		
$00009C_H$	BTSEL01[R/W] B ----0000	-	BTSSSR[W] B,H -------- ------11		Base timer 0,1

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000588_H | $00058C_H$	-	-	-	-	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H | $00060C_H$	-	-	-	-	Reserved [S]
000610_H | $00063C_H$	-	-	-	-	Reserved [S]
000640_H | $00064C_H$	-	-	-	-	Reserved [S]
000650_H | $00067C_H$	-	-	-	-	Reserved [S]
000680_H | $00068C_H$	-	-	-	-	Reserved [S]
000690_H | $0006BC_H$	-	-	-	-	Reserved [S]
$0006C0_H$ | $0006CC_H$	-	-	-	-	Reserved [S]
$0006D0_H$ | $0006F0_H$	-	-	-	-	Reserved
$0006F4_H$	-				Reserved
$0006F8_H$ | $0006FC_H$	-	-	-	-	Reserved
000700_H	-				Reserved
000704_H | $00070C_H$	-	-	-	-	Reserved
000710_H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	-	Bus performance counter
000714_H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000E00_H$	DDR00[R/W] B,H 00000000	DDR01[R/W] B,H 00000000	DDR02[R/W] B,H 00000000	DDR03[R/W] B,H 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H -----000	-	DDR06[R/W] B,H 00000000	DDR07[R/W] B,H 00000000	
$000E08_H$	DDR08[R/W] B,H 00000000	DDR09[R/W] B,H 00000000	DDR10[R/W] B,H 00000000	DDR11[R/W] B,H 00000000	
$000E0C_H$	DDR12[R/W] B,H 00000000	DDR13[R/W] B,H 00-00000	-	-	
$000E10_H$ | $000E1C_H$	-	-	-	-	Reserved
$000E20_H$	PFR00[R/W] B,H 00000000	PFR01[R/W] B,H 00000000	PFR02[R/W] B,H 00000000	PFR03[R/W] B,H 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H -----000	-	PFR06[R/W] B,H 00000000	PFR07[R/W] B,H 00000000	
$000E28_H$	PFR08[R/W] B,H 00000000	PFR09[R/W] B,H 00000000	PFR10[R/W] B,H 00000000	PFR11[R/W] B,H 00000000	
$000E2C_H$	PFR12[R/W] B,H 00000000	PFR13[R/W] B,H 00-00000	-	-	
$000E30_H$ | $000E3C_H$	-	-	-	-	Reserved
$000E40_H$	PDDR00[R] B,H,W XXXXXXXX	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
$000E44_H$	PDDR04[R] B,H,W -----XXX	-	PDDR06[R] B,H,W XXXXXXXX	PDDR07[R] B,H,W XXXXXXXX	
$000E48_H$	PDDR08[R] B,H,W XXXXXXXX	PDDR09[R] B,H,W XXXXXXXX	PDDR10[R] B,H,W XXXXXXXX	PDDR11[R] B,H,W XXXXXXXX	
$000E4C_H$	PDDR12[R] B,H,W XXXXXXXX	PDDR13[R] B,H,W XX-XXXXX	-	-	
$000E50_H$ | $000E5C_H$	-	-	-	-	Reserved
$000E60_H$	EPFR00[R/W] B,H -----000	EPFR01[R/W] B,H ------00	EPFR02[R/W] B,H --000000	EPFR03[R/W] B,H 00000000	Extended port function register
$000E64_H$	EPFR04[R/W] B,H 00000000	EPFR05[R/W] B,H 00000000	EPFR06[R/W] B,H ------00	EPFR07[R/W] B,H ----0000	
$000E68_H$	EPFR08[R/W] B,H ----0000	EPFR09[R/W] B,H -------0	EPFR10[R/W] B,H 00000000	EPFR11[R/W] B,H ----0000	
$000E6C_H$	EPFR12[R/W] B,H --000000	EPFR13[R/W] B,H -------1	EPFR14[R/W] B,H -0000000	EPFR15[R/W] B,H -0000000	
$000E70_H$	EPFR16[R/W] B,H --000000	EPFR17[R/W] B,H 00000000	EPFR18[R/W] B,H 00000000	EPFR19[R/W] B,H 00000000	
$000E74_H$	EPFR20[R/W] B,H 00000000	EPFR21[R/W] B,H 00000000	EPFR22[R/W] B,H 00000000	EPFR23[R/W] B,H 00000000	
$000E78_H$	EPFR24[R/W] B,H 00000000	EPFR25[R/W] B,H 00000000	EPFR26[R/W] B,H 00000000	EPFR27[R/W] B,H 00000000	
$000E7C_H$	EPFR28[R/W] B,H 00000000	EPFR29[R/W] B,H 00000000	EPFR30[R/W] B,H 00000000	EPFR31[R/W] B,H 00000000	
$000E80_H$	EPFR32[R/W] B,H 00000000	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001524_H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000000-0	SSR1[R/W] B,H,W 0--00011	ESCR1/(IBSR1) [R/W] B,H,W 00000000	Multi Function Serial I/F 1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001528_H	-/(RDR11/(TDR11))[R/W] H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
$00152C_H$	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001530_H	STMCR1[R/W] B,H,W 00000000 00000000		-/(SCSCR1/SFUR1) [R/W] B,H,W -------- -------- *3,*4		
001534_H	-/(SCSTR31) [R/W] B,H,W -------- *3	-/(SCSTR21) [R/W] B,H,W -------- *3	-/(SCSTR11/SFLR11) [R/W] B,H,W -------- *3,*4	-/(SCSTR01/SFLR01) [R/W] B,H,W -------- *3,*4	
001538_H	-	-	-	-	
$00153C_H$	-	-	-	TBYTE01[R/W] B,H,W 00000000	
001540_H	BGR1[R/W] H,W 00000000 00000000		-/(ISMK1)[R/W] B,H,W -------- *2	-/(ISBA1)[R/W] B,H,W -------- *2	
001544_H	FCR11[R/W] B,H,W 00-00100	FCR01[R/W] B,H,W -0000000	FBYTE21[R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
001548_H	SCR2[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000000-0	SSR2[R/W] B,H,W 0--00011	ESCR2[R/W] B,H,W 00000000	Multi Function Serial I/F 2 *1: Byte access is possible only for access to lower 8 bits. *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
$00154C_H$	-/(RDR12/(TDR12))[R/W] H,W -------- -------- *3		RDR02/(TDR02)[R/W] B,H,W -------0 00000000 *1		
001550_H	SACSR2[R/W] B,H,W 0----000 00000000		STMR2[R] B,H,W 00000000 00000000		
001554_H	STMCR2[R/W] B,H,W 00000000 00000000		-/(SCSCR2/SFUR2) [R/W] B,H,W -------- -------- *3,*4		
001558_H	-/(SCSTR32) [R/W] B,H,W -------- *3	-/(SCSTR22) [R/W] B,H,W -------- *3	-/(SCSTR12/SFLR12) [R/W] B,H,W -------- *3,*4	-/(SCSTR02/SFLR02) [R/W] B,H,W -------- *3,*4	
$00155C_H$	-	-	-	-	
001560_H	-	-	-	TBYTE02[R/W] B,H,W 00000000	
001564_H	BGR2[R/W] H,W 00000000 00000000		-	-	
001568_H	FCR12[R/W] B,H,W 00-00100	FCR02[R/W] B,H,W -0000000	FBYTE22[R/W] B,H,W 00000000	FBYTE12[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$002228_{H,}$ $00222C_H$	-		-		CAN 2 64msb
$002230_{H,}$ 002234_H	Reserved (IF1 data mirror)				
$002238_{H,}$ $00223C_H$	-		-		
002240_H	IF2CREQ2[R/W] B,H,W 0------- 00000001		IF2CMSK2[R/W] B,H,W -------- 00000000		
002244_H	IF2MSK22[R/W] B,H,W 11-11111 11111111		IF2MSK12[R/W] B,H,W 11111111 11111111		
002248_H	IF2ARB22[R/W] B,H,W 00000000 00000000		IF2ARB12[R/W] B,H,W 00000000 00000000		
$00224C_H$	IF2MCTR2[R/W] B,H,W 00000000 0---0000		-		
002250_H	IF2DTA12[R/W] B,H,W 00000000 00000000		IF2DTA22[R/W] B,H,W 00000000 00000000		
002254_H	IF2DTB12[R/W] B,H,W 00000000 00000000		IF2DTB22[R/W] B,H,W 00000000 00000000		
$002258_{H,}$ $00225C_H$	-		-		
$002260_{H,}$ 002264_H	Reserved (IF2 data mirror)				
002268_H | $00227C_H$	-		-		
002280_H	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		
002284_H	TREQR42[R] B,H,W 00000000 00000000		TREQR32[R] B,H,W 00000000 00000000		
002288_H	-		-		
$00228C_H$	-		-		
002290_H	NEWDT22[R] B,H,W 00000000 00000000		NEWDT12[R] B,H,W 00000000 00000000		
002294_H	NEWDT42[R] B,H,W 00000000 00000000		NEWDT32[R] B,H,W 00000000 00000000		
002298_H	-		-		
$00229C_H$	-		-		
$0022A0_H$	INTPND22[R] B,H,W 00000000 00000000		INTPND12[R] B,H,W 00000000 00000000		
$0022A4_H$	INTPND42[R] B,H,W 00000000 00000000		INTPND32[R] B,H,W 00000000 00000000		
$0022A8_H$	-		-		
$0022AC_H$	-		-		
$0022B0_H$	MSGVAL22[R] B,H,W 00000000 00000000		MSGVAL12[R] B,H,W 00000000 00000000		
$0022B4_H$	MSGVAL42[R] B,H,W 00000000 00000000		MSGVAL32[R] B,H,W 00000000 00000000		
$0022B8_H$	-		-		
$0022BC_H$	-		-		
$0022C0_H$ | $0022FC_H$	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D100_H$	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay SUC
$00D104_H$	CCEV[R] W -------- -------- ---00000 00--0000				
$00D108_H$ $00D10C_H$	-				Reserved
$00D110_H$	SCV[R] W -----000 00000000 -----000 00000000				FlexRay GTU
$00D114_H$	MTCCV[R] W -------- --000000 --000000 00000000				
$00D118_H$	RCV[R] W -------- -------- ----0000 00000000				
$00D11C_H$	OCV[R] W -------- -----000 00000000 00000000				
$00D120_H$	SFS[R] W -------- ----0000 00000000 00000000				
$00D124_H$	SWNIT[R] W -------- -------- ----0000 00000000				
$00D128_H$	ACS[R/W] W -------- -------- ---00000 ---00000				
$00D12C_H$	-				
$00D130_H$	ESID1[R] W -------- -------- 00----00 00000000				
$00D134_H$	ESID2[R] W -------- -------- 00----00 00000000				
$00D138_H$	ESID3[R] W -------- -------- 00----00 00000000				
$00D13C_H$	ESID4[R] W -------- -------- 00----00 00000000				
$00D140_H$	ESID5[R] W -------- -------- 00----00 00000000				
$00D144_H$	ESID6[R] W -------- -------- 00----00 00000000				
$00D148_H$	ESID7[R] W -------- -------- 00----00 00000000				
$00D14C_H$	ESID8[R] W -------- -------- 00----00 00000000				
$00D150_H$	ESID9[R] W -------- -------- 00----00 00000000				
$00D154_H$	ESID10[R] W -------- -------- 00----00 00000000				
$00D158_H$	ESID11[R] W -------- -------- 00----00 00000000				
$00D15C_H$	ESID12[R] W -------- -------- 00----00 00000000				
$00D160_H$	ESID13[R] W -------- -------- 00----00 00000000				
$00D164_H$	ESID14[R] W -------- -------- 00----00 00000000				
$00D168_H$	ESID15[R] W -------- -------- 00----00 00000000				
$00D16C_H$	-				
$00D170_H$	OSID1[R] W -------- -------- 00----00 00000000				

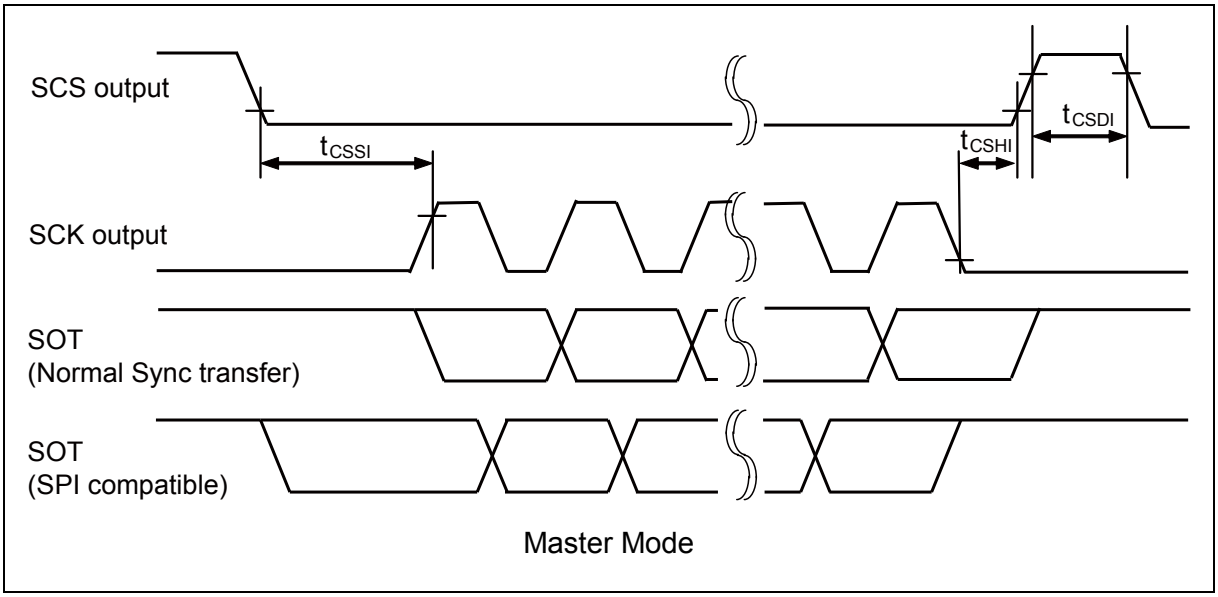
Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000414_H	ICSEL20[R/W] B,H,W -------0	ICSEL21[R/W] B,H,W -----000	ICSEL22[R/W] B,H,W -----000	ICSEL23[R/W] B,H,W -----000	Generation and clearing of DMA transfer requests
000418_H	ICSEL24[R/W] B,H,W -----000	ICSEL25[R/W] B,H,W -----000	ICSEL26[R/W] B,H,W -------0	ICSEL27[R/W] B,H,W -------0	
$00041C_H$	-	-	-	-	
000420_H	-	-	-	-	
000424_H | $00043C_H$	-	-	-	-	Reserved
000440_H	ICR00[R/W] B,H,W ---11111	ICR01[R/W] B,H,W ---11111	ICR02[R/W] B,H,W ---11111	ICR03[R/W] B,H,W ---11111	Interrupt controller [S]
000444_H	ICR04[R/W] B,H,W ---11111	ICR05[R/W] B,H,W ---11111	ICR06[R/W] B,H,W ---11111	ICR07[R/W] B,H,W ---11111	
000448_H	ICR08[R/W] B,H,W ---11111	ICR09[R/W] B,H,W ---11111	ICR10[R/W] B,H,W ---11111	ICR11[R/W] B,H,W ---11111	
$00044C_H$	ICR12[R/W] B,H,W ---11111	ICR13[R/W] B,H,W ---11111	ICR14[R/W] B,H,W ---11111	ICR15[R/W] B,H,W ---11111	
000450_H	ICR16[R/W] B,H,W ---11111	ICR17[R/W] B,H,W ---11111	ICR18[R/W] B,H,W ---11111	ICR19[R/W] B,H,W ---11111	
000454_H	ICR20[R/W] B,H,W ---11111	ICR21[R/W] B,H,W ---11111	ICR22[R/W] B,H,W ---11111	ICR23[R/W] B,H,W ---11111	
000458_H	ICR24[R/W] B,H,W ---11111	ICR25[R/W] B,H,W ---11111	ICR26[R/W] B,H,W ---11111	ICR27[R/W] B,H,W ---11111	
$00045C_H$	ICR28[R/W] B,H,W ---11111	ICR29[R/W] B,H,W ---11111	ICR30[R/W] B,H,W ---11111	ICR31[R/W] B,H,W ---11111	
000460_H	ICR32[R/W] B,H,W ---11111	ICR33[R/W] B,H,W ---11111	ICR34[R/W] B,H,W ---11111	ICR35[R/W] B,H,W ---11111	
000464_H	ICR36[R/W] B,H,W ---11111	ICR37[R/W] B,H,W ---11111	ICR38[R/W] B,H,W ---11111	ICR39[R/W] B,H,W ---11111	
000468_H	ICR40[R/W] B,H,W ---11111	ICR41[R/W] B,H,W ---11111	ICR42[R/W] B,H,W ---11111	ICR43[R/W] B,H,W ---11111	
$00046C_H$	ICR44[R/W] B,H,W ---11111	ICR45[R/W] B,H,W ---11111	ICR46[R/W] B,H,W ---11111	ICR47[R/W] B,H,W ---11111	
000470_H | $00047C_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000480_H	RSTRR[R] B,H,W XXXX--XX	RSTCR[R/W] B,H,W 111----0	STBCR[R/W] B,H,W* 000---11	-	Reset control [S] Power consumption control [S] * Writing to STBCR by DMA is disabled.
000484_H	-	-	-	-	Reserved [S]
000488_H	DIVR0[R/W] B,H,W 000-----	DIVR1[R/W] B,H,W 0001----	DIVR2[R/W] B,H,W 0011----	-	Clock control [S]
$00048C_H$	-	-	-	-	Reserved [S]
000490_H	IORR0[R/W] B,H,W -0000000	IORR1[R/W] B,H,W -0000000	IORR2[R/W] B,H,W -0000000	IORR3[R/W] B,H,W -0000000	DMA transfer request from a peripheral [S]
000494_H	IORR4[R/W] B,H,W -0000000	IORR5[R/W] B,H,W -0000000	IORR6[R/W] B,H,W -0000000	IORR7[R/W] B,H,W -0000000	
000498_H	-	-	-	-	
$00049C_H$	-	-	-	-	
$0004A0_H$	-	-	-	-	Reserved
$0004A4_H$	CANPRE[R/W] B,H,W ----0000	-	-	-	CAN prescaler
$0004A8_H$ | $0004AC_H$	-	-	-	-	Reserved
$0004B0_H$	-	-	-	-	Reserved
$0004B4_H$ | $0004C0_H$	-	-	-	-	Reserved
$0004C4_H$	CUCR1[R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		WDT1 calibration
$0004C8_H$	CUTR1[R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$ | $0004DC_H$	-	-	-	-	Reserved
$0004E0_H$	-	-	CSCFG[R/W] B,H,W ---0----	CMCFG[R/W] B,H,W 00000000	Clock monitor
$0004E4_H$	-	-	-	-	
$0004E8_H$	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	FlexRay clock control
$0004EC_H$	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -------0	CLKR2[R/W] B,H,W 000--000	-	
$0004F0_H$ | $0004FC_H$	-	-	-	-	Reserved
000500_H	-				Reserved
000504_H	-				Reserved

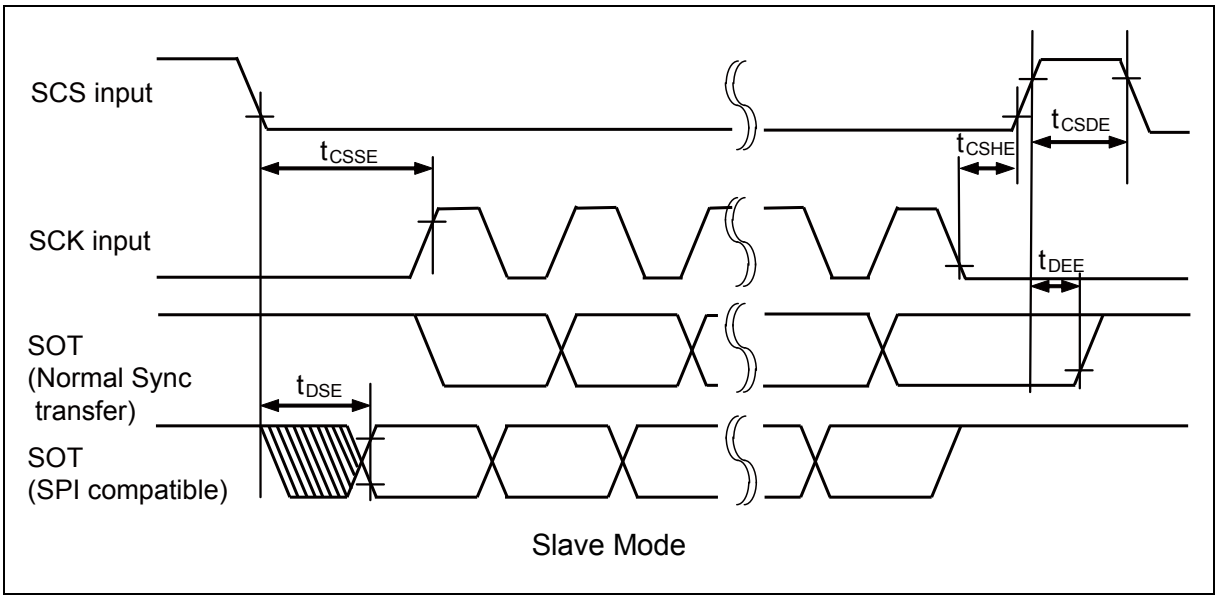
Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0012A8_H$	ADCS1[R/W] B,H,W 0------- --------		ADCH1[R] B,H,W -----000	ADMD1[R/W] B,H,W ----0000	12-bit A/D converter
$0012AC_H$	ADCS2[R/W] B,H,W 0------- --------		ADCH2[R] B,H,W -----000	ADMD2[R/W] B,H,W ----0000	
$0012B0_H$ | $0012FC_H$	-	-	-	-	Reserved
001300_H	-	-	-	-	Reserved
001304_H	-	-	-	-	
001308_H	-	-	-	-	
$00130C_H$	-	-	-	-	
001310_H	-	-	-	-	
001314_H	-	-	-	-	
001318_H	-	-	-	-	
$00131C_H$	-	-	-	-	
001320_H	-	-	-	-	
001324_H	-		-		
001328_H	-	-	-	-	
$00132C_H$	-	-	-	-	
001330_H	-		-		
001334_H | $0013FC_H$	-	-	-	-	Reserved
001400_H	DACR[R/W] B,H,W -------0	-	DADR[R/W] H,W ------XX XXXXXXXX		DAC
001404_H | $0014FC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002044_H	IF2MSK20[R/W] B,H,W 11-11111 11111111		IF2MSK10[R/W] B,H,W 11111111 11111111		CAN 0 64msb
002048_H	IF2ARB20[R/W] B,H,W 00000000 00000000		IF2ARB10[R/W] B,H,W 00000000 00000000		
$00204C_H$	IF2MCTR0[R/W] B,H,W 00000000 0---0000		-		
002050_H	IF2DTA10[R/W] B,H,W 00000000 00000000		IF2DTA20[R/W] B,H,W 00000000 00000000		
002054_H	IF2DTB10[R/W] B,H,W 00000000 00000000		IF2DTB20[R/W] B,H,W 00000000 00000000		
002058_H, $00205C_H$	-		-		
002060_H, 002064_H	Reserved (IF2 data mirror)				
002068_H | $00207C_H$	-		-		
002080_H	TREQR20[R] B,H,W 00000000 00000000		TREQR10[R] B,H,W 00000000 00000000		
002084_H	TREQR40[R] B,H,W 00000000 00000000		TREQR30[R] B,H,W 00000000 00000000		
002088_H	-		-		
$00208C_H$	-		-		
002090_H	NEWDT20[R] B,H,W 00000000 00000000		NEWDT10[R] B,H,W 00000000 00000000		
002094_H	NEWDT40[R] B,H,W 00000000 00000000		NEWDT30[R] B,H,W 00000000 00000000		
002098_H	-		-		
$00209C_H$	-		-		
$0020A0_H$	INTPND20[R] B,H,W 00000000 00000000		INTPND10[R] B,H,W 00000000 00000000		
$0020A4_H$	INTPND40[R] B,H,W 00000000 00000000		INTPND30[R] B,H,W 00000000 00000000		
$0020A8_H$	-		-		
$0020AC_H$	-		-		
$0020B0_H$	MSGVAL20[R] B,H,W 00000000 00000000		MSGVAL10[R] B,H,W 00000000 00000000		
$0020B4_H$	MSGVAL40[R] B,H,W 00000000 00000000		MSGVAL30[R] B,H,W 00000000 00000000		
$0020B8_H$	-		-		
$0020BC_H$	-		-		
$0020C0_H$ | $0020FC_H$	-		-		
002100_H	CTRLR1[R/W] B,H,W -------- 000-0001		STATR1[R/W] B,H,W -------- 00000000		CAN 1 64msb
002104_H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1[R/W] B,H,W -0100011 00000001		
002108_H	INTR1[R] B,H,W 00000000 00000000		TESTR1[R/W] B,H,W -------- X00000--		
$00210C_H$	BRPER1[R/W] B,H,W -------- ----0000		-		
002110_H	IF1CREQ1[R/W] B,H,W 0------- 00000001		IF1CMSK1[R/W] B,H,W -------- 00000000		

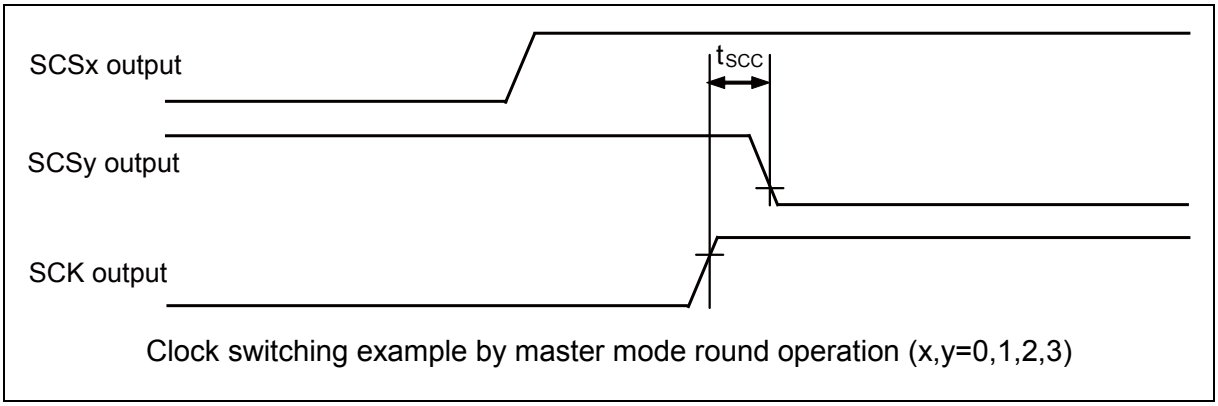
Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D080_H$	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC
$00D084_H$	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
$00D088_H$	SUCC3[R/W] W -------- -------- -------- 00010001				
$00D08C_H$	NEMC[R/W] W -------- -------- -------- ----0000				FlexRay NEM
$00D090_H$	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT
$00D094_H$	PRTC2[R/W] W --001111 00101101 --001010 --001110				
$00D098_H$	MHDC[R/W] W ---00000 00000000 -------- -0000000				FlexRay MHD
$00D09C_H$	-				Reserved
$00D0A0_H$	GTUC1[R/W] W -------- ----0000 00000010 10000000				FlexRay GTU
$00D0A4_H$	GTUC2[R/W] W -------- ----0010 --000000 00001010				
$00D0A8_H$	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
$00D0AC_H$	GTUC4[R/W] W --000000 00001000 --000000 00000111				
$00D0B0_H$	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
$00D0B4_H$	GTUC6[R/W] W -----000 00000010 -----000 00000000				
$00D0B8_H$	GTUC7[R/W] W ------00 00000010 ------00 00000100				
$00D0BC_H$	GTUC8[R/W] W ---00000 00000000 -------- --000010				
$00D0C0_H$	GTUC9[R/W] W -------- ------00 ---00001 --000001				
$00D0C4_H$	GTUC10[R/W] W -----000 00000010 --000000 00000101				
$00D0C8_H$	GTUC11[R/W] W -----000 -----000 ------00 ------00				
$00D0CC_H$ | $00D0FC_H$	-				Reserved
$00D100_H$	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay SUC
$00D104_H$	CCEV[R] W -------- -------- ---00000 00--0000				
$00D108_H$ $00D10C_H$	-				Reserved
$00D110_H$	SCV[R] W -----000 00000000 -----000 00000000				FlexRay GTU
$00D114_H$	MTCCV[R] W -------- --000000 --000000 00000000				
$00D118_H$	RCV[R] W -------- -------- ----0000 00000000				
$00D11C_H$	OCV[R] W -------- -----000 00000000 00000000				



Master Mode

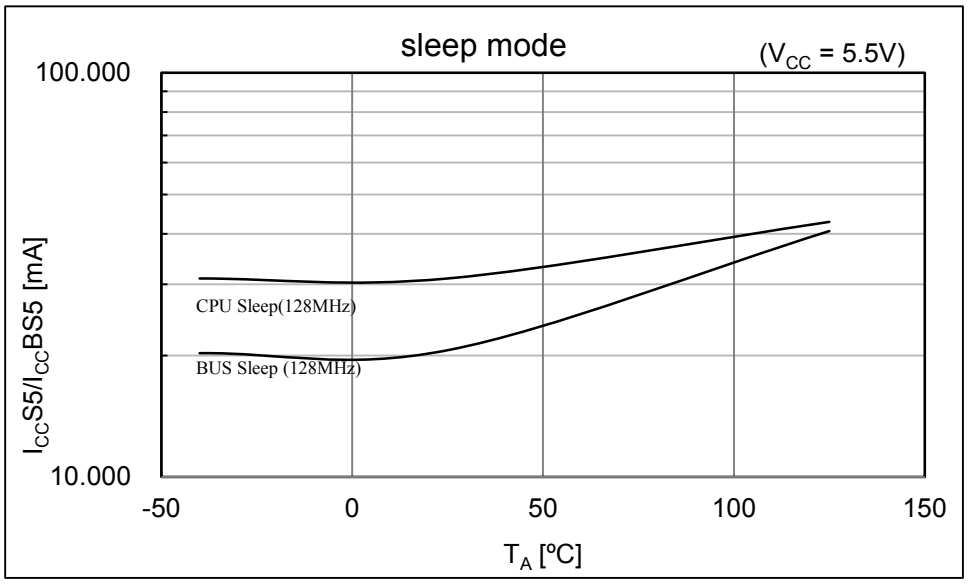


Slave Mode



Clock switching example by master mode round operation (x,y=0,1,2,3)

- MB91F585LA/F586LA/F587LA/F585LB/F586LB/F587LB/ F585LC/F586LC/F587LC/F585LD/F586LD/F587LD



- MB91F585LA/F586LA/F587LA/F585LB/F586LB/F587LB/ F585LC/F586LC/F587LC/F585LD/F586LD/F587LD