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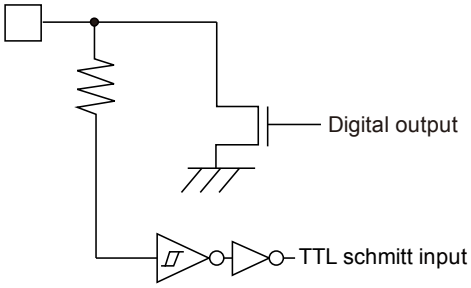
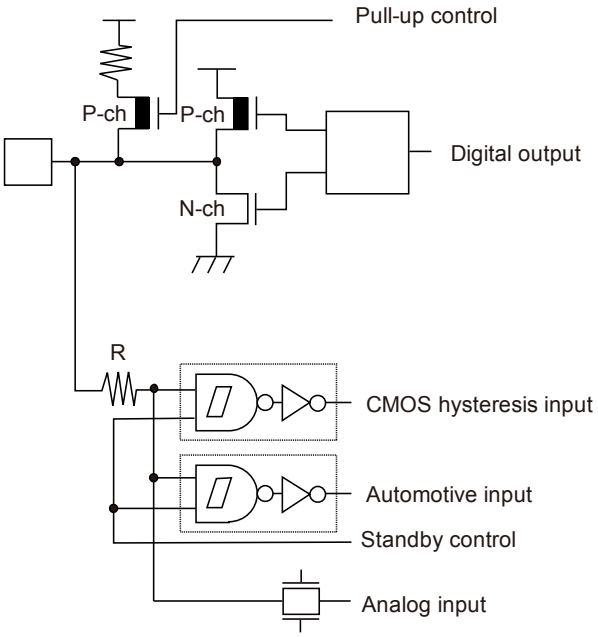
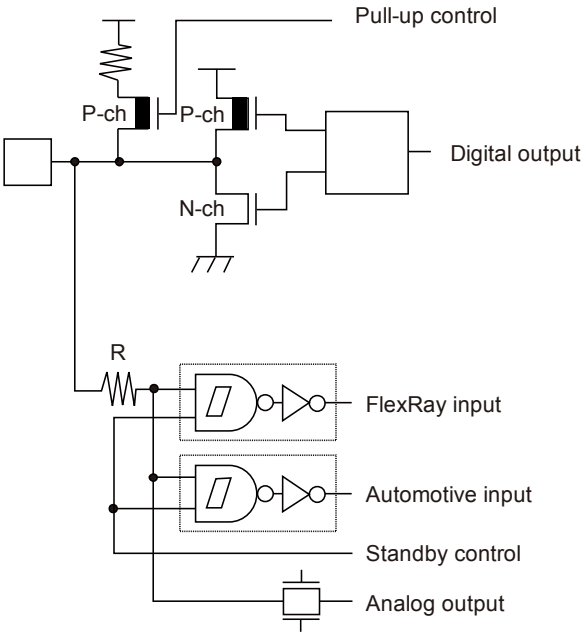
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	98
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f587lapmc-gtk5e1

Pin No.	Pin name	I/O circuit type*1	Function
141	P012	D	General-purpose I/O port
	D26		External bus data bit26 I/O pin
	TIOB0		Base timer ch.0 TIOB I/O pin
142	P013	D	General-purpose I/O port
	D27		External bus data bit27 I/O pin
	TIOA1		Base timer ch.1 TIOA I/O pin
143	P014	D	General-purpose I/O port
	D28		External bus data bit28 I/O pin
	TIOB1		Base timer ch.1 TIOB I/O pin
2	P015	D	General-purpose I/O port
	D29		External bus data bit29 I/O pin
	TRG0		PPG ch.0 to ch.3 external trigger
3	P016	D	General-purpose I/O port
	D30		External bus data bit30 I/O pin
	TRG1		PPG ch.4 to ch.7 external trigger
4	P017	D	General-purpose I/O port
	D31		External bus data bit31 I/O pin
	TRG2		PPG ch.8 to ch.11 external trigger
5	P020	D	General-purpose I/O port
	ASX		External bus address strobe output pin
	TRG3		PPG ch.12 to ch.15 external trigger
	SIN3_1		Multi-function serial ch.3 serial data input pin (1)
6	P021	K	General-purpose I/O port
	CS0X		External bus chip select 0 output pin
	TRG4		PPG16 to PPG19 external trigger
	SOT3_1		Multi-function serial ch.3 serial data output pin (1)/ I^2C ch.3 serial data I/O pin (1) (SDA)
7	P022	K	General-purpose I/O port
	CS1X		External bus chip select 1 output pin
	TRG5		PPG ch.20 to ch.23 external trigger
	SCK3_1		Multi-function serial ch.3 clock I/O pin (1)/ I^2C ch.3 clock I/O pin (1) (SCL)
8	P023	D	General-purpose I/O port
	RDX		External bus read strobe output pin
	TIN0		Reload timer ch.0 event input pin
	SCS3_1		Multi-function serial ch.3 serial chip select I/O pin (1)
9	P024	D	General-purpose I/O port
	WR0X		External bus write strobe 0 output pin
	TIN1		Reload timer ch.1 event input pin
	SIN4_1		Multi-function serial ch.4 serial data input pin (1)
10	P025	K	General-purpose I/O port
	WR1X		External bus write strobe 1 output pin
	TIN2		Reload timer ch.2 event input pin
	SOT4_1		Multi-function serial ch.4 serial data output pin (1)/ I^2C ch.4 serial data I/O pin (1) (SDA)

Type	Circuit	Remarks
L		Open drain I/O
M		• With analog input, I^2C, general-purpose I/O port • CMOS level output I_{OH}=-3mA, I_{OL}=3mA (at I^2C output) I_{OH}=-2/-5mA, I_{OL}=2/5mA (other than above) • With 50 kΩ pull-up resistor control • CMOS hysteresis input (0.7Vcc/0.3Vcc) • Automotive input (0.8Vcc/0.5Vcc)
N		• With analog output, general-purpose I/O port • CMOS level output I_{OH}=-2/-4mA, I_{OL}=2/4mA • With 50 kΩ pull-up resistor control • FlexRay input (0.7Vcc/0.3Vcc) • Automotive input (0.8Vcc/0.5Vcc)

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- Processing and Protection of Pins

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high-voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

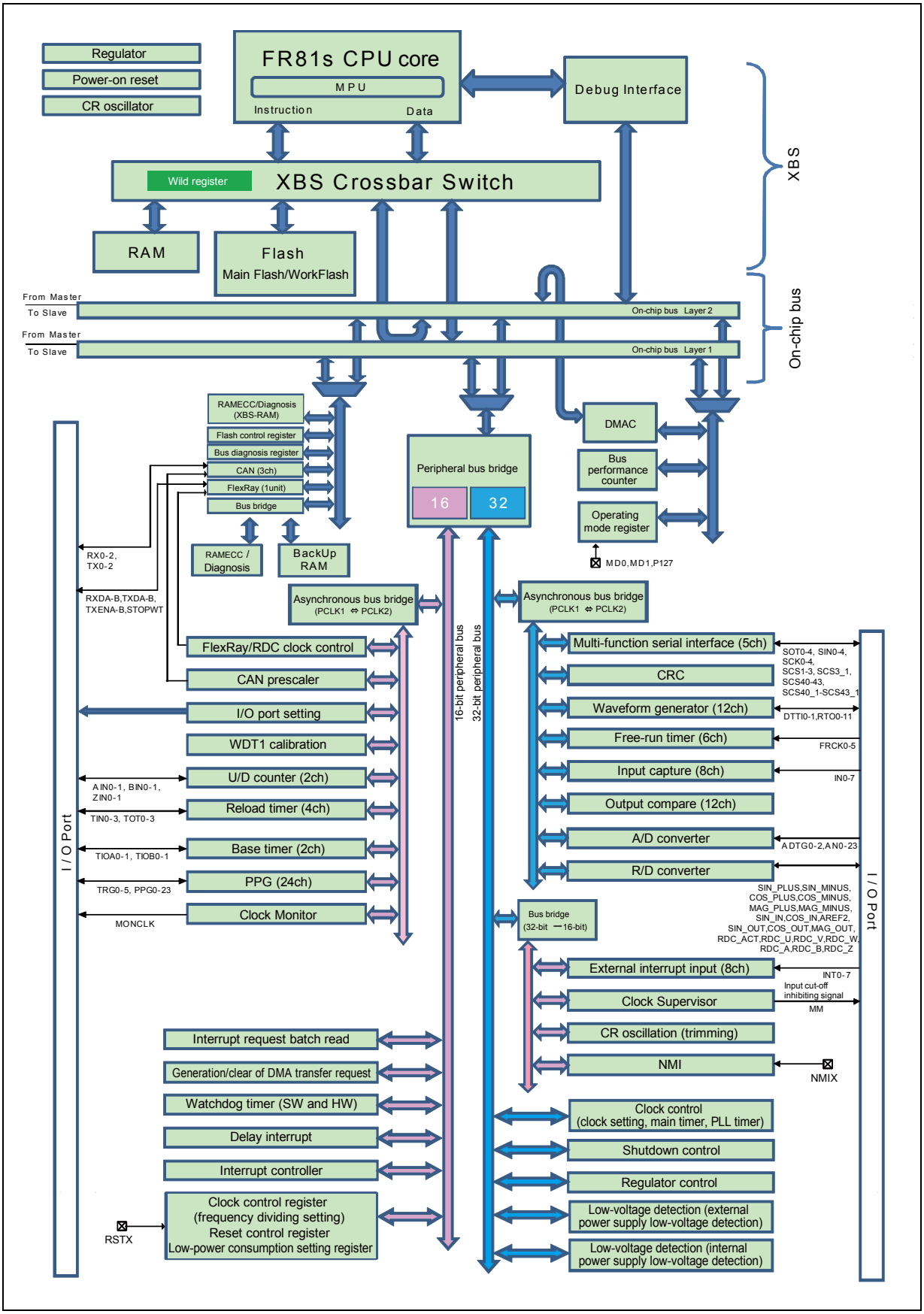
  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

■ BLOCK DIAGRAM

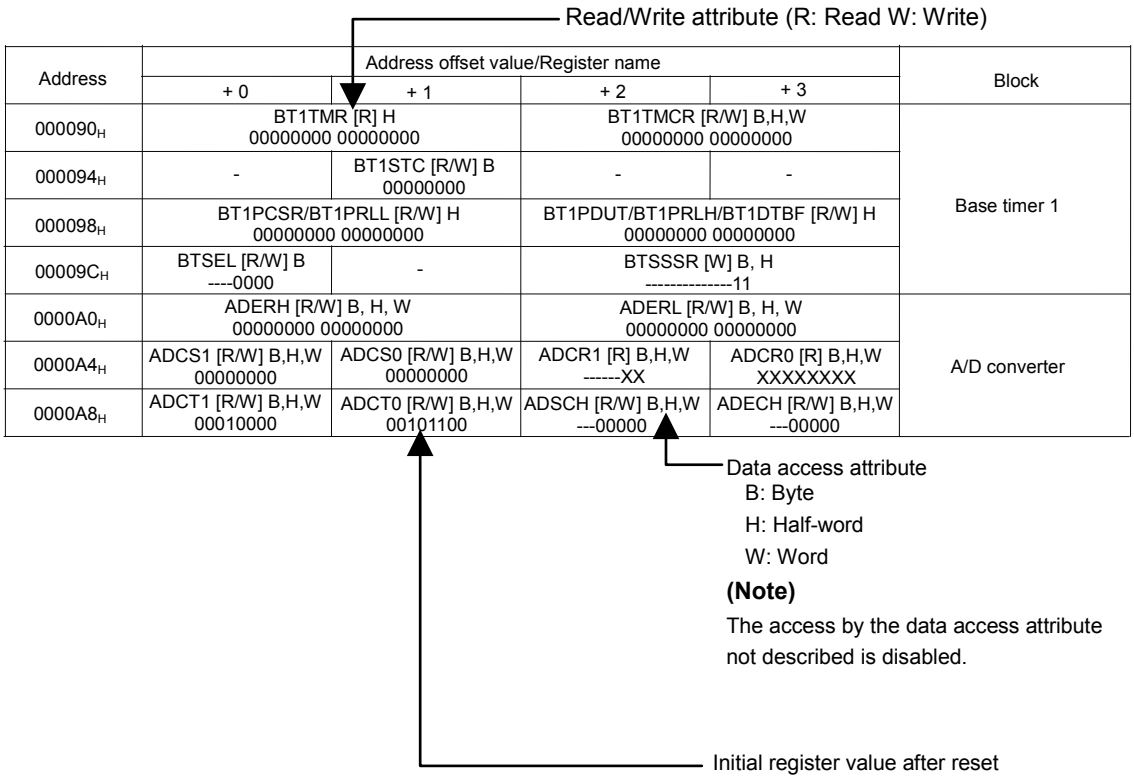
• MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC



■ I/O MAP

The following I/O map shows the relationship between memory space and registers for peripheral resources.

- Legend of I/O Map



Address	Address offset value/Register name				Block
	+ 0	+ 1	+ 2	+ 3	
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] B,H,W 00000000 00000000		Base timer 1
000094_H	-	BT1STC [R/W] B 00000000	-	-	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL [R/W] B ----0000	-	BTSSSR [W] B, H ----------11		
$0000A0_H$	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B,H,W 00000000	ADCS0 [R/W] B,H,W 00000000	ADCR1 [R] B,H,W ------XX	ADCR0 [R] B,H,W XXXXXXXX	
$0000A8_H$	ADCT1 [R/W] B,H,W 00010000	ADCT0 [R/W] B,H,W 00101100	ADSCH [R/W] B,H,W ---00000	ADECH [R/W] B,H,W ---00000	

The initial register values after reset are indicated as follows:

"1": Initial value "1"
"0": Initial value "0"
"X": Initial value undefined
"-": Reserved bit/Undefined bit
"*": Initial value "0" or "1" according to the setting

Note:

It is prohibited to access addresses not described here.

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001524_H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000000-0	SSR1[R/W] B,H,W 0--00011	ESCR1/(IBSR1) [R/W] B,H,W 00000000	Multi Function Serial I/F 1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001528_H	-/(RDR11/(TDR11))[R/W] H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
$00152C_H$	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001530_H	STMCR1[R/W] B,H,W 00000000 00000000		-/(SCSCR1/SFUR1) [R/W] B,H,W -------- -------- *3,*4		
001534_H	-/(SCSTR31) [R/W] B,H,W -------- *3	-/(SCSTR21) [R/W] B,H,W -------- *3	-/(SCSTR11/SFLR11) [R/W] B,H,W -------- *3,*4	-/(SCSTR01/SFLR01) [R/W] B,H,W -------- *3,*4	
001538_H	-	-	-	-	
$00153C_H$	-	-	-	TBYTE01[R/W] B,H,W 00000000	
001540_H	BGR1[R/W] H,W 00000000 00000000		-/(ISMK1)[R/W] B,H,W -------- *2	-/(ISBA1)[R/W] B,H,W -------- *2	
001544_H	FCR11[R/W] B,H,W 00-00100	FCR01[R/W] B,H,W -0000000	FBYTE21[R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
001548_H	SCR2[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000000-0	SSR2[R/W] B,H,W 0--00011	ESCR2[R/W] B,H,W 00000000	Multi Function Serial I/F 2 *1: Byte access is possible only for access to lower 8 bits. *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
$00154C_H$	-/(RDR12/(TDR12))[R/W] H,W -------- -------- *3		RDR02/(TDR02)[R/W] B,H,W -------0 00000000 *1		
001550_H	SACSR2[R/W] B,H,W 0----000 00000000		STMR2[R] B,H,W 00000000 00000000		
001554_H	STMCR2[R/W] B,H,W 00000000 00000000		-/(SCSCR2/SFUR2) [R/W] B,H,W -------- -------- *3,*4		
001558_H	-/(SCSTR32) [R/W] B,H,W -------- *3	-/(SCSTR22) [R/W] B,H,W -------- *3	-/(SCSTR12/SFLR12) [R/W] B,H,W -------- *3,*4	-/(SCSTR02/SFLR02) [R/W] B,H,W -------- *3,*4	
$00155C_H$	-	-	-	-	
001560_H	-	-	-	TBYTE02[R/W] B,H,W 00000000	
001564_H	BGR2[R/W] H,W 00000000 00000000		-	-	
001568_H	FCR12[R/W] B,H,W 00-00100	FCR02[R/W] B,H,W -0000000	FBYTE22[R/W] B,H,W 00000000	FBYTE12[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002000_H	CTRLR0[R/W] B,H,W -------- 000-0001		STATR0[R/W] B,H,W -------- 00000000		CAN 0 64msb
002004_H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008_H	INTR0[R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W -------- X00000--		
$00200C_H$	BRPER0[R/W] B,H,W -------- ----0000		-		
002010_H	IF1CREQ0[R/W] B,H,W 0------- 00000001		IF1CMSK0[R/W] B,H,W -------- 00000000		
002014_H	IF1MSK20[R/W] B,H,W 11-11111 11111111		IF1MSK10[R/W] B,H,W 11111111 11111111		
002018_H	IF1ARB20[R/W] B,H,W 00000000 00000000		IF1ARB10[R/W] B,H,W 00000000 00000000		
$00201C_H$	IF1MCTR0[R/W] B,H,W 00000000 0---0000		-		
002020_H	IF1DTA10[R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024_H	IF1DTB10[R/W] B,H,W 00000000 00000000		IF1DTB20[R/W] B,H,W 00000000 00000000		
002028_H, $00202C_H$	-		-		
002030_H, 002034_H	Reserved (IF1 data mirror)				
002038_H, $00203C_H$	-		-		
002040_H	IF2CREQ0[R/W] B,H,W 0------- 00000001		IF2CMSK0[R/W] B,H,W -------- 00000000		
002044_H	IF2MSK20[R/W] B,H,W 11-11111 11111111		IF2MSK10[R/W] B,H,W 11111111 11111111		
002048_H	IF2ARB20[R/W] B,H,W 00000000 00000000		IF2ARB10[R/W] B,H,W 00000000 00000000		
$00204C_H$	IF2MCTR0[R/W] B,H,W 00000000 0---0000		-		
002050_H	IF2DTA10[R/W] B,H,W 00000000 00000000		IF2DTA20[R/W] B,H,W 00000000 00000000		
002054_H	IF2DTB10[R/W] B,H,W 00000000 00000000		IF2DTB20[R/W] B,H,W 00000000 00000000		
002058_H, $00205C_H$	-		-		
002060_H, 002064_H	Reserved (IF2 data mirror)				
002068_H | $00207C_H$	-		-		
002080_H	TREQR20[R] B,H,W 00000000 00000000		TREQR10[R] B,H,W 00000000 00000000		
002084_H	TREQR40[R] B,H,W 00000000 00000000		TREQR30[R] B,H,W 00000000 00000000		
002088_H	-		-		
$00208C_H$	-		-		
002090_H	NEWDT20[R] B,H,W 00000000 00000000		NEWDT10[R] B,H,W 00000000 00000000		
002094_H	NEWDT40[R] B,H,W 00000000 00000000		NEWDT30[R] B,H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D03C_H$	SIER[R/W] W ------00 ------00 00000000 00000000				FlexRay INT
$00D040_H$	ILE[R/W] W -------- -------- -------- ------00				
$00D044_H$	T0C[R/W] W --000000 00000000 -0000000 ------00				
$00D048_H$	T1C[R/W] W --000000 00000010 -------- ------00				
$00D04C_H$	STPW1[R/W] W --000000 00000000 --000000 -0000000				
$00D050_H$	STPW2[R] W -----000 00000000 -----000 00000000				
$00D054_H$ | $00D07C_H$	-	-	-	-	Reserved
$00D080_H$	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC
$00D084_H$	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
$00D088_H$	SUCC3[R/W] W -------- -------- -------- 00010001				
$00D08C_H$	NEMC[R/W] W -------- -------- -------- ----0000				FlexRay NEM
$00D090_H$	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT
$00D094_H$	PRTC2[R/W] W --001111 00101101 --001010 --001110				
$00D098_H$	MHDC[R/W] W ---00000 00000000 -------- -0000000				FlexRay MHD
$00D09C_H$	-				Reserved
$00D0A0_H$	GTUC1[R/W] W -------- ----0000 00000010 10000000				FlexRay GTU
$00D0A4_H$	GTUC2[R/W] W -------- ----0010 --000000 00001010				
$00D0A8_H$	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
$00D0AC_H$	GTUC4[R/W] W --000000 00001000 --000000 00000111				
$00D0B0_H$	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
$00D0B4_H$	GTUC6[R/W] W -----000 00000010 -----000 00000000				
$00D0B8_H$	GTUC7[R/W] W ------00 00000010 ------00 00000100				
$00D0BC_H$	GTUC8[R/W] W ---00000 00000000 -------- --000010				
$00D0C0_H$	GTUC9[R/W] W -------- ------00 ---00001 --000001				
$00D0C4_H$	GTUC10[R/W] W -----000 00000010 --000000 00000101				
$00D0C8_H$	GTUC11[R/W] W -----000 -----000 ------00 ------00				
$00D0CC_H$ | $00D0FC_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000588_H | $00058C_H$	-	-	-	-	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H	ASR0[R/W] W 00000000 00000000 -------- 1111-001				External bus interface [S]
000604_H	ASR1[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608_H	ASR2[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
$00060C_H$	ASR3[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000610_H | $00063C_H$	-	-	-	-	Reserved[S]
000640_H	ACR0[R/W] W -------- -------- -------- 00--00--				External bus interface [S]
000644_H	ACR1[R/W] W -------- -------- -------- XX--XX--				
000648_H	ACR2[R/W] W -------- -------- -------- XX--XX--				
$00064C_H$	ACR3[R/W] W -------- -------- -------- XX--XX--				
000650_H | $00067C_H$	-	-	-	-	Reserved[S]
000680_H	AWR0[R/W] W ----1111 00000000 11110000 00000-0-				External bus interface [S]
000684_H	AWR1[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688_H	AWR2[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
$00068C_H$	AWR3[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690_H | $0006BC_H$	-	-	-	-	Reserved[S]
$0006C0_H$	DMAR0[R/W] W -------- -------- -------- ----0000				External bus interface [S]
$0006C4_H$	DMAR1[R/W] W -------- -------- -------- ----0000				
$0006C8_H$	DMAR2[R/W] W -------- -------- -------- ----0000				
$0006CC_H$	DMAR3[R/W] W -------- -------- -------- ----0000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000F20_H$	PODR00[R/W] B,H 00000000	PODR01[R/W] B,H 00000000	PODR02[R/W] B,H 00000000	PODR03[R/W] B,H 00000000	Port output drive register
$000F24_H$	PODR04[R/W] B,H 00000000	PODR05[R/W] B,H 00000000	PODR06[R/W] B,H 00000000	PODR07[R/W] B,H 00000000	
$000F28_H$	PODR08[R/W] B,H 00000000	PODR09[R/W] B,H 00000000	PODR10[R/W] B,H 00000000	PODR11[R/W] B,H 00000000	
$000F2C_H$	PODR12[R/W] B,H 00000000	PODR13[R/W] B,H 00-00000	-	-	
$000F30_H$ | $000F3C_H$	-	-	-	-	Reserved
$000F40_H$	PORTEN[R/W] B,H,W ------00	-	-	-	Port input enable register
$000F44_H$	KEYCDR[R/W] H 00000000 00000000		-	-	Port key code
$000F48_H$	ADERH[R/W] B,H -------- 11111111		ADERL[R/W] B,H 11111111 11111111		Analog input enable register
$000F4C_H$	DAER[R/W] B,H -------0	-	-	-	Analog output enable register
$000F50_H$ | $000FFC_H$	-	-	-	-	Reserved
001000_H	SACR[R/W] B,H,W -------0	PICD[R/W] B,H,W ----0011	-	-	Synchronous/asynchronous switch control
001004_H | $0010BC_H$	-	-	-	-	Reserved
$0010C0_H$	-	-	-	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation
$0010C4_H$	CRCINIT[R/W] B,H,W 11111111 11111111 11111111 11111111				
$0010C8_H$	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
$0010CC_H$	CRCR[R] B,H,W 11111111 11111111 11111111 11111111				
$0010D0_H$ | $0010FC_H$	-	-	-	-	Reserved
001100_H	TCGS[R/W] B,H,W ------00	-	-	TCGSE[R/W] B,H,W --000000	Free-run timer simultaneous activation
001104_H	CPCLRB0/CPCLR0[R/W] H,W 11111111 11111111		TCDT0[R/W] H,W 00000000 00000000		Free-run timer 0
001108_H	TCCS0[R/W] B,H,W 00000000 01000000 ----0000 --------				

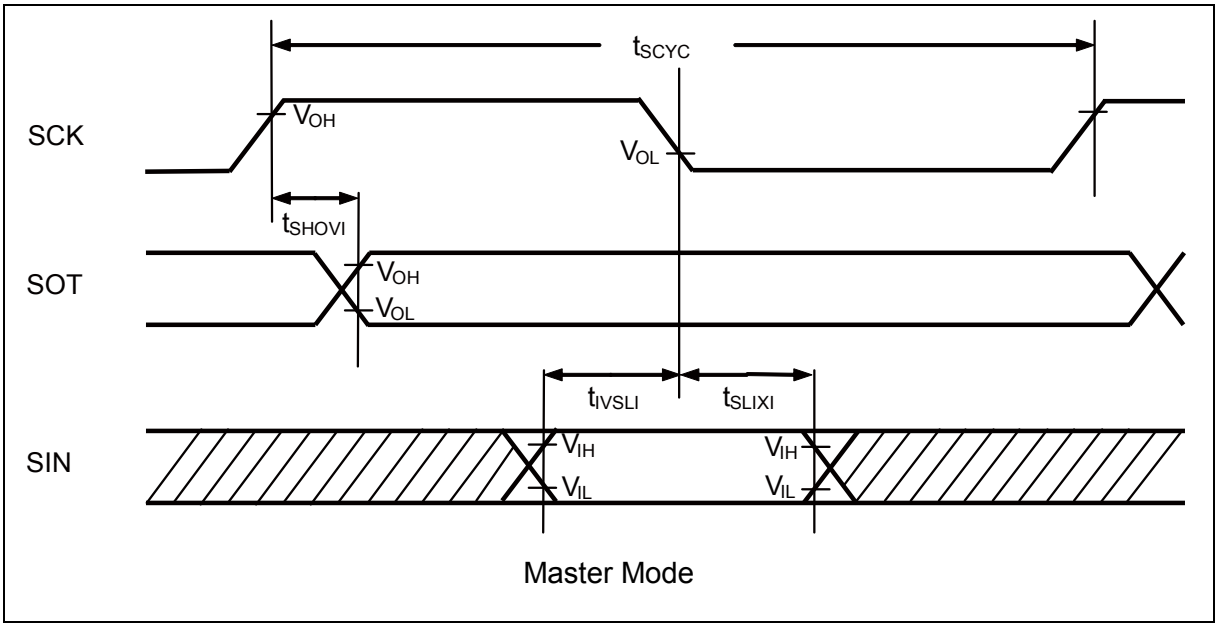
Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00300C_H$	TEAR0X[R] B,H,W 000----- -------- -0000000 00000000				XBS RAM diagnosis register
003010_H	TEAR1X[R] B,H,W 000----- -------- -0000000 00000000				
003014_H	TEAR2X[R] B,H,W 000----- -------- -0000000 00000000				
003018_H	TAEARX[R/W] B,H,W -1011111 11111111		TASARX[R/W] B,H,W -0000000 00000000		
$00301C_H$	TFECRX[R/W] B,H,W ----0000	TICRX[R/W] B,H,W ----0000	TTCRX[R/W] B,H,W ------00 00001100		
003020_H	TSRCRX[R/W] B,H,W 0-------	-	-	TKCCRX[R/W] B,H,W 00----00	
003024_H	SEEARA[R] B,H,W --000000 00000000		DEEARA[R] B,H,W --000000 00000000		Backup RAM ECC control register
003028_H	EECSRA[R/W] B,H,W ----00-0	-	EFEARA[R/W] B,H,W --000000 00000000		
$00302C_H$	-	EFECRA[R/W] B,H,W -------0 00000000 00000000			
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				Backup RAM diagnosis register
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA[R/W] B,H,W ----0000	TICRA[R/W] B,H,W ----0000	TTCRA[R/W] B,H,W ------00 00001100		
003044_H	TSRCRA[R/W] B,H,W 0-------	-	-	TKCCRA[R/W] B,H,W 00----00	
003048_H | $0030FC_H$	-	-	-	-	Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114_H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
$00311C_H$	-				
003120_H	BUSADR3[R] W 00000000 00000000 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D33C_H$	NDAT4[R] W 00000000 00000000 00000000 00000000				FlexRay MHD
$00D340_H$	MBSC1[R] W 00000000 00000000 00000000 00000000				
$00D344_H$	MBSC2[R] W 00000000 00000000 00000000 00000000				
$00D348_H$	MBSC3[R] W 00000000 00000000 00000000 00000000				
$00D34C_H$	MBSC4[R] W 00000000 00000000 00000000 00000000				
$00D350_H$ | $00D3EC_H$	-				Reserved
$00D3F0_H$	CREL[R] W 00010000 00111001 00000010 00000110				FlexRay GIF
$00D3F4_H$	ENDN[R] W 10000111 01100101 01000011 00100001				
$00D3F8_H$ | $00D3FC_H$	-				Reserved
$00D400_H$ | $00D4FC_H$	WRDSn[1-64][R/W] W 00000000 00000000 00000000 00000000				FlexRay IBF
$00D500_H$	WRHS1[R/W] W --000000 -0000000 -----000 00000000				
$00D504_H$	WRHS2[R/W] W -------- -0000000 -----000 00000000				
$00D508_H$	WRHS3[R/W] W -------- -------- -----000 00000000				
$00D50C_H$	-				
$00D510_H$	IBCM[R/W] W -------- ------00 -------- -----000				
$00D514_H$	IBCR[R/W] W 0------- -0000000 0------- -0000000				
$00D518_H$ | $00D5FC_H$	-				Reserved
$00D600_H$ | $00D6FC_H$	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF
$00D700_H$	RDHS1[R] W --000000 -0000000 -----000 00000000				
$00D704_H$	RDHS2[R] W -0000000 -0000000 -----000 00000000				
$00D708_H$	RDHS3[R] W --000000 --000000 -----000 00000000				
$00D70C_H$	MBS[R] W --000000 --000000 00-00000 00000000				
$00D710_H$	OBCM[R/W] W -------- ------00 -------- ------00				
$00D714_H$	OBCR[R/W] W -------- -0000000 0-----00 -0000000				
$00D718_H$ | $00D7FC_H$	-				Reserved

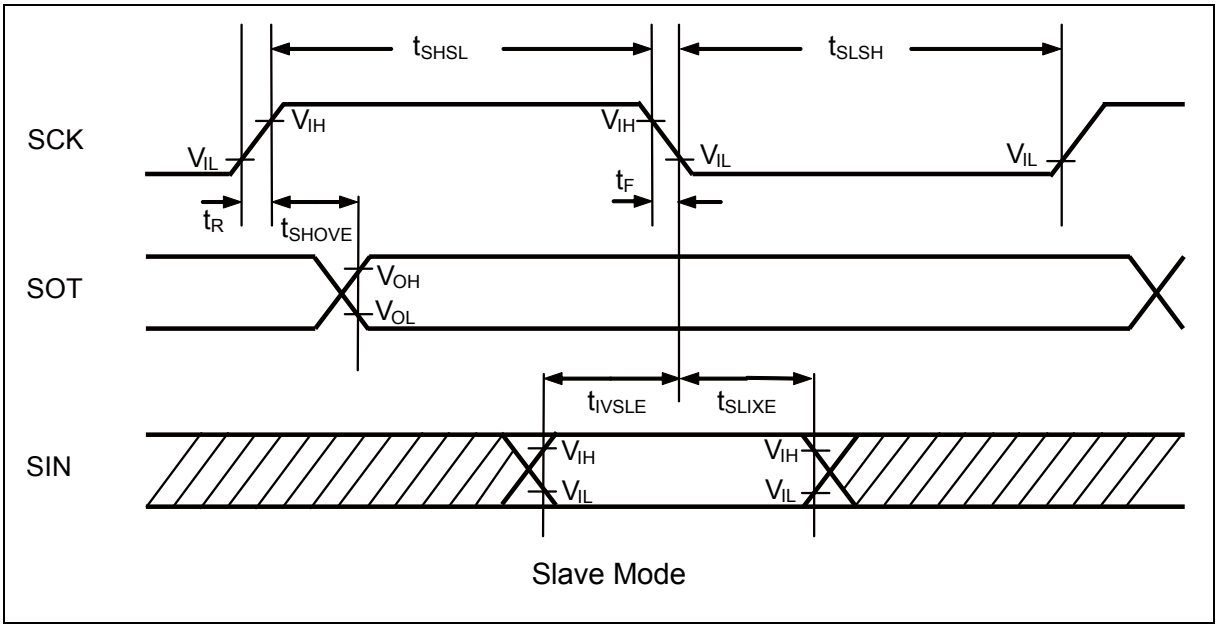
(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OL}=2.0mA	0	-	0.4	V	
	V_{OL2}	P003 to P007, P010	Vcc=4.5V I_{OL}=4.0mA	0	-	0.4	V	When FlexRay is selected
	V_{OL3}	P000 to P002, P011 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OL}=5.0mA	0	-	0.4	V	
	V_{OL4}	P001,P002, P021,P022, P025,P026, P073,P074, P076,P077, P127,P130	Vcc=4.5V I_{OL}=3.0mA	0	-	0.4	V	I^2C shared pin (when I^2C is selected)
	V_{OL5}	DEBUGIF	Vcc=2.7V I_{OL}=25.0mA	0	-	0.25	V	

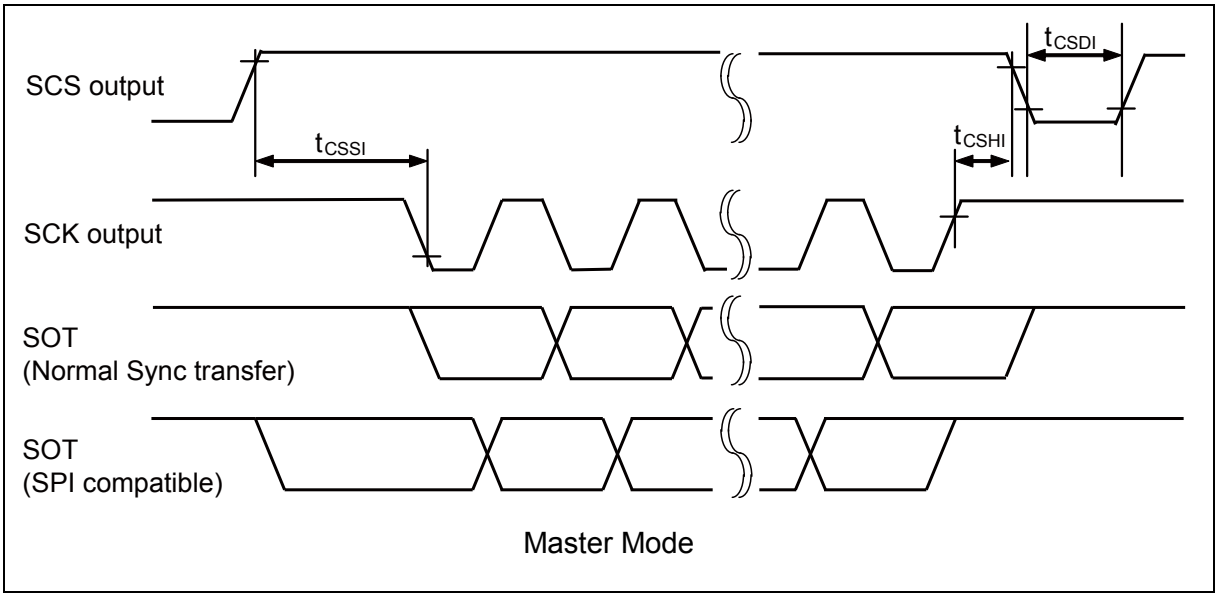
*: Only available with MB91F585LB/F586LB/F587LB, MB91F585LD/F586LD/F587LD



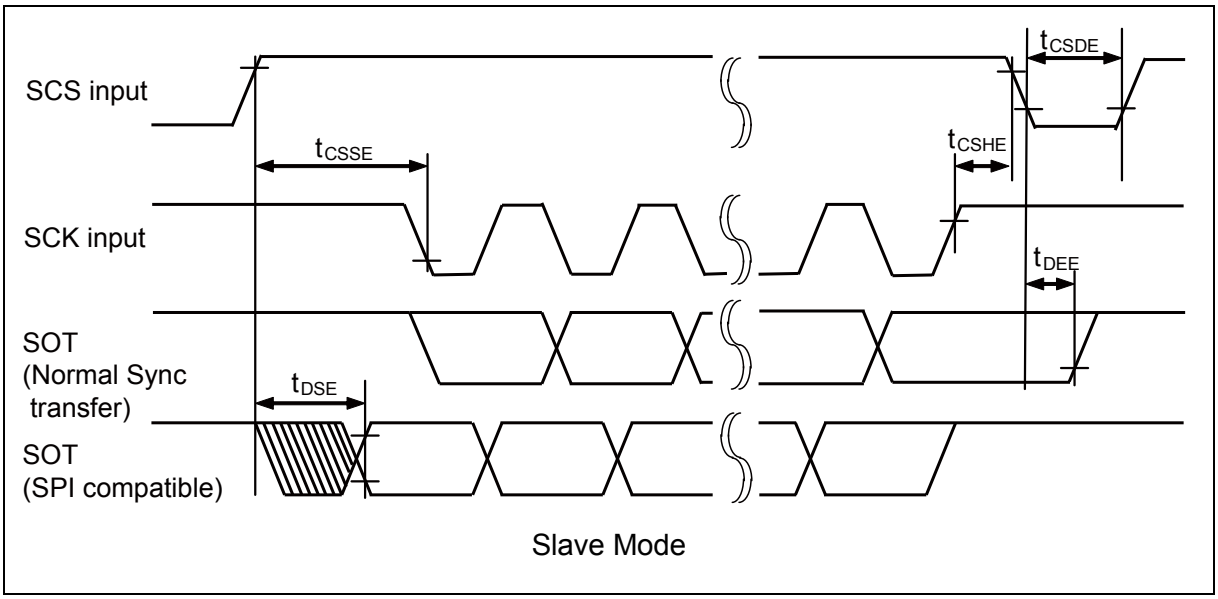
Master Mode



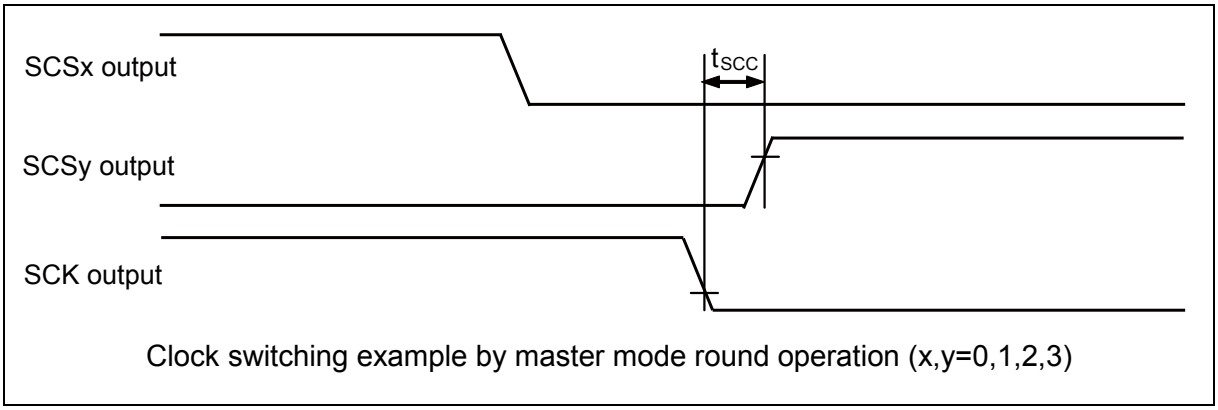
Slave Mode



Master Mode

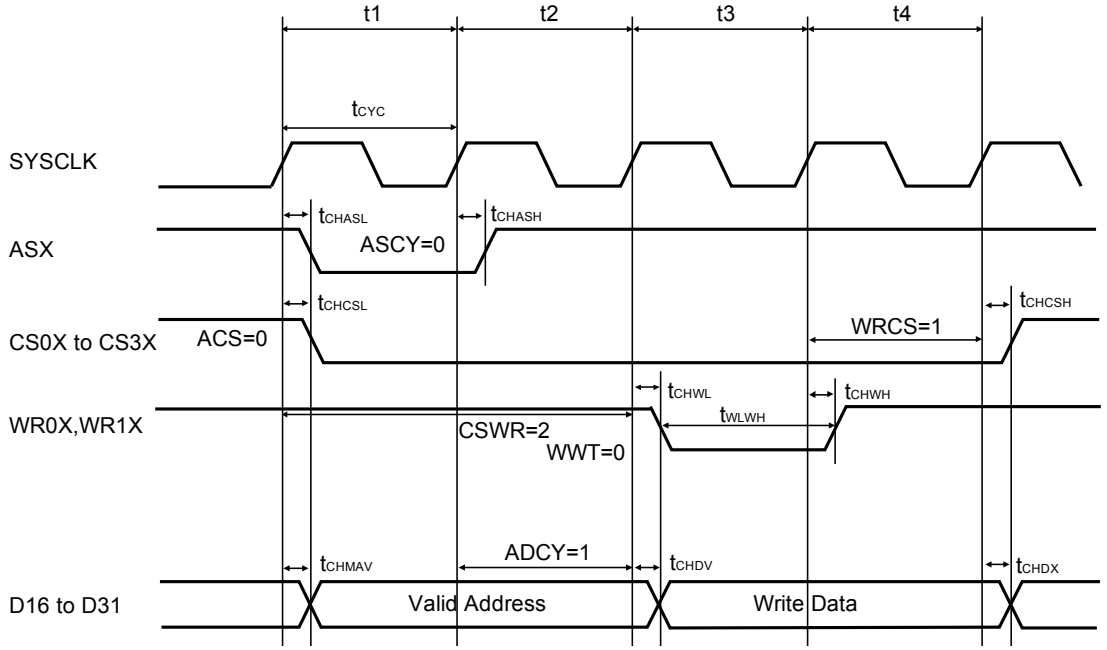


Slave Mode

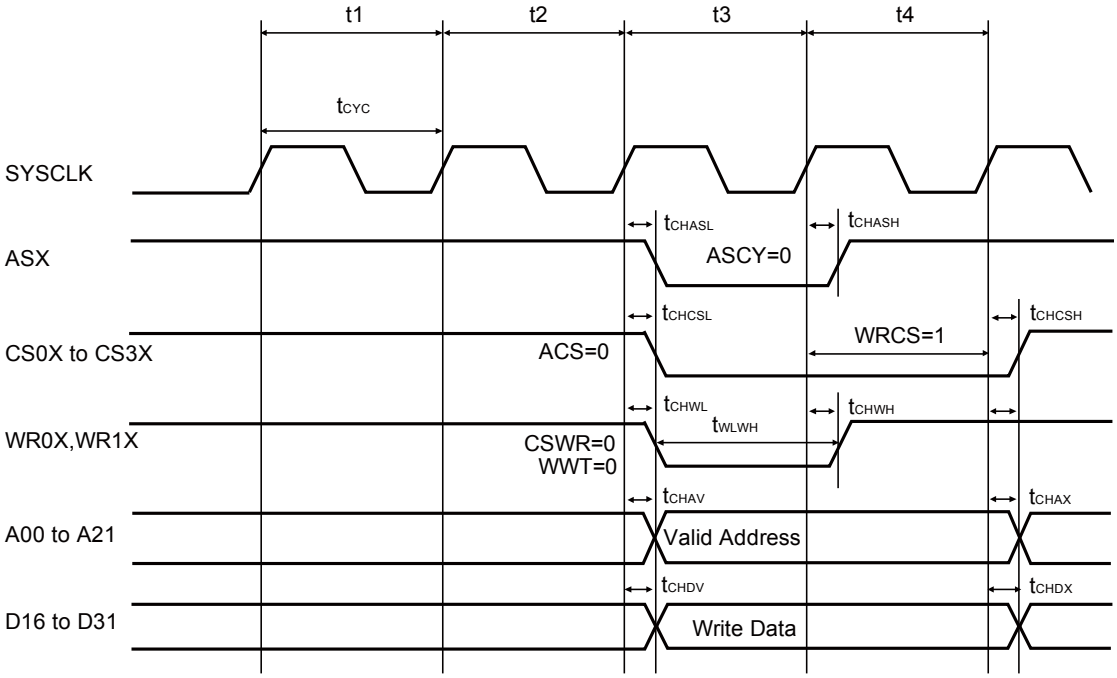


Clock switching example by master mode round operation (x,y=0,1,2,3)

External bus I/F (synchronous mode, write operation, and multiplex mode) timing



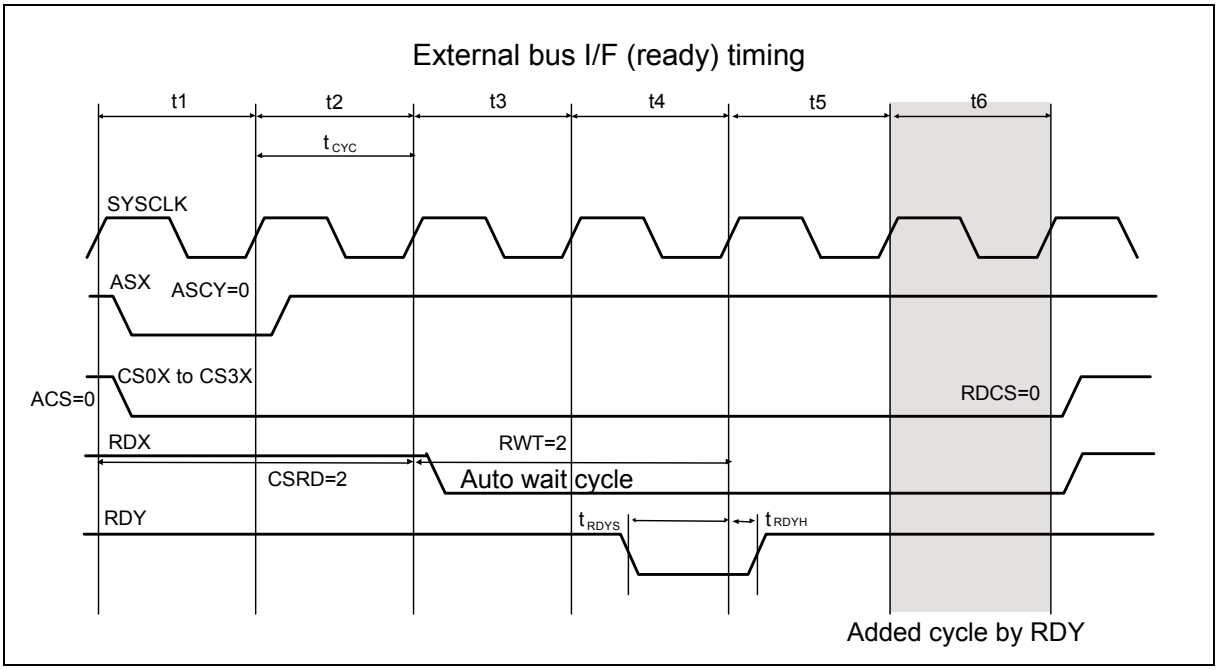
External bus I/F (synchronous mode, write operation, and split mode) timing



(13) External bus I/F (ready) timing

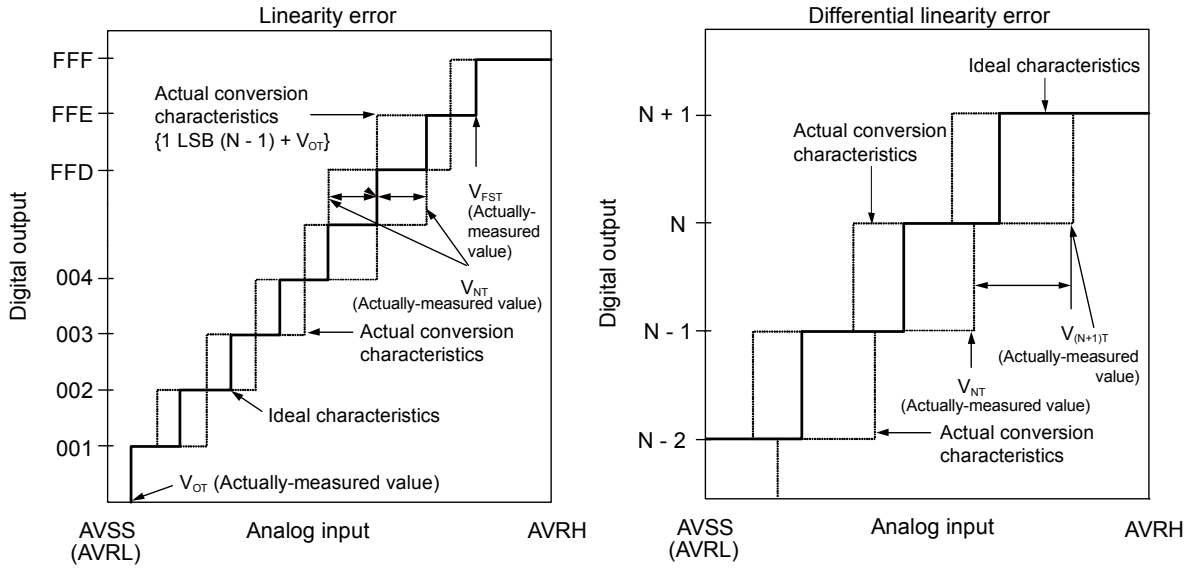
(T_A: Recommended operating conditions, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)
(External load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	50	-	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK ↑	t_{RDYS}	SYSCLK, RDY	28	-	ns	
SYSCLK ↑ → RDY hold time	t_{RDYH}	SYSCLK, RDY	0	-	ns	



(2) Definition of Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000"←→"0000 0000 0001") to the full-scale transition point ("1111 1111 1110"←→"1111 1111 1111").
- Differential linearity error: Deviation of the input voltage from the ideal value that is required to change the output code by 1LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N-1) + V_{OT}\}}{1LSB} \quad [LSB]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1\ LSB \quad [LSB]$$

$$1LSB = \frac{V_{FST} - V_{OT}}{4094} \quad [V]$$

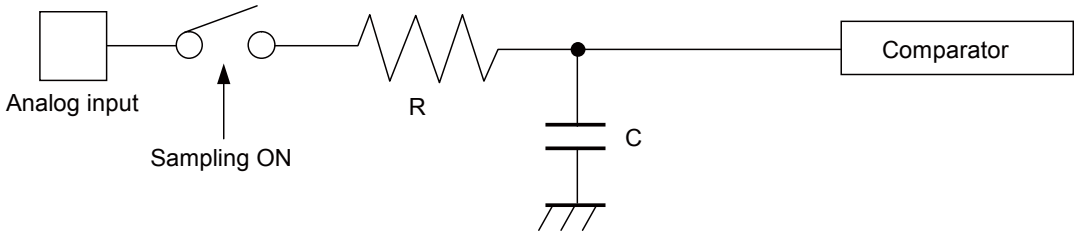
V_{OT}: Voltage at which the digital output changes from "000 $_H$" to "001$_H$".
V_{FST}: Voltage at which the digital output changes from "FFE $_H$" to "FFF$_H$".

(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling time for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

- Analog input circuit model



	R	C
12bit A/D	1.9kΩ (max)	8.30pF (max) (4.5V≦Avcc≦5.5V)

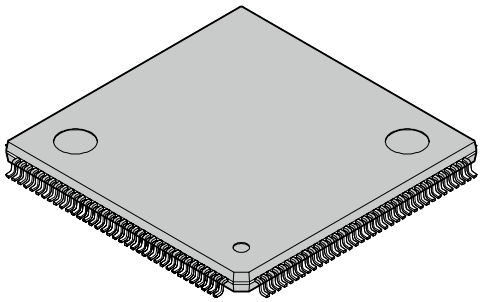
Note: Listed values must be considered as reference values.

6. D/A Converter

(T_A: Recommended operating conditions, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

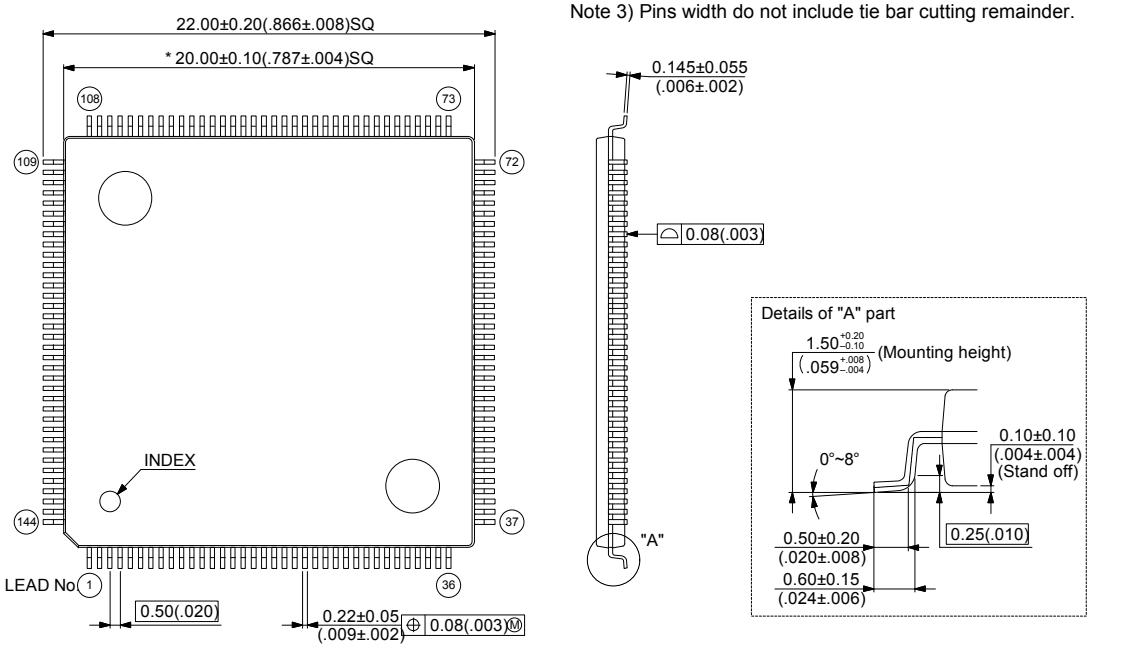
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Differential linearity error	-	-	-4.0	-	+4.0	LSB	When the analog output voltage is 0.5V to 4.5V

■ PACKAGE DIMENSIONS

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20 g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)

Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/