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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	3.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 1x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f587lbpmc-gtk5e1

<CSIO (Synchronous serial interface) >
- Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
- SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
- Built-in dedicated baud rate generator (Master operation)
- An external clock can be entered. (Slave operation)
- Overrun error detection function is provided.
- Built-in chip selection function
- DMA transfer supported

<LIN interface (v2.1)>
- Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
- LIN protocol revision2.1 supported.
- Master and slave systems supported
- Framing error and overrun error detection
- LIN synch break generation and detection; LIN synch delimiter generation
- Built-in dedicated baud rate generator
- An external clock can be adjusted by the reload counter.
- DMA transfer supported

< I^2C >
- Supported for 4 channels: ch.0,ch.1,ch.3, and ch4.
- Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
- Standard mode (Max. 100 kbps) / high-speed mode (Max. 400 kbps) supported
- DMA transfer supported (for transmission only)

- CAN controller (CAN): 3 channels
  - Transfer speed: Up to 1Mbps
  - 64-transmission/reception message buffering: 3 channels
- FlexRay controller: 1unit(ch.A/ch.B)
  - FlexRay Specifications Version 2.1 supported
  - Up to 128 message buffers
  - 8K bytes of message RAM
  - Variable length of message buffers
  - Each message buffer can be allocated as a part of reception buffer, transmission buffer or reception FIFO memory
  - Host access to the message buffer via input and output buffers
  - Filtering for slot counter, cycle counter and channels
  - Maskable interrupts are supported
- PPG: 16 bits × 24 channels
- Reload timer: 16 bits × 4 channels
- A/D converter (successive approximation type)
  - 12-bit resolution: 3units(24 channels)
  - Conversion time: 1 µs
- Free-run timer: 16 bits × 6 channels (1 channel can be selected for input capture, and 1 channel for output compare.)
- Input capture: 16 bits × 8 channels (linked to the free-run timer)
- Output compare: 16 bits × 12 channels (linked to the free-run timer)
- Waveform generator: 2 units (12 channels)
- R/D converter: 1 channel (MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC)
- 10-bit D/A converter: 1 channel (MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD)
- Calibration: The hardware watchdog for CR oscillation drive
  The CR oscillation frequency can be trimmed.

MB91580S Series Product Lineup Comparison

- Memory size

Items	MB91F583SG MB91F583SH MB91F583SJ MB91F583SK	MB91F584SG MB91F584SH MB91F584SJ MB91F584SK	MB91F585SG MB91F585SH MB91F585SJ MB91F585SK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

- Function

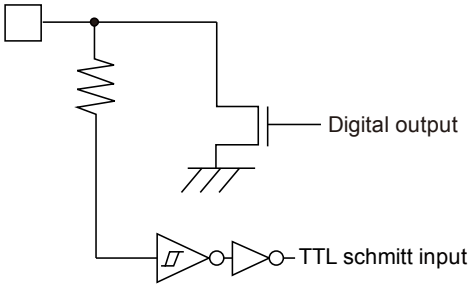
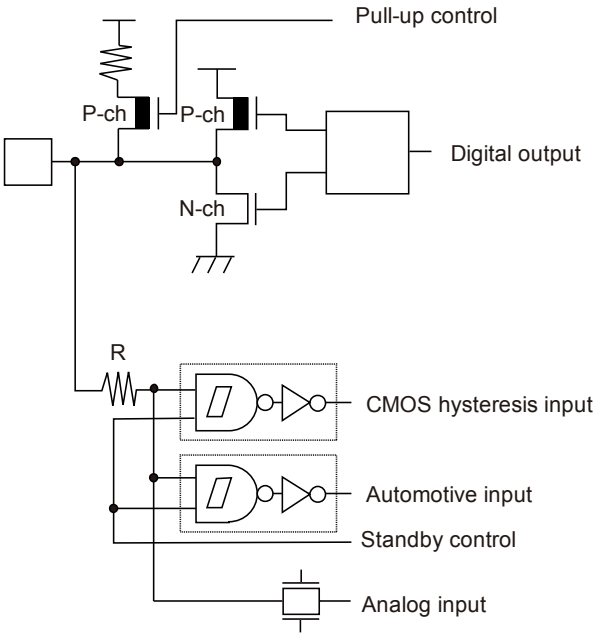
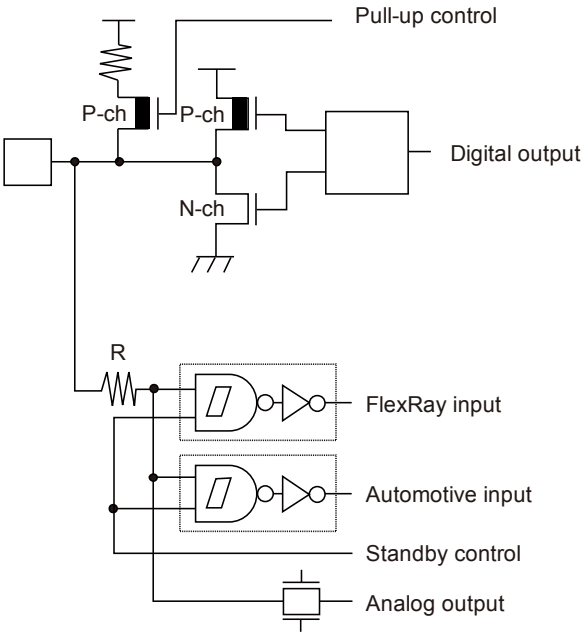
Items	MB91F583SG MB91F584SG MB91F585SG	MB91F583SH MB91F584SH MB91F585SH	MB91F583SJ MB91F584SJ MB91F585SJ	MB91F583SK MB91F584SK MB91F585SK
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during stand-by	Provided	Provided	Not provided	Not provided
External bus interface	Not provided			
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	4 channels			
Output compare	7 channels			
Waveform generator	2 unit (7channels)			
16-bit reload timer	4 channels			
PPG	6 channels			
External interrupt	7 channels			
A/D converter	3 units (17 channels)			
R/D converter	Not provided			
D/A converter	Provided			
Up/ down counter	2 channels			
Multi-function serial interface	2 channels			
CAN	64msb × 1 channel (ch.0)			
FlexRay	128msb × 1unit (ch.A / ch.B)	Not provided	128msb × 1unit (ch.A / ch.B)	Not provided
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	2 channels			
Low-voltage detection reset (Internal low-voltage detection)	Provided			
Low-voltage detection reset (External low-voltage detection)	Provided			
Device package	LQFP-64			
Debug interface	Built-in OCD (On Chip Debug Unit)			

Note: For details on the MB91580S series, see the "MB91580M/S Series HARDWARE MANUAL".

Pin No.	Pin name	I/O circuit type*	Function
22	P037	D	General-purpose I/O port
	ZIN0		Up/ down counter ch.0 ZIN input pin
	RDC_W		RDC phase W output pin
23	P040	D	General-purpose I/O port
	AIN1		Up/ down counter ch.1 AIN input pin
	RDC_A		RDC phase A output pin
24	P041	D	General-purpose I/O port
	BIN1		Up/ down counter ch.1 BIN input pin
	RDC_B		RDC phase B output pin
25	P042	D	General-purpose I/O port
	ZIN1		Up/ down counter ch.1 ZIN input pin
	RDC_Z		RDC phase Z output pin
26	RDC_ACT	J	RDC operation status output pin
27	MAG_OUT	I	RDC excitation signal output pin
28	MAG_PLUS	H	RDC excitation external input pin +
29	MAG_MINUS	H	RDC excitation external input pin -
30	COS_OUT	I	RDC COS output pin
31	COS_MINUS	H	RDC COS input pin -
32	COS_PLUS	H	RDC COS input pin +
33	SIN_PLUS	H	RDC SIN input pin +
34	SIN_MINUS	H	RDC SIN input pin -
35	SIN_OUT	I	RDC SIN output pin
38	COS_IN	H	RDC COS coil earth leakage detection input pin
39	SIN_IN	H	RDC SIN coil earth leakage detection input pin
41	AREF2	I	RDC Aref output (AVcc0/2) pin
44	P060	D	General-purpose I/O port
	MM		Clock supervisor main clock missing output pin
45	P061	D	General-purpose I/O port
	IN6		16-bit input capture ch.6 external pulse input pin
46	P062	D	General-purpose I/O port
	FRCK0		Free-run timer ch.0 external clock input pin
	SCS40		Multi-function serial ch.4 serial chip select 0 I/O pin
47	P063	D	General-purpose I/O port
	FRCK1		Free-run timer ch.1 external clock input pin
	SCS41		Multi-function serial ch.4 serial chip select 1 output pin
48	P064	D	General-purpose I/O port
	FRCK2		Free-run timer ch.2 external clock input pin
	SCS42		Multi-function serial ch.4 serial chip select 2 output pin
49	P065	D	General-purpose I/O port
	FRCK3		Free-run timer ch.3 external clock input pin
	SCS43		Multi-function serial ch.4 serial chip select 3 output pin
50	P066	D	General-purpose I/O port
	FRCK4		Free-run timer ch.4 external clock input pin
	SCS3		Multi-function serial ch.3 serial chip select I/O pin
51	P067	D	General-purpose I/O port
	FRCK5		Free-run timer ch.5 external clock input pin

Pin No.	Pin name	I/O circuit type*1	Function
124	P131	D	General-purpose I/O port
	ADTG0		A/D converter ch.0 to ch.7 external trigger input pin
125	P132	D	General-purpose I/O port
	ADTG1		A/D converter ch.8 to ch.15 external trigger input pin
	SCS1		Multi-function serial ch.1 serial chip select I/O pin
126	P133	D	General-purpose I/O port
	ADTG2		A/D converter ch.16 to ch.23 external trigger input pin
	TX2		CAN transmission data 2 output pin
127	P134	E	General-purpose I/O port
	STOPWT		FlexRay Stopwatch input pin
	RX2		CAN reception data 2 input pin
	INT7		INT7 external interrupt input pin
	IN7		16-bit input capture ch.7 external pulse input pin
110	DEBUGIF	L	DEBUG I/F pin
121	P136	D	General-purpose I/O port
	DTTI0		Waveform generator output stop signal input pin 0
	MONCLK		Clock monitor output pin
122	P137	D	General-purpose I/O port
	DTTI1		Waveform generator output stop signal input pin 1
40	AVCC0	-	*2
84	AVCC3	-	A/D converter analog power supply
42	AVRH0	-	*2
52	AVRH1	-	A/D converter upper limit reference voltage
62	AVRH2	-	A/D converter upper limit reference voltage
83	AVRH3	-	A/D converter upper limit reference voltage
43	AVSS0	-	*3
	AVRL0		*3
53	AVSS1	-	A/D converter GND
	AVRL1		A/D converter lower limit reference voltage
63	AVSS2	-	A/D converter GND
	AVRL2		A/D converter lower limit reference voltage
82	AVSS3	-	A/D converter GND
	AVRL3		A/D converter lower limit reference voltage
130	C	-	External capacity connection output pin
18, 36, 93, 72, 109, 128, 144	VCC5	-	+5.0V power supply
1, 19, 37, 73, 94, 108, 120, 129	VSS	-	GND

*1: For the I/O circuit types, see "■ I/O circuit type".
*2: The MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD do not use this pin. Connect it with the VCC5 pin.
*3: The MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD do not use this pin. Connect it with the VSS pin.

Type	Circuit	Remarks
L		Open drain I/O
M		• With analog input, I^2C, general-purpose I/O port • CMOS level output I_{OH}=-3mA, I_{OL}=3mA (at I^2C output) I_{OH}=-2/-5mA, I_{OL}=2/5mA (other than above) • With 50 kΩ pull-up resistor control • CMOS hysteresis input (0.7Vcc/0.3Vcc) • Automotive input (0.8Vcc/0.5Vcc)
N		• With analog output, general-purpose I/O port • CMOS level output I_{OH}=-2/-4mA, I_{OL}=2/4mA • With 50 kΩ pull-up resistor control • FlexRay input (0.7Vcc/0.3Vcc) • Automotive input (0.8Vcc/0.5Vcc)

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- Processing and Protection of Pins

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high-voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- Crystal oscillation circuit

  An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.
  The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

- Mode pin (MD[1:0])

  Connect the MD[1:0] mode pin to the VCC or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

- During power-on

  To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.

- Notes during PLL clock operation

  When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self oscillator circuit built in the PLL. This operation is not guaranteed.

- Treatment of R/D converter* and A/D converter power supply pins

  Connect the pins to have AVCC0 = AVCC3 = AVRH0 = AVRH1=AVRH2=AVRH3=VCC and AVSS0/AVRL0=AVSS1/AVRL1=AVSS2/AVRL2=AVSS3/AVRL3=VSS even if the R/D converter* and the A/D converter are not used.

- Note on using external clock

  The external clock is unsupported.
  External direct clock input cannot use.

- Power-on sequence of R/D converter* and A/D converter power supply analog inputs

  Be sure to turn on the digital power supply (VCC5) first, and then turn on the R/D converter* and A/D converter power supplies (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3, AVRL0*, AVRL1, AVRL2, AVRL3) and analog inputs (MAG_PLUS*, MAG_MINUS*, COS_PLUS*, COS_MINUS*, SIN_PLUS*, SIN_MINUS*, COS_IN*, SIN_IN*, AN0 to AN23). Also, turn off the R/D converter* and A/D converter power supplies (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3, AVRL0*, AVRL1, AVRL2, AVRL3) and analog inputs (MAG_PLUS*, MAG_MINUS*, COS_PLUS*, COS_MINUS*, SIN_PLUS*, SIN_MINUS*, COS_IN*, SIN_IN*, AN0 to AN23) first, and then turn off the digital power supply (VCC5). When the AVRH0*, AVRH1, AVRH2, and AVRH3 pin voltages are turned on or off, they must not exceed AVCC0* and AVCC3. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVCC0* or AVCC3. (However, the analog power supply voltage and digital power supply voltage can be turned on or off simultaneously.)

- Treatment of C pin

  This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

  *: MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC only

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001194_H	IPCP4[R] H,W 00000000 00000000		IPCP5[R] H,W 00000000 00000000		Input capture 4/5
001198_H	ICS45[R/W] B,H,W ------00 00000000		-	-	
$00119C_H$	IPCP6[R] H,W 00000000 00000000		IPCP7[R] H,W 00000000 00000000		Input capture 6/7
$0011A0_H$	ICS67[R/W] B,H,W ------00 00000000		-	-	
$0011A4_H$	DTSR[R/W] B,H,W ------10	-	-	-	DTTI selection
$0011A8_H$	TMRR0[R/W] H,W 00000000 00000001		TMRR1[R/W] H,W 00000000 00000001		Waveform generator 0/1/2
$0011AC_H$	TMRR2[R/W] H,W 00000000 00000001		-	-	
$0011B0_H$	DTSCR0[R/W] B,H,W 00000000	DTSCR1[R/W] B,H,W 00000000	DTSCR2[R/W] B,H,W 00000000	-	
$0011B4_H$	-	DTIR0[R/W] B,H,W 000000--	-	DTMNS0[R/W] B,H,W 00---000	
$0011B8_H$	-	SIGCR10[R/W] B,H,W 00000000	-	SIGCR20[R/W] B,H,W 000000-1	
$0011BC_H$	PICS0[R/W] B,H,W 000000-- -------- -------- --------				
$0011C0_H$	TMRR3[R/W] H,W 00000000 00000001		TMRR4[R/W] H,W 00000000 00000001		Waveform generator 3/4/5
$0011C4_H$	TMRR5[R/W] H,W 00000000 00000001		-	-	
$0011C8_H$	DTSCR3[R/W] B,H,W 00000000	DTSCR4[R/W] B,H,W 00000000	DTSCR5[R/W] B,H,W 00000000	-	
$0011CC_H$	-	DTIR1[R/W] B,H,W 000000--	-	DTMNS1[R/W] B,H,W 00---000	
$0011D0_H$	-	SIGCR11[R/W] B,H,W 00000000	-	SIGCR21[R/W] B,H,W 000000-1	
$0011D4_H$	PICS1[R/W] B,H,W 000000-- -------- -------- --------				
$0011D8_H$	-	-	-	-	12-bit A/D converter
$0011DC_H$	ADTSS[R/W] B,H,W -------0	-	-	-	
$0011E0_H$	ADTSE[R/W] B,H,W -------- 00000000 00000000 00000000				
$0011E4_H$	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		
$0011E8_H$	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
$0011EC_H$	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$002158_{H,}$ $00215C_H$	-		-		CAN 1 64msb
$002160_{H,}$ 002164_H	Reserved (IF2 data mirror)				
002168_H | $00217C_H$	-		-		
002180_H	TREQR21[R] B,H,W 00000000 00000000		TREQR11[R] B,H,W 00000000 00000000		
002184_H	TREQR41[R] B,H,W 00000000 00000000		TREQR31[R] B,H,W 00000000 00000000		
002188_H	-		-		
$00218C_H$	-		-		
002190_H	NEWDT21[R] B,H,W 00000000 00000000		NEWDT11[R] B,H,W 00000000 00000000		
002194_H	NEWDT41[R] B,H,W 00000000 00000000		NEWDT31[R] B,H,W 00000000 00000000		
002198_H	-		-		
$00219C_H$	-		-		
$0021A0_H$	INTPND21[R] B,H,W 00000000 00000000		INTPND11[R] B,H,W 00000000 00000000		
$0021A4_H$	INTPND41[R] B,H,W 00000000 00000000		INTPND31[R] B,H,W 00000000 00000000		
$0021A8_H$	-		-		
$0021AC_H$	-		-		
$0021B0_H$	MSGVAL21[R] B,H,W 00000000 00000000		MSGVAL11[R] B,H,W 00000000 00000000		
$0021B4_H$	MSGVAL41[R] B,H,W 00000000 00000000		MSGVAL31[R] B,H,W 00000000 00000000		
$0021B8_H$	-		-		
$0021BC_H$	-		-		
$0021C0_H$ | $0021FC_H$	-		-		
002200_H	CTRLR2[R/W] B,H,W -------- 000-0001		STATR2[R/W] B,H,W -------- 00000000		CAN 2 64msb
002204_H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2[R/W] B,H,W -0100011 00000001		
002208_H	INTR2[R] B,H,W 00000000 00000000		TESTR2[R/W] B,H,W -------- X00000--		
$00220C_H$	BRPER2[R/W] B,H,W -------- ----0000		-		
002210_H	IF1CREQ2[R/W] B,H,W 0------- 00000001		IF1CMSK2[R/W] B,H,W -------- 00000000		
002214_H	IF1MSK22[R/W] B,H,W 11-11111 11111111		IF1MSK12[R/W] B,H,W 11111111 11111111		
002218_H	IF1ARB22[R/W] B,H,W 00000000 00000000		IF1ARB12[R/W] B,H,W 00000000 00000000		
$00221C_H$	IF1MCTR2[R/W] B,H,W 00000000 0---0000		-		
002220_H	IF1DTA12[R/W] B,H,W 00000000 00000000		IF1DTA22[R/W] B,H,W 00000000 00000000		
002224_H	IF1DTB12[R/W] B,H,W 00000000 00000000		IF1DTB22[R/W] B,H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$002228_{H,}$ $00222C_H$	-		-		CAN 2 64msb
$002230_{H,}$ 002234_H	Reserved (IF1 data mirror)				
$002238_{H,}$ $00223C_H$	-		-		
002240_H	IF2CREQ2[R/W] B,H,W 0------- 00000001		IF2CMSK2[R/W] B,H,W -------- 00000000		
002244_H	IF2MSK22[R/W] B,H,W 11-11111 11111111		IF2MSK12[R/W] B,H,W 11111111 11111111		
002248_H	IF2ARB22[R/W] B,H,W 00000000 00000000		IF2ARB12[R/W] B,H,W 00000000 00000000		
$00224C_H$	IF2MCTR2[R/W] B,H,W 00000000 0---0000		-		
002250_H	IF2DTA12[R/W] B,H,W 00000000 00000000		IF2DTA22[R/W] B,H,W 00000000 00000000		
002254_H	IF2DTB12[R/W] B,H,W 00000000 00000000		IF2DTB22[R/W] B,H,W 00000000 00000000		
$002258_{H,}$ $00225C_H$	-		-		
$002260_{H,}$ 002264_H	Reserved (IF2 data mirror)				
002268_H | $00227C_H$	-		-		
002280_H	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		
002284_H	TREQR42[R] B,H,W 00000000 00000000		TREQR32[R] B,H,W 00000000 00000000		
002288_H	-		-		
$00228C_H$	-		-		
002290_H	NEWDT22[R] B,H,W 00000000 00000000		NEWDT12[R] B,H,W 00000000 00000000		
002294_H	NEWDT42[R] B,H,W 00000000 00000000		NEWDT32[R] B,H,W 00000000 00000000		
002298_H	-		-		
$00229C_H$	-		-		
$0022A0_H$	INTPND22[R] B,H,W 00000000 00000000		INTPND12[R] B,H,W 00000000 00000000		
$0022A4_H$	INTPND42[R] B,H,W 00000000 00000000		INTPND32[R] B,H,W 00000000 00000000		
$0022A8_H$	-		-		
$0022AC_H$	-		-		
$0022B0_H$	MSGVAL22[R] B,H,W 00000000 00000000		MSGVAL12[R] B,H,W 00000000 00000000		
$0022B4_H$	MSGVAL42[R] B,H,W 00000000 00000000		MSGVAL32[R] B,H,W 00000000 00000000		
$0022B8_H$	-		-		
$0022BC_H$	-		-		
$0022C0_H$ | $0022FC_H$	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000100_H	TMRLRA1[R/W] H XXXXXXXX XXXXXXXX		TMR1[R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104_H	TMRLRB1[R/W] H XXXXXXXX XXXXXXXX		TMCSR1[R/W] B,H,W 00000000 0-000000		
000108_H	TMRLRA2[R/W] H XXXXXXXX XXXXXXXX		TMR2[R] H XXXXXXXX XXXXXXXX		Reload timer 2
$00010C_H$	TMRLRB2[R/W] H XXXXXXXX XXXXXXXX		TMCSR2[R/W] B,H,W 00000000 0-000000		
000110_H	TMRLRA3[R/W] H XXXXXXXX XXXXXXXX		TMR3[R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114_H	TMRLRB3[R/W] H XXXXXXXX XXXXXXXX		TMCSR3[R/W] B,H,W 00000000 0-000000		
000118_H | $00011C_H$	-	-	-	-	Reserved
000120_H	IRPR0H[R] B,H,W 00------	IRPR0L[R] B,H,W 00------	IRPR1H[R] B,H,W 00------	IRPR1L[R] B,H,W --------	Interrupt request batch read register
000124_H	IRPR2H[R] B,H,W --------	IRPR2L[R] B,H,W 0000----	IRPR3H[R] B,H,W 00------	IRPR3L[R] B,H,W 00------	
000128_H	IRPR4H[R] B,H,W 00------	IRPR4L[R] B,H,W 000000--	IRPR5H[R] B,H,W 00------	IRPR5L[R] B,H,W 00------	
$00012C_H$	IRPR6H[R] B,H,W 000000--	IRPR6L[R] B,H,W 000000--	IRPR7H[R] B,H,W 000000--	IRPR7L[R] B,H,W 000000--	
000130_H	IRPR8H[R] B,H,W 000000--	IRPR8L[R] B,H,W 00------	IRPR9H[R] B,H,W 00------	IRPR9L[R] B,H,W 00------	
000134_H	IRPR10H[R] B,H,W 00------	IRPR10L[R] B,H,W 00------	IRPR11H[R] B,H,W 00------	IRPR11L[R] B,H,W 0000000-	
000138_H	IRPR12H[R] B,H,W 0000000-	IRPR12L[R] B,H,W 00000000	IRPR13H[R] B,H,W 00000000	IRPR13L[R] B,H,W 00000000	
$00013C_H$	IRPR14H[R] B,H,W 00------	IRPR14L[R] B,H,W 00------	IRPR15H[R] B,H,W 00000000	IRPR15L[R] B,H,W 00000---	
000140_H	IRPR16H[R] B,H,W 00------	IRPR16L[R] B,H,W 00------	IRPR17H[R] B,H,W 00------	IRPR17L[R] B,H,W 00------	
000144_H	IRPR18H[R] B,H,W 00------	IRPR18L[R] B,H,W 000000--	-	-	
000148_H | $0001FC_H$	-	-	-	-	Reserved
000200_H	PCN0[R/W] B,H,W 00000000 000000-0		PCSR0[W] H,W XXXXXXXX XXXXXXXX		PPG0
000204_H	PDUT0[W] H,W XXXXXXXX XXXXXXXX		PTMR0[R] H,W 11111111 11111111		
000208_H	PCN1[R/W] B,H,W 00000000 000000-0		PCSR1[W] H,W XXXXXXXX XXXXXXXX		PPG1
$00020C_H$	PDUT1[W] H,W XXXXXXXX XXXXXXXX		PTMR1[R] H,W 11111111 11111111		
000210_H	PCN2[R/W] B,H,W 00000000 000000-0		PCSR2[W] H,W XXXXXXXX XXXXXXXX		PPG2
000214_H	PDUT2[W] H,W XXXXXXXX XXXXXXXX		PTMR2[R] H,W 11111111 11111111		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000588_H | $00058C_H$	-	-	-	-	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H	ASR0[R/W] W 00000000 00000000 -------- 1111-001				External bus interface [S]
000604_H	ASR1[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608_H	ASR2[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
$00060C_H$	ASR3[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000610_H | $00063C_H$	-	-	-	-	Reserved[S]
000640_H	ACR0[R/W] W -------- -------- -------- 00--00--				External bus interface [S]
000644_H	ACR1[R/W] W -------- -------- -------- XX--XX--				
000648_H	ACR2[R/W] W -------- -------- -------- XX--XX--				
$00064C_H$	ACR3[R/W] W -------- -------- -------- XX--XX--				
000650_H | $00067C_H$	-	-	-	-	Reserved[S]
000680_H	AWR0[R/W] W ----1111 00000000 11110000 00000-0-				External bus interface [S]
000684_H	AWR1[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688_H	AWR2[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
$00068C_H$	AWR3[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690_H | $0006BC_H$	-	-	-	-	Reserved[S]
$0006C0_H$	DMAR0[R/W] W -------- -------- -------- ----0000				External bus interface [S]
$0006C4_H$	DMAR1[R/W] W -------- -------- -------- ----0000				
$0006C8_H$	DMAR2[R/W] W -------- -------- -------- ----0000				
$0006CC_H$	DMAR3[R/W] W -------- -------- -------- ----0000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002114_H	IF1MSK21[R/W] B,H,W 11-11111 11111111		IF1MSK11[R/W] B,H,W 11111111 11111111		CAN 1 64msb
002118_H	IF1ARB21[R/W] B,H,W 00000000 00000000		IF1ARB11[R/W] B,H,W 00000000 00000000		
$00211C_H$	IF1MCTR1[R/W] B,H,W 00000000 0---0000		-		
002120_H	IF1DTA11[R/W] B,H,W 00000000 00000000		IF1DTA21[R/W] B,H,W 00000000 00000000		
002124_H	IF1DTB11[R/W] B,H,W 00000000 00000000		IF1DTB21[R/W] B,H,W 00000000 00000000		
002128_H, $00212C_H$	-		-		
002130_H, 002134_H	Reserved (IF1 data mirror)				
002138_H, $00213C_H$	-		-		
002140_H	IF2CREQ1[R/W] B,H,W 0------- 00000001		IF2CMSK1[R/W] B,H,W -------- 00000000		
002144_H	IF2MSK21[R/W] B,H,W 11-11111 11111111		IF2MSK11[R/W] B,H,W 11111111 11111111		
002148_H	IF2ARB21[R/W] B,H,W 00000000 00000000		IF2ARB11[R/W] B,H,W 00000000 00000000		
$00214C_H$	IF2MCTR1[R/W] B,H,W 00000000 0---0000		-		
002150_H	IF2DTA11[R/W] B,H,W 00000000 00000000		IF2DTA21[R/W] B,H,W 00000000 00000000		
002154_H	IF2DTB11[R/W] B,H,W 00000000 00000000		IF2DTB21[R/W] B,H,W 00000000 00000000		
002158_H, $00215C_H$	-		-		
002160_H, 002164_H	Reserved (IF2 data mirror)				
002168_H | $00217C_H$	-		-		
002180_H	TREQR21[R] B,H,W 00000000 00000000		TREQR11[R] B,H,W 00000000 00000000		
002184_H	TREQR41[R] B,H,W 00000000 00000000		TREQR31[R] B,H,W 00000000 00000000		
002188_H	-		-		
$00218C_H$	-		-		
002190_H	NEWDT21[R] B,H,W 00000000 00000000		NEWDT11[R] B,H,W 00000000 00000000		
002194_H	NEWDT41[R] B,H,W 00000000 00000000		NEWDT31[R] B,H,W 00000000 00000000		
002198_H	-		-		
$00219C_H$	-		-		
$0021A0_H$	INTPND21[R] B,H,W 00000000 00000000		INTPND11[R] B,H,W 00000000 00000000		
$0021A4_H$	INTPND41[R] B,H,W 00000000 00000000		INTPND31[R] B,H,W 00000000 00000000		
$0021A8_H$	-		-		
$0021AC_H$	-		-		
$0021B0_H$	MSGVAL21[R] B,H,W 00000000 00000000		MSGVAL11[R] B,H,W 00000000 00000000		

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

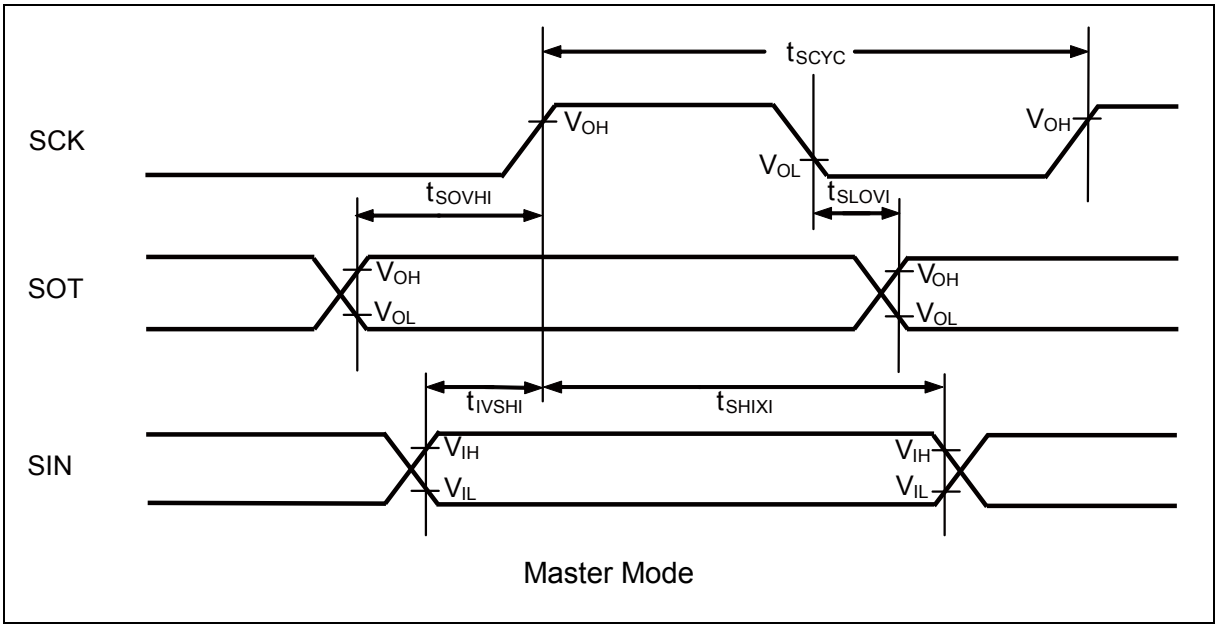
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input Leak Current	I_{IL}	All input pins	Vcc= AV_{CC}=5.5V $V_{SS} < V_I < V_{CC}$	-5	-	+5	µA	
Pull-up resistance	R_{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R_{UP2}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	When pull-up resistance is selected	25	-	100	kΩ	
Input Capacitor	C_{IN}	Other than VCC, VSS, AVCC, AVSS, C	-	-	5	15	pF	

*: Only available with MB91F585LB/F586LB/F587LB, MB91F585LD/F586LD/F587LD

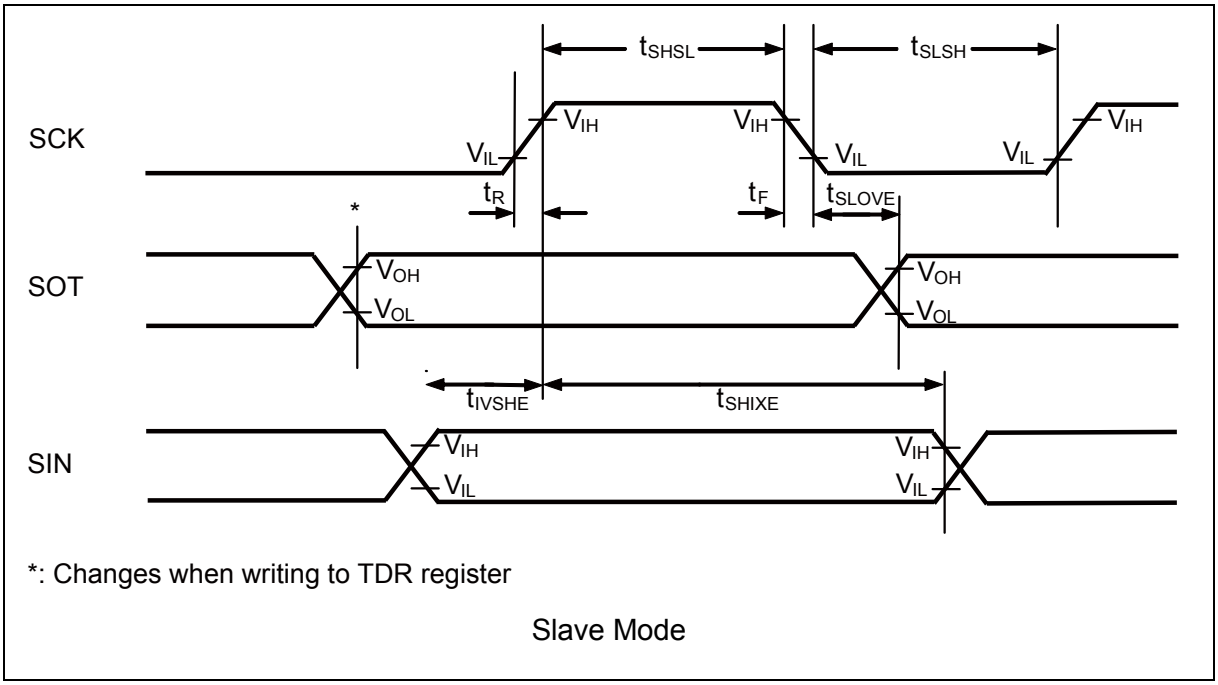
(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCS}	VCC5	CPU sleep F_{CP}=128MHz, F_{CPP}=32MHz	-	46	68	mA	*1, *2, *3, *4
	I_{CCBS}		Bus sleep F_{CP}=128MHz, F_{CPP}=32MHz	-	31	54	mA	*1, *2, *3, *4
	I_{CCT}		Clock mode 4MHz source oscillation	-	1.2	1.8	mA	When using external clock*6 T_A=25°C, *1, *2, *3, *4
				-	2.7	3.3	mA	When using crystal T_A=25°C, *1, *2, *3, *4
	I_{CCTS}		Clock mode shutdown 4MHz source oscillation	-	0.7	0.8	mA	When using external clock*6 T_A=25°C, *3, *4
				-	2.2	2.3	mA	When using crystal T_A=25°C, *3, *4
				-	0.3	0.4	mA	When using external clock*6 T_A=25°C, *1, *2
				-	1.8	1.9	mA	When using crystal T_A=25°C, *1, *2
	I_{CCH}		STOP mode	-	1.0	1.6	mA	T_A=25°C, *3, *4
				-	0.6	1.1	mA	T_A=25°C, *1, *2
	I_{CCHS}		STOP mode shutdown	-	0.5	0.6	mA	T_A=25°C, *3, *4
				-	0.1	0.2	mA	T_A=25°C, *1, *2

*1: MB91F585LA/F586LA/F587LA
*2: MB91F585LB/F586LB/F587LB
*3: MB91F585LC/F586LC/F587LC
*4: MB91F585LD/F586LD/F587LD
*6: The power supply current is the current value when the external clock is supplied from the X1 pin. Note that the power supply current value when using the external clock is different from that using the oscillator.

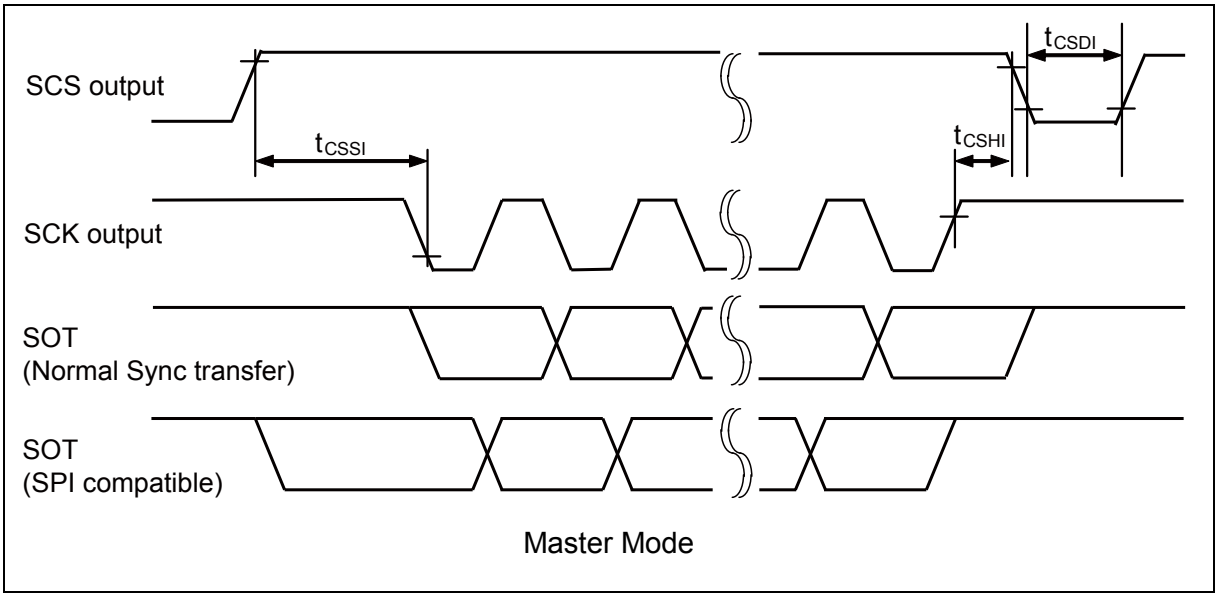


Master Mode

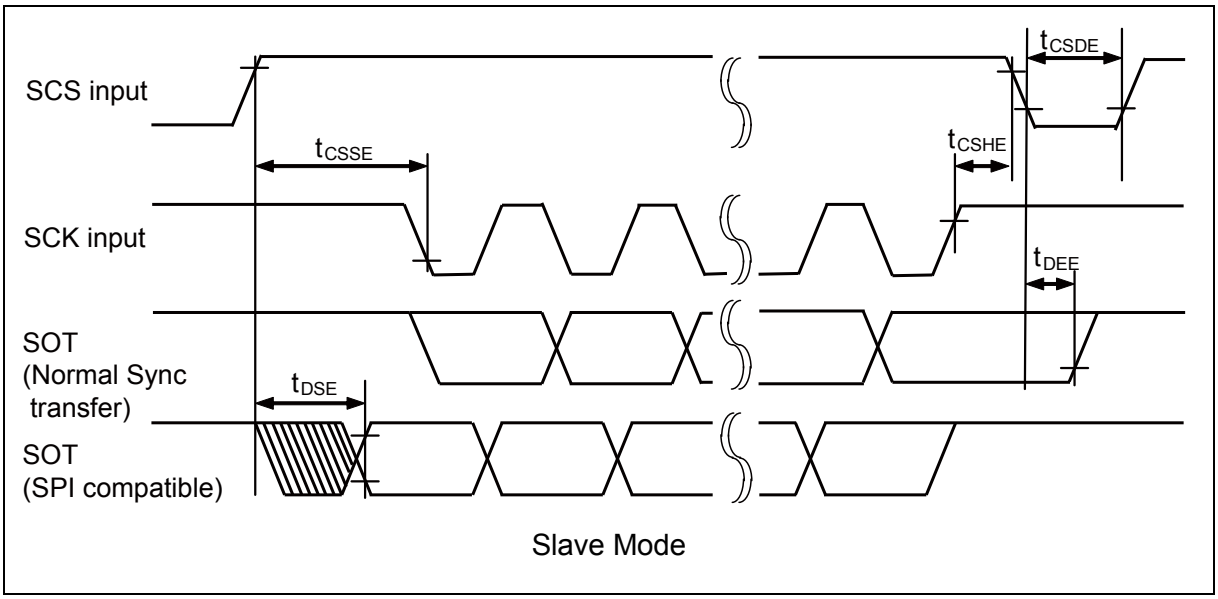


*: Changes when writing to TDR register

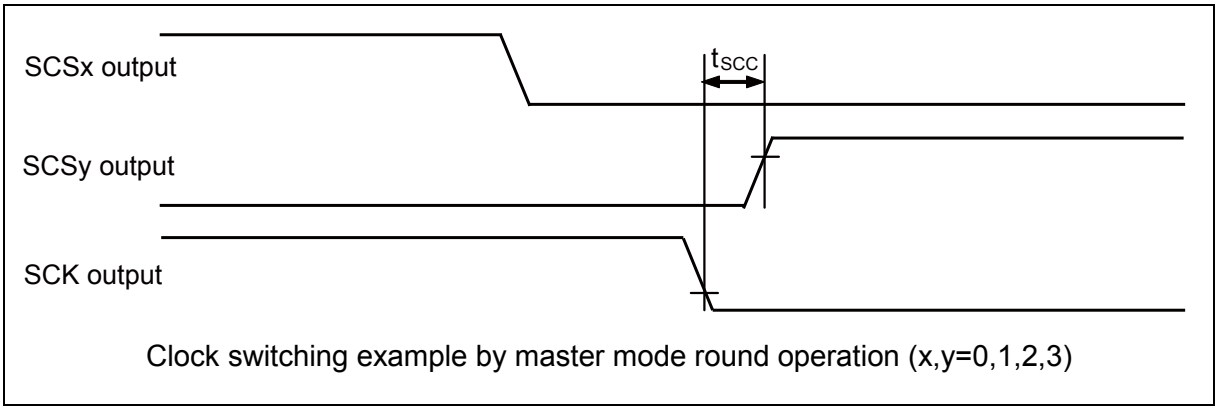
Slave Mode



Master Mode



Slave Mode



Clock switching example by master mode round operation (x,y=0,1,2,3)

(4-1-8) When the serial chip select is used (SCSCR:CSEN=1)

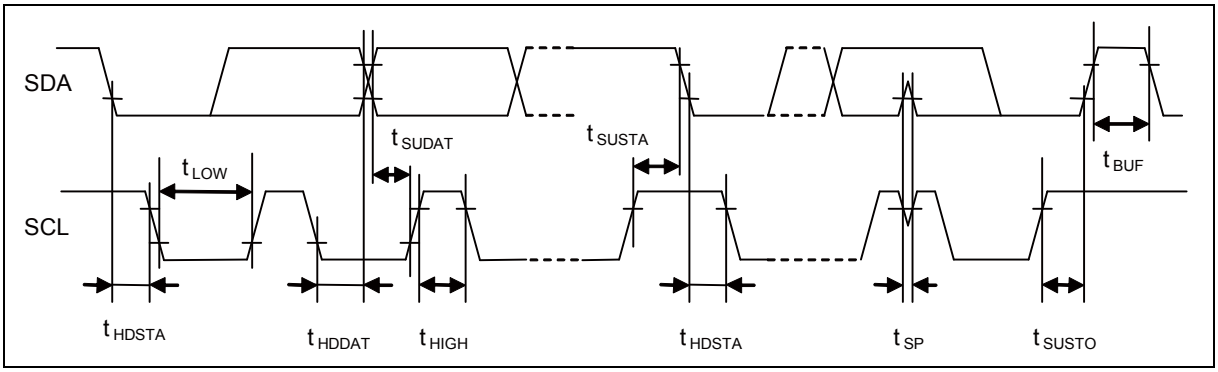
- Serial clock output signal detect level "L"(SMR,SCSFR:SCINV=1)
- Serial chip select inactive level "L"(SCSCR,SCSFR:CSLVL=0)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ ⇒ SCK ↑ setup time	t_{CSSI}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode C_L=50pF	t_{CSSU} *1+0	t_{CSSU} *1+50	ns	
SCK ↓ ⇒ SCS ↓ hold time	t_{CSHI}			t_{CSHD} *2-50	t_{CSHD} *2+0	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1		-50+5t_{CPP} +t_{CSDS} *3	+50+5t_{CPP} +t_{CSDS} *3	ns	
SCS ↑ ⇒ SCK ↑ setup time	t_{CSSE}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↓ ⇒ SCS ↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1		3t_{CPP}+30	-	ns	
SCS ↑ ⇒ SOT delay time	t_{DSE}	SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	40	ns	
SCS ↓ ⇒ SOT delay time	t_{DEE}			0	-	ns	
SCK ↑ ⇒ SCS ↑ clock switch time	t_{SCC}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode round operation C_L=50pF	3t_{CPP}+0	3t_{CPP}+50	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock
*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.


SDA
SCL
t LOW
t SUDAT
t SUSTA
t BUF
t HDSTA
t HDDAT
t HIGH
t HDSTA
t SP
t SUSTO

Page	Section	Change Results
137, 139, 141, 143	■ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4) Multi-function Serial (4-1) CSIO timing (SMR:MD2-0="010"b) (4-1-5) When the serial chip select is used (SCSCR:CSEN=1) • Serial clock output signal detect level "H" (SMR,SCSFR:SCINV=0) • Serial chip select inactive level "H" (SCSCR,SCSFR:CSLVL=1) (4-1-6) When the serial chip select is used (SCSCR:CSEN=1) • Serial clock output signal detect level "L" (SMR,SCSFR:SCINV=1) • Serial chip select inactive level "H" (SCSCR,SCSFR:CSLVL=1) (4-1-7) When the serial chip select is used (SCSCR:CSEN=1) • Serial clock output signal detect level "H" (SMR,SCSFR:SCINV=0) • Serial chip select inactive level "L" (SCSCR,SCSFR:CSLVL=0) (4-1-8) When the serial chip select is used (SCSCR:CSEN=1) • Serial clock output signal detect level "L" (SMR,SCSFR:SCINV=1) • Serial chip select inactive level "L" (SCSCR,SCSFR:CSLVL=0)	The specifications of t_{CSSI}, t_{CSHI} and t_{CSDI} are corrected. ·t_{CSSI} Min: -50-t_{CSSU} *1 Max: +0-t_{CSSU} *1 ↓ Min: t_{CSSU} *1+0 Max: t_{CSSU} *1+50 ·t_{CSHI} Min: +0+t_{CSHD} *2 Max: +50+t_{CSHD} *2 ↓ Min: t_{CSHD} *2-50 Max: t_{CSHD} *2+0 ·t_{CSDI} Min: -50+t_{CSDS} *3 Max: +50+t_{CSDS} *3 ↓ Min: -50+5t_{CPP}+t_{CSDS} *3 Max: +50+5t_{CPP}+t_{CSDS} *3
146	■ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4) Multi-function Serial (4-4) I^2C timing (SMR:MD2-0="100"b)	The explanatory note *1 is corrected. *1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. VP shows that the power supply voltage of the pull-up resistor and IOL shows the VOL guarantee current. ↓ *1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. VP shows that the power supply voltage of the pull-up resistor and IOL shows the VOL guarantee current.
162	■ELECTRICAL CHARACTERISTICS 7. Flash memory	Item name is changed. (1) Main Flash ↓ (1) Electrical Characteristics
162	■ELECTRICAL CHARACTERISTICS 7. Flash memory	The remark of " Erase cycle*2 / Data retention time " is corrected. Temperature at writing/erasing Tj <+105°C Average temperature T_A=+85°C *3 ↓ Average temperature T_A=+85°C *3
164	■ELECTRICAL CHARACTERISTICS 8. R/D Converter	The remark of " Amplitude" of "Resolver response signal*1 " is added. More than 2Vp-p
165-168	■EXAMPLE CHARACTERISTICS	"■EXAMPLE CHARACTERISTICS" is newly added.