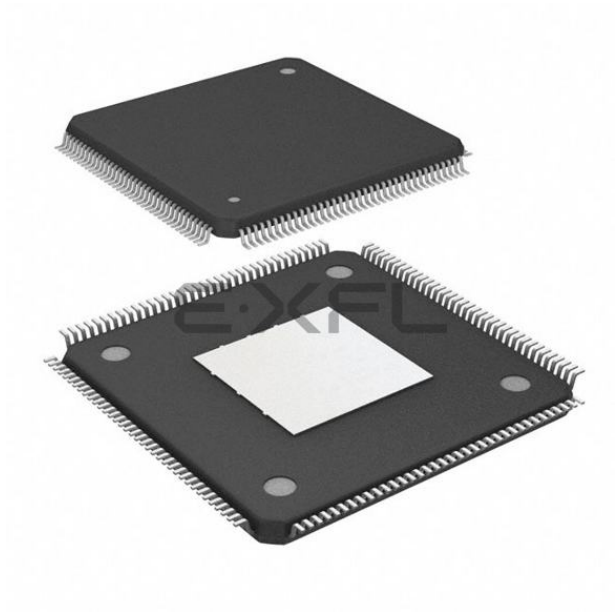
Infineon Technologies - XC2288H200F100LABKXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	1.6MB (1.6M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	138K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2288h200f100labkxuma1

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

XC228xH (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC228xH are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 10 ns instruction cycle @ 100 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1,024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 112 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 10 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - 24 Kbytes on-chip data SRAM (DSRAM)
  - Up to 112 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 1,600 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)

The XC228xH types are offered with several PSRAM memory sizes. **Figure 1** shows the allocation rules. For example 80 Kbytes of PSRAM will be allocated at E0’0000h-E1’3FFFh.

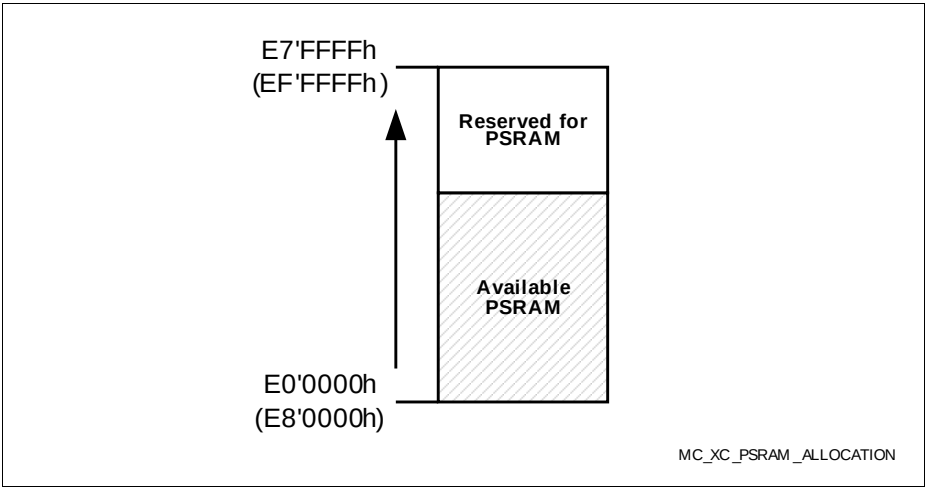

Figure 1 PSRAM Allocation

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
5	P8.4	O0 / I	St/B	**Bit 4 of Port 8, General Purpose Input/Output**
	CCU60_COUT61	O1	St/B	**CCU60 Channel 1 Output**
	CCU62_CC61	O2	St/B	**CCU62 Channel 1 Output**
	CC1_CC2	O3	St/B	**CC1 Channel 2 Output**
	TMS_D	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
	CCU62_CC61INB	I	St/B	**CCU62 Channel 1 Input**
	U4C1_DX1A	I	St/B	**USIC4 Channel 1 Shift Clock Input**
6	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC228xH's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.
7	P8.3	O0 / I	St/B	**Bit 3 of Port 8, General Purpose Input/Output**
	CCU60_COUT60	O1	St/B	**CCU60 Channel 0 Output**
	CCU62_CC60	O2	St/B	**CCU62 Channel 0 Output**
	U4C1_SELO0	O3	St/B	**USIC4 Channel 1 Select/Control 0 Output**
	TDI_D	IH	St/B	**JTAG Test Data Input** If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	CCU62_CC60INB	I	St/B	**CCU62 Channel 0 Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
52	P2.11	O0 / I	St/B	**Bit 11 of Port 2, General Purpose Input/Output**
	U0C0_SELO2	O1	St/B	**USIC0 Channel 0 Select/Control 2 Output**
	U0C1_SELO2	O2	St/B	**USIC0 Channel 1 Select/Control 2 Output**
	U3C1_DOUT	O3	St/B	**USIC3 Channel 1 Shift Data Output**
	$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	OH	St/B	**External Bus Interf. High-Byte Control Output** Can operate either as Byte High Enable ($\overline{\text{BHE}}$) or as Write strobe for High Byte ($\overline{\text{WRH}}$).
53	P11.5	O0 / I	St/B	**Bit 5 of Port 11, General Purpose Input/Output**
	CCU61_CC60	O1	St/B	**CCU61 Channel 0 Output**
	CCU61_COUT63	O2	St/B	**CCU61 Channel 3 Output**
	U3C1_SELO1	O3	St/B	**USIC3 Channel 1 Select/Control 1 Output**
	CCU61_CC60INB	I	St/B	**CCU61 Channel 0 Input**
	U3C1_DX2B	I	St/B	**USIC3 Channel 1 Shift Control Input**
	U4C0_DX2A	I	St/B	**USIC4 Channel 0 Shift Control Input**
55	P2.0	O0 / I	St/B	**Bit 0 of Port 2, General Purpose Input/Output**
	TxDC5	O1	St/B	**CAN Node 5 Transmit Data Output**
	CCU63_CC60	O2	St/B	**CCU63 Channel 0 Output**
	AD13	OH / IH	St/B	**External Bus Interface Address/Data Line 13**
	RxDC0C	I	St/B	**CAN Node 0 Receive Data Input**
	CCU63_CC60INB	I	St/B	**CCU63 Channel 0 Input**
	T5INB	I	St/B	**GPT12E Timer T5 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
59	P11.3	O0 / I	St/B	**Bit 3 of Port 11, General Purpose Input/Output**
	CCU61_COUT63	O1	St/B	**CCU61 Channel 3 Output**
	CCU61_COUT62	O2	St/B	**CCU61 Channel 2 Output**
	TxDC5	O3	St/B	**CAN Node 5 Transmit Data Input**
	CCU61_T13HRF	I	St/B	**External Run Control Input for T13 of CCU61**
	U4C0_DX1A	I	St/B	**USIC4 Channel 0 Shift Clock Input**
60	P4.0	O0 / I	St/B	**Bit 0 of Port 4, General Purpose Input/Output**
	CC2_CC24	O3 / I	St/B	**CAPCOM2 CC24IO Capture Inp./ Compare Out.**
	$\overline{CS0}$	OH	St/B	**External Bus Interface Chip Select 0 Output**
61	P2.3	O0 / I	St/B	**Bit 3 of Port 2, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU63_COUT63	O2	St/B	**CCU63 Channel 3 Output**
	CC2_CC16	O3 / I	St/B	**CAPCOM2 CC16IO Capture Inp./ Compare Out.**
	A16	OH	St/B	**External Bus Interface Address Line 16**
	ESR2_0	I	St/B	**ESR2 Trigger Input 0**
	U0C0_DX0E	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0D	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC0A	I	St/B	**CAN Node 0 Receive Data Input**
62	P11.2	O0 / I	St/B	**Bit 2 of Port 11, General Purpose Input/Output**
	CCU61_CC61	O1	St/B	**CCU61 Channel 1 Output**
	U3C1_DOUT	O2	St/B	**USIC3 Channel 1 Shift Data Output**
	U4C0_SELO1	O3	St/B	**USIC4 Channel 0 Select/Control 1 Output**
	CCU63_CCPOS2A	I	St/B	**CCU63 Position Input 2**
	CCU61_CC61INB	I	St/B	**CCU61 Channel 1 Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
81	P4.7	O0 / I	St/B	**Bit 7 of Port 4, General Purpose Input/Output**
	CC2_CC31	O3 / I	St/B	**CAPCOM2 CC31IO Capture Inp./ Compare Out.**
	T4EUDA	I	St/B	**GPT12E Timer T4 External Up/Down Control Input**
	CCU61_CCPOS2A	I	St/B	**CCU61 Position Input 2**
82	P2.9	O0 / I	St/B	**Bit 9 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CC2_CC22	O3 / I	St/B	**CAPCOM2 CC22IO Capture Inp./ Compare Out.**
	A22	OH	St/B	**External Bus Interface Address Line 22**
	CLKIN1	I	St/B	**Clock Signal Input 1**
	TCK_A	IH	St/B	**DAP0/JTAG Clock Input** If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
83	P0.2	O0 / I	St/B	**Bit 2 of Port 0, General Purpose Input/Output**
	U1C0_SCLKOUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_CC62	O3	St/B	**CCU61 Channel 2 Output**
	A2	OH	St/B	**External Bus Interface Address Line 2**
	U1C0_DX1B	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	CCU61_CC62INA	I	St/B	**CCU61 Channel 2 Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
90	P0.4	O0 / I	St/B	**Bit 4 of Port 0, General Purpose Input/Output**
	U1C1_SELO 0	O1	St/B	**USIC1 Channel 1 Select/Control 0 Output**
	U1C0_SELO 1	O2	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	CCU61_COU T61	O3	St/B	**CCU61 Channel 1 Output**
	A4	OH	St/B	**External Bus Interface Address Line 4**
	U1C1_DX2A	I	St/B	**USIC1 Channel 1 Shift Control Input**
	RxDC1B	I	St/B	**CAN Node 1 Receive Data Input**
	ESR2_8	I	St/B	**ESR2 Trigger Input 8**
92	P2.13	O0 / I	St/B	**Bit 13 of Port 2, General Purpose Input/Output**
	U2C1_SELO 2	O1	St/B	**USIC2 Channel 1 Select/Control 2 Output**
	U4C0_DOUT	O3	St/B	**USIC4 Channel 0 Shift Data Output**
	U4C0_DX0E	I	St/B	**USIC4 Channel 0 Shift Data Input**
	RxDC2D	I	St/B	**CAN Node 2 Receive Data Input**
93	P3.2	O0 / I	St/B	**Bit 2 of Port 3, General Purpose Input/Output**
	U2C0_SCLK OUT	O1	St/B	**USIC2 Channel 0 Shift Clock Output**
	TxDC3	O2	St/B	**CAN Node 3 Transmit Data Output**
	U2C0_DX1B	I	St/B	**USIC2 Channel 0 Shift Clock Input**
94	P2.10	O0 / I	St/B	**Bit 10 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_SELO 3	O2	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CC2_CC23	O3 / I	St/B	**CAPCOM2 CC23IO Capture Inp./ Compare Out.**
	A23	OH	St/B	**External Bus Interface Address Line 23**
	U0C1_DX0E	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CAPINA	I	St/B	**GPT12E Register CAPREL Capture Input**
	U3C1_DX0A	I	St/B	**USIC3 Channel 1 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
14, 54, 91, 127	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.
20	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.*
2, 36, 38, 72, 74, 108, 110, 144	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB}.*
1, 37, 73, 109	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane. *Note: Also the exposed pad is connected internally to V_{SS}. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground.* *For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.*

1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

Up to 24 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

8 Kbytes of on-chip Stand-By SRAM (SBRAM) provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC2000 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see **Table 8**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

The on-chip Flash memory stores code, constant data, and control data. The 1,600 Kbytes of on-chip Flash memory consist of 1 module of 64 Kbytes (preferably for data storage) and 6 modules of 256 Kbytes. Each module is organized in 4-Kbyte sectors.
The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen device type.

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.6**.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.4 Memory Protection Unit (MPU)

The XC228xH's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.5 Memory Checker Module (MCHK)

The XC228xH's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.15 FlexRay™ Protocol Controller (E-Ray)

The E-Ray module performs communication according to the FlexRay™ [1] protocol specification V2.1. With maximum specified clock the bitrate can be programmed to values up to 10 Mbit/s. Additional bus driver (BD) hardware is required for connection to the physical layer.

Figure 13 shows a global view of the E-Ray interface.

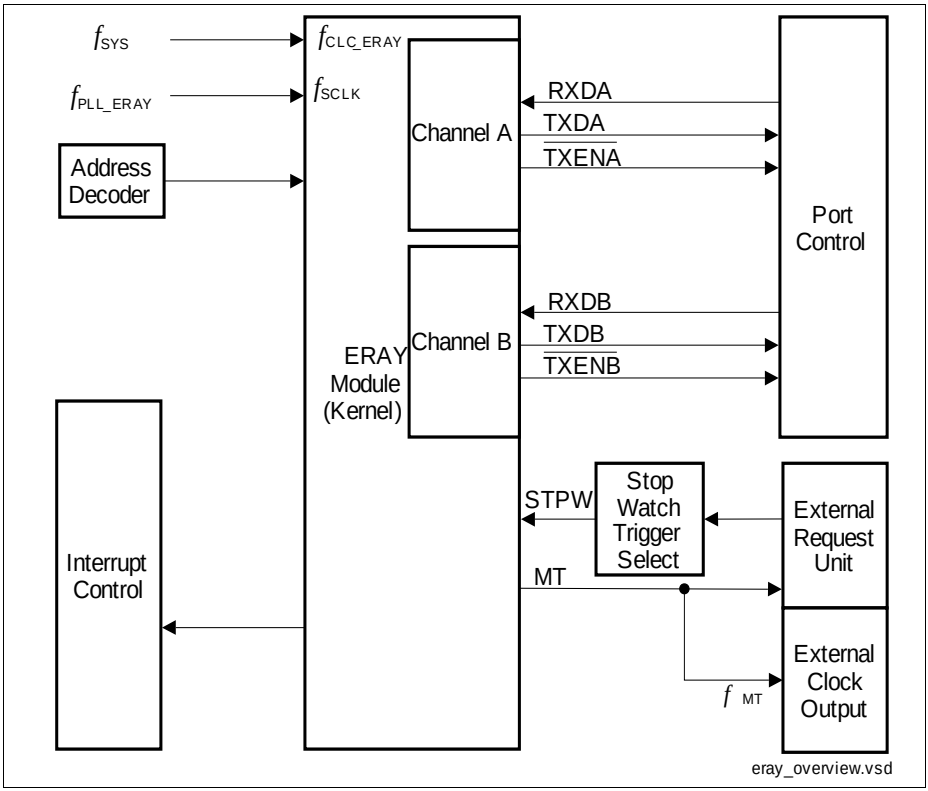

Figure 13 General Block Diagram of the E-Ray Interface

The E-Ray module communicates with the external world via three I/O lines each channel. The RXDAx and RXDBx lines are the receive data input signals, TXDA and TXDB lines are the transmit output signals, and $\overline{\text{TXENA}}$ and $\overline{\text{TXENB}}$ the transmit enable signals.

1) FlexRay™ is a trademark of the FlexRay Consortium.

3.16 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

3.17 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 µs and 13.4 s can be monitored (@ 80 MHz).

Time intervals between 2.56 µs and 10.71 s can be monitored (@ 100 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

3.18 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XC228xH from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.7.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

3.19 Parallel Ports

The XC228xH provides up to 119 I/O lines which are organized into 11 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 10**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Table 10 Summary of the XC228xH's Ports

Port	Width	I/O	Connected Modules
P0	8	I/O	EBC (A7...A0), CCU6, USIC, CAN
P1	8	I/O	EBC (A15...A8), CCU6, USIC
P2	14	I/O	EBC (READY, $\overline{\text{BHE}}$, A23...A16, AD15...AD13, D15...D13), CAN, CC2, GPT12E, USIC, DAP/JTAG
P3	8	I/O	CAN, USIC
P4	8	I/O	EBC ($\overline{\text{CS4}}$...$\overline{\text{CS0}}$), CC2, CAN, GPT12E, USIC
P5	16	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN, CC1
P6	4	I/O	ADC, CAN, GPT12E
P7	5	I/O	CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC
P8		I/O	CCU6, DAP/JTAG, CC1, USIC
P9	8	I/O	CCU6, DAP/JTAG, CAN, ERAY, CC1
P10	16	I/O	EBC (ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, AD12...AD0, D12...D0), CCU6, USIC, DAP/JTAG, CAN, ERAY
P11	6	I/O	CCU6, USIC, CAN
P15	8	I	Analog Inputs, GPT12E

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 21**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS}. The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

D_{Tmax} [ns] = ±(220 / (K2 × f_{SYS}) + 4.3)

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of **T** × TCS the accumulated jitter D_T is determined by:

D_T [ns] = D_{Tmax} × [(1 - 0.058 × K2) × (T - 1) / (0.83 × f_{SYS} - 1) + 0.058 × K2]

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

D_{max} = ±(220 / (4 × 33) + 4.3) = 5.97 ns (Not applicable directly in this case!)

D_3 = 5.97 × [(1 - 0.058 × 4) × (3 - 1) / (0.83 × 33 - 1) + 0.058 × 4]
= 5.97 × [0.768 × 2 / 26.39 + 0.232]
= 1.7 ns

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

D_{max} = ±(220 / (2 × 33) + 4.3) = 7.63 ns (Not applicable directly in this case!)

D_3 = 7.63 × [(1 - 0.058 × 2) × (3 - 1) / (0.83 × 33 - 1) + 0.058 × 2]
= 7.63 × [0.884 × 2 / 26.39 + 0.116]
= 1.4 ns

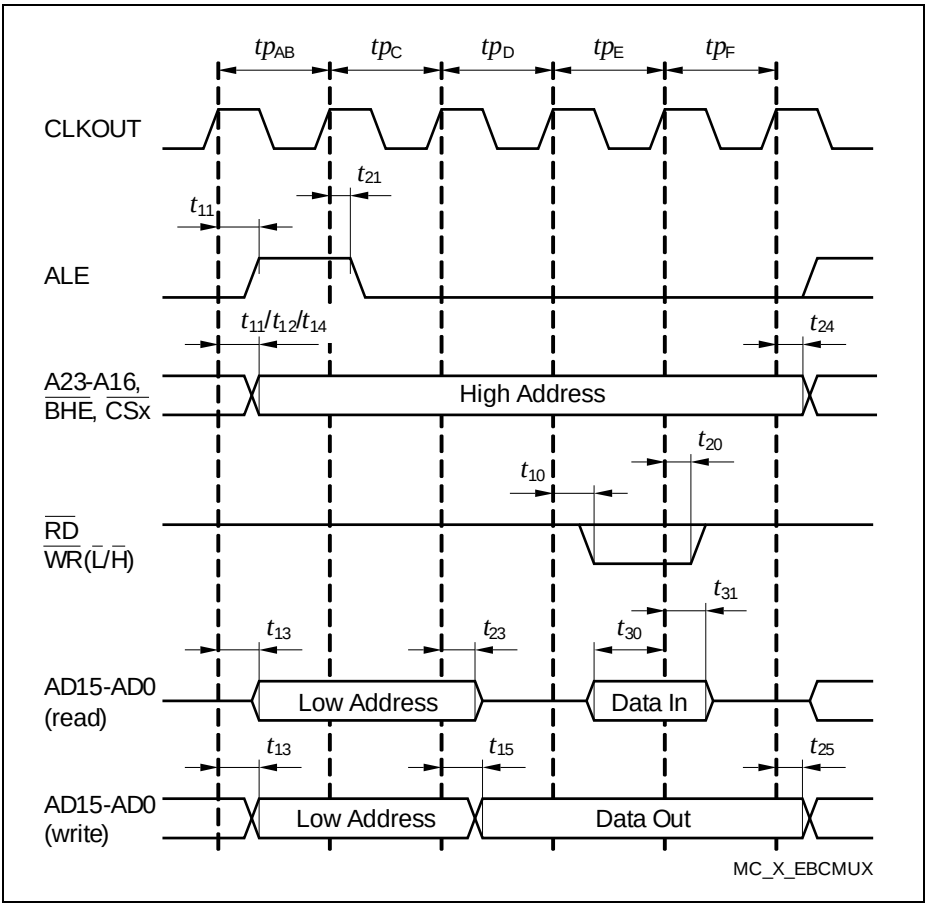

Figure 24 Multiplexed Bus Cycle

Table 36 USIC SSC Master Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 10[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 9[1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-7	–	11	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	40	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-5	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 37 is valid under the following conditions: C_L= 20 pF; *SSC*= slave ; voltage_range= upper

Table 37 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	7	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	

Table 41 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 41 DAP Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1)]	t_{11} SR	25	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time[1)]	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	3	–	–	ns	pad_type= high speed [2)]
		6	–	–	ns	pad_type= stan dard
DAP1 hold after DAP0 rising edge	t_{17} SR	4	–	–	ns	pad_type= high speed [2)]
		6	–	–	ns	pad_type= stan dard
DAP1 valid per DAP0 clock period[3)]	t_{19} CC	19	21	–	ns	pad_type= high speed [2)]
		12	17	–	ns	pad_type= stan dard

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) Available high speed pins can be found in the pin definitions table in chapter 2.

3) The Host has to find a suitable sampling point by analyzing the sync telegram response.

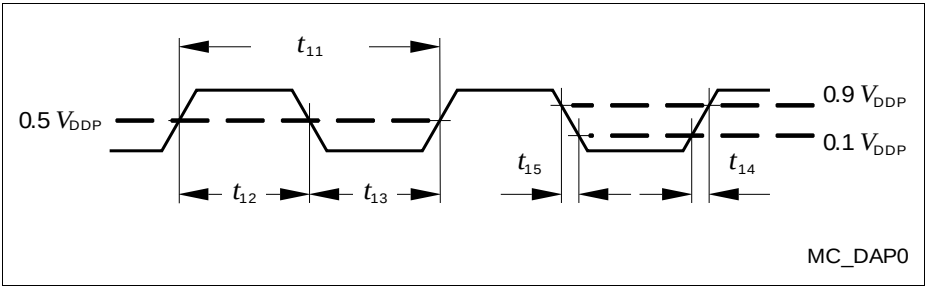

Figure 29 Test Clock Timing (DAP0)

Table 42 JTAG Interface Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[2]	t_8 CC	–	25	29	ns	
TDO high impedance to valid output from TCK falling edge[3][2]	t_9 CC	–	25	29	ns	
TDO valid output to high impedance from TCK falling edge[2]	t_{10} CC	–	25	29	ns	
TDO hold after TCK falling edge[2]	t_{18} CC	5	–	–	ns	

1) Under typical conditions, the JTAG interface can operate at transfer rates up to 20 MHz.
2) The falling edge on TCK is used to generate the TDO timing.
3) The setup time for TDO is given implicitly by the TCK cycle time.

Table 43 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 43 JTAG Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	–	–	ns	
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	

Table 43 JTAG Interface Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[1]	t_8 CC	–	32	36	ns	
TDO high impedance to valid output from TCK falling edge[2)1]	t_9 CC	–	32	36	ns	
TDO valid output to high impedance from TCK falling edge[1]	t_{10} CC	–	32	36	ns	
TDO hold after TCK falling edge[1]	t_{18} CC	5	–	–	ns	

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

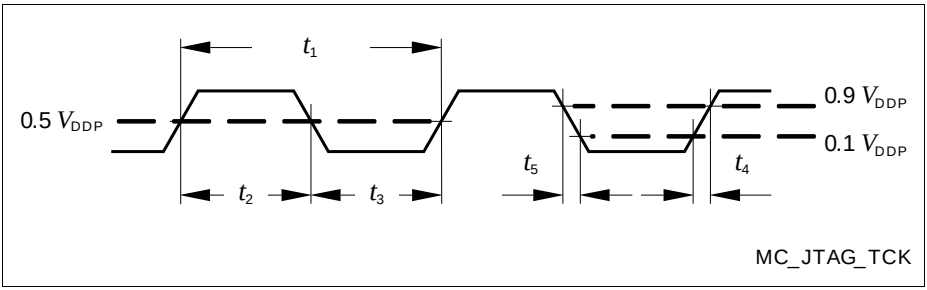

Figure 32 Test Clock Timing (TCK)