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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 317000 |
| Number of Logic Elements/Cells | 840000 |
| Total RAM Bits | 53248000 |
| Number of I/O | 840 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1932-BBGA, FCBGA |
| Supplier Device Package | 1932-FBGA, FC (45x45) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5see9f45i3l |

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

**Table 5. Maximum Allowed Overshoot During Transitions**

| Symbol | Description | Condition (V) | Overshoot Duration as % @ $T_J$ = 100°C | Unit |
|---|---|---|---|---|
| Vi (AC) | AC input voltage | 3.8 | 100 | % |
| | | 3.85 | 64 | % |
| | | 3.9 | 36 | % |
| | | 3.95 | 21 | % |
| | | 4 | 12 | % |
| | | 4.05 | 7 | % |
| | | 4.1 | 4 | % |
| | | 4.15 | 2 | % |
| | | 4.2 | 1 | % |

**Figure 1. Stratix V Device Overshoot Duration**

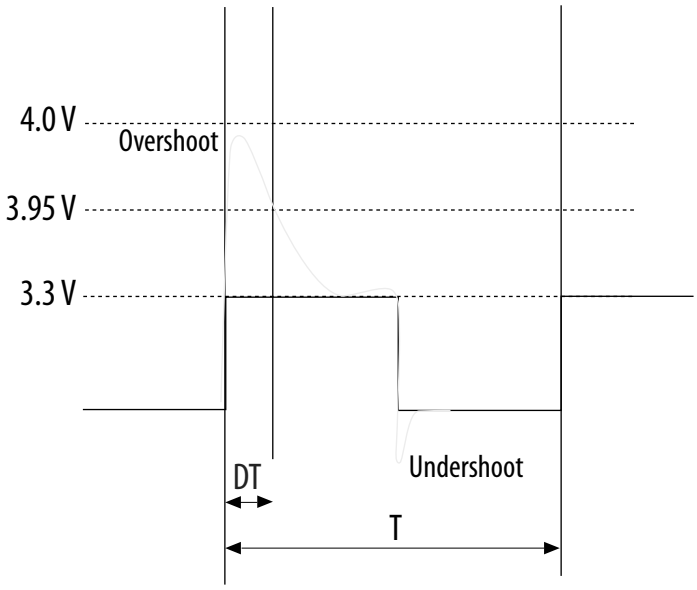


**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

| Symbol | Description | Devices | Minimum (4) | Typical | Maximum (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCR\_GXBR}$ (2) | Receiver analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCR\_GTBR}$ | Receiver analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCT\_GXBL}$ (2) | Transmitter analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT\_GXBR}$ (2) | Transmitter analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT\_GTBR}$ | Transmitter analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCL\_GTBR}$ | Transmitter clock network power supply | GT | 1.02 | 1.05 | 1.08 | V |
| $V_{CCH\_GXBL}$ | Transmitter output buffer power supply (left side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |
| $V_{CCH\_GXBR}$ | Transmitter output buffer power supply (right side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |

**Notes to Table 7:**

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) (1)**

| Symbol | Description | $V_{CCIO}$ (V) | Typical | Unit |
|---|---|---|---|---|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/°C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

**Note to Table 13:**

(1) Valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0° to 85°C.

### Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

**Table 14. Pin Capacitance for Stratix V Devices**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on the top and bottom I/O pins | 6 | pF |
| $C_{IOLR}$ | Input capacitance on the left and right I/O pins | 6 | pF |
| $C_{OUTFB}$ | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

### Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

**Table 15. Hot Socketing Specifications for Stratix V Devices**

| Symbol | Description | Maximum |
|---|---|---|
| $I_{IOPIN\ (DC)}$ | DC current per I/O pin | 300 µA |
| $I_{IOPIN\ (AC)}$ | AC current per I/O pin | 8 mA (1) |
| $I_{XCVR\text{-}TX\ (DC)}$ | DC current per transceiver transmitter pin | 100 mA |
| $I_{XCVR\text{-}RX\ (DC)}$ | DC current per transceiver receiver pin | 50 mA |

**Note to Table 15:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25* $V_{CCIO}$ | 0.75* $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25* $V_{CCIO}$ | 0.75* $V_{CCIO}$ | 16 | –16 |
| HSUL-12 | — | $V_{REF}$ – 0.13 | $V_{REF}$ + 0.13 | — | $V_{REF}$ – 0.22 | $V_{REF}$ + 0.22 | 0.1* $V_{CCIO}$ | 0.9* $V_{CCIO}$ | — | — |

**Table 20. Differential SSTL I/O Standards for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.2 | — | $V_{CCIO}/2$ + 0.2 | 0.62 | $V_{CCIO}$ + 0.6 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.175 | — | $V_{CCIO}/2$ + 0.175 | 0.5 | $V_{CCIO}$ + 0.6 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | *(1)* | $V_{CCIO}/2$ – 0.15 | — | $V_{CCIO}/2$ + 0.15 | 0.35 | — |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.2 | *(1)* | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | *(1)* | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | — |
| SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.18 | — | $V_{REF}$ –0.15 | $V_{CCIO}/2$ | $V_{REF}$ + 0.15 | –0.30 | 0.30 |

**Note to Table 20:**

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 4 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors (21) | 85–Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100–Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120–Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |
| | 150-Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |
| $V_{ICM}$ (AC and DC coupled) | $V_{CCR\_GXB}$ = 0.85 V or 0.9 V full bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR\_GXB}$ = 0.85 V or 0.9 V half bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR\_GXB}$ = 1.0 V/1.05 V full bandwidth | — | 700 | — | — | 700 | — | — | 700 | — | mV |
| | $V_{CCR\_GXB}$ = 1.0 V half bandwidth | — | 750 | — | — | 750 | — | — | 750 | — | mV |
| $t_{LTR}$ (11) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$ (12) | — | 4 | — | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD\_manual}$ (13) | — | 4 | — | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR\_LTD\_manual}$ (14) | — | 15 | — | — | 15 | — | — | 15 | — | — | µs |
| Run Length | — | — | — | 200 | — | — | 200 | — | — | 200 | UI |
| Programmable equalization (AC Gain) (10) | Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz) | — | — | 16 | — | — | 16 | — | — | 16 | dB |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 5 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 2 | — | — | 2 | — | — | 2 | — | dB |
| | DC Gain Setting = 2 | — | 4 | — | — | 4 | — | — | 4 | — | dB |
| | DC Gain Setting = 3 | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| | DC Gain Setting = 4 | — | 8 | — | — | 8 | — | — | 8 | — | dB |
| **Transmitter** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Rise time (7) | 20% to 80% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Fall time (7) | 80% to 20% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | — | — | 120 | ps |

Figure 6 shows the Stratix V DC gain curves for GT channels.

**Figure 6. DC Gain Curves for GT Channels**

## Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

# Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

## Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

**Table 30. Clock Tree Performance for Stratix V Devices** *(1)*

| Symbol | Performance | | | Unit |
|---|---|---|---|---|
| | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 | |
| Global and Regional Clock | 717 | 650 | 580 | MHz |
| Periphery Clock | 550 | 500 | 500 | MHz |

**Note to Table 30:**

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

## PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

**Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (C1, C2, C2L, I2, and I2L speed grades) | 5 | — | 800 (1) | MHz |
| | Input clock frequency (C3, I3, I3L, and I3YY speed grades) | 5 | — | 800 (1) | MHz |
| | Input clock frequency (C4, I4 speed grades) | 5 | — | 650 (1) | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{FINPFD}$ | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| $f_{VCO}$ (9) | PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C3, I3, I3L, I3YY speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grades) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades) | — | — | 717 (2) | MHz |
| | Output frequency for an internal global or regional clock (C3, I3, I3L speed grades) | — | — | 650 (2) | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grades) | — | — | 580 (2) | MHz |
| $f_{OUT\_EXT}$ | Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades) | — | — | 800 (2) | MHz |
| | Output frequency for an external clock output (C3, I3, I3L speed grades) | — | — | 667 (2) | MHz |
| | Output frequency for an external clock output (C4, I4 speed grades) | — | — | 553 (2) | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to **50%**) | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic Configuration Clock used for `mgmt_clk` and `scanclk` | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from the end-of-device configuration or deassertion of `areset` | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth (7) | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | 10 | — | — | ns |

**Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{INCCJ}$ (3), (4) | Input clock cycle-to-cycle jitter ($f_{REF} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter ($f_{REF} < 100$ MHz) | –750 | — | +750 | ps (p-p) |
| $t_{OUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output ($f_{OUT} \geq 100$ MHz) | — | — | 175 (1) | ps (p-p) |
| | Period Jitter for dedicated clock output ($f_{OUT} < 100$ MHz) | — | — | 17.5 (1) | mUI (p-p) |
| $t_{FOUTPJ\_DC}$ (5) | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ (5) | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTCCJ\_DC}$ (5) | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 250 (11), 175 (12) | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100$ MHz)+ | — | — | 25 (11), 17.5 (12) | mUI (p-p) |
| $t_{OUTPJ\_IO}$ (5), (8) | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{FOUTPJ\_IO}$ (5), (8), (11) | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{OUTCCJ\_IO}$ (5), (8) | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz) | — | — | 60 (10) | mUI (p-p) |
| $t_{FOUTCCJ\_IO}$ (5), (8), (11) | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 (10) | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{CASC\_OUTPJ\_DC}$ (5), (6) | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $f_{DRIFT}$ | Frequency drift after PFDENA is disabled for a duration of 100 µs | — | — | ±10 | % |
| $dK_{BIT}$ | Bit number of Delta Sigma Modulator (DSM) | 8 | 24 | 32 | Bits |
| $k_{VALUE}$ | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |

**Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{RES}$ | Resolution of VCO frequency ($f_{INPFD}$ = 100 MHz) | 390625 | 5.96 | 0.023 | Hz |

**Notes to Table 31:**

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $f_{OUT}$ of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.

(4) $f_{REF}$ is fIN/N when N = 1.

(5) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.

(6) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(7) High bandwidth PLL settings are not supported in external feedback mode.

(8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.

(9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(10) This specification only covers fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.05 - 0.95 must be ≥ 1000 MHz, while $f_{VCO}$ for fractional value range 0.20 - 0.80 must be ≥ 1200 MHz.

(11) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.05-0.95 must be ≥ 1000 MHz.

(12) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.20-0.80 must be ≥ 1200 MHz.

## DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)**

| Mode | Peformance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | C1 | C2, C2L | I2, I2L | C3 | I3, I3L, I3YY | C4 | I4 | |
| **Modes using one DSP** | | | | | | | | |
| Three 9 x 9 | 600 | 600 | 600 | 480 | 480 | 420 | 420 | MHz |
| One 18 x 18 | 600 | 600 | 600 | 480 | 480 | 420 | 400 | MHz |
| Two partial 18 x 18 (or 16 x 16) | 600 | 600 | 600 | 480 | 480 | 420 | 400 | MHz |
| One 27 x 27 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 36 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of two 18 x 18(One sum of 2 16 x 16) | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of square | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 18 x 18 plus 36 (a x b) + c | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| **Modes using two DSPs** | | | | | | | | |
| Three 18 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One sum of four 18 x 18 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |
| One sum of two 27 x 27 | 465 | 465 | 450 | 380 | 380 | 300 | 290 | MHz |
| One sum of two 36 x 18 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |
| One complex 18 x 18 | 500 | 500 | 500 | 400 | 400 | 350 | 350 | MHz |
| One 36 x 36 | 475 | 475 | 475 | 380 | 380 | 300 | 300 | MHz |

# Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

☞ The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

**Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)**

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK\_in}$ (input clock frequency) True Differential I/O Standards | Clock boost factor W = 1 to 40 (4) | 5 | — | 800 | 5 | — | 800 | 5 | — | 625 | 5 | — | 525 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) Single Ended I/O Standards (3) | Clock boost factor W = 1 to 40 (4) | 5 | — | 800 | 5 | — | 800 | 5 | — | 625 | 5 | — | 525 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) Single Ended I/O Standards | Clock boost factor W = 1 to 40 (4) | 5 | — | 520 | 5 | — | 520 | 5 | — | 420 | 5 | — | 420 | MHz |
| $f_{HSCLK\_OUT}$ (output clock frequency) | — | 5 | — | 800 | 5 | — | 800 | 5 | — | 625 (5) | 5 | — | 525 (5) | MHz |

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

**Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled**

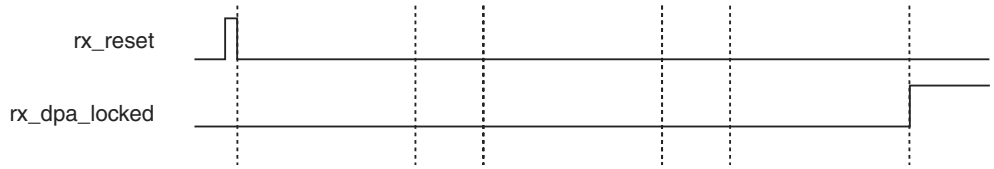



Table 37 lists the DPA lock time specifications for Stratix V devices.

**Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only** *(1), (2), (3)*

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions *(4)* | Maximum |
|---|---|---|---|---|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

**Notes to Table 37:**

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in this table applies to both commercial and industrial grade.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

**Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps**

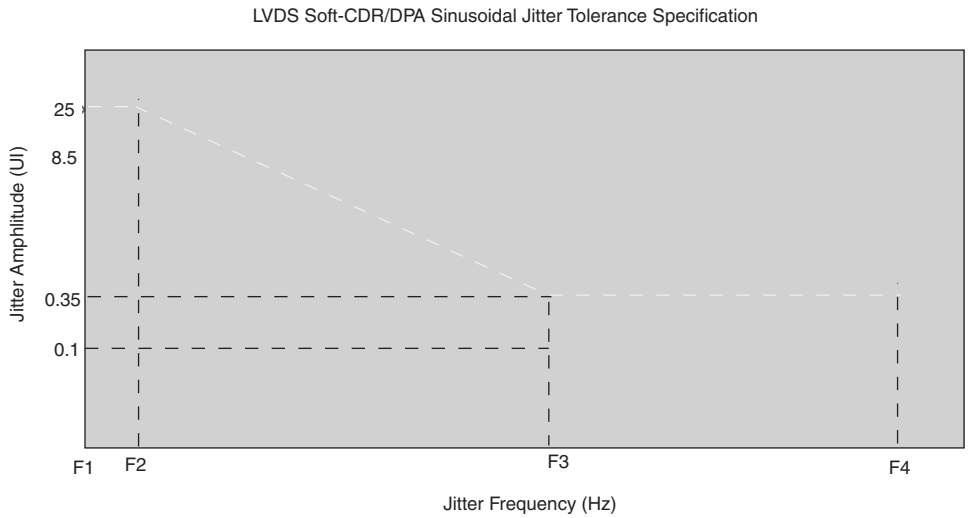


**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) (4), (5) |
|---|---|---|---|---|
| Stratix V E (1) | 5SEE9 | — | 342,742,976 | 700,888 |
| | 5SEEB | — | 342,742,976 | 700,888 |

**Notes to Table 47:**

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
(2) 36-transceiver devices.
(3) 24-transceiver devices.
(4) File size for the periphery image.
(5) The IOCSR **.rbf** size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (**.hex**) or tabular text file (**.ttf**) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GX | A3 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | A4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | A5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | AB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | B5 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B6 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | BB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| GT | C5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | C7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GS | D3 | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D5 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | D6 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| | D8 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| E | E9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | EB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |

**Notes to Table 48:**

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

## DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[] ratio for each combination.

**Table 49. DCLK-to-DATA[] Ratio (1) (Part 1 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

**Table 49. DCLK-to-DATA[] Ratio (1) (Part 2 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×32 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 4 |
| | Enabled | Disabled | 8 |
| | Enabled | Enabled | 8 |

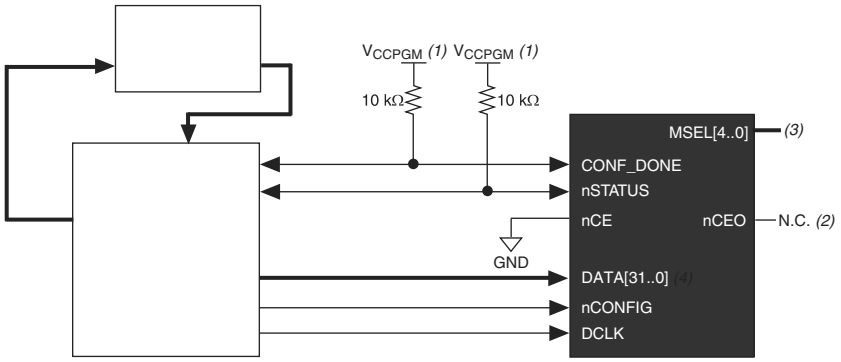
**Note to Table 49:**

(1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

**Figure 11. Single Device FPP Configuration Using an External Host**




**Notes to Figure 11:**

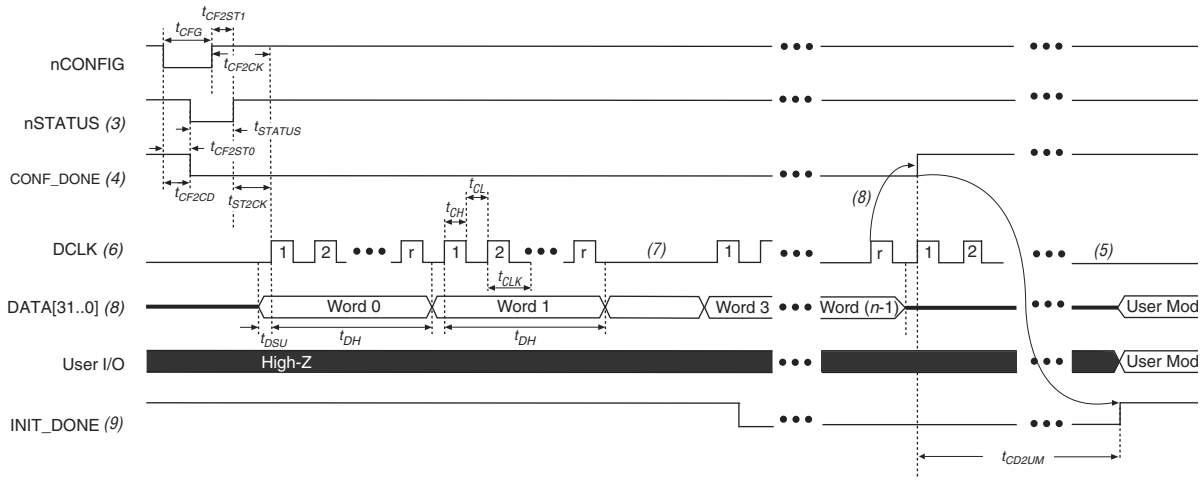
(1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device. $V_{CCPGM}$ must be high enough to meet the $V_{IH}$ specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with $V_{CCPGM}$.

(2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.

(3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(4) If you use FPP ×8, use DATA[7..0]. If you use FPP ×16, use DATA[15..0].

**Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1** *(1), (2)*




**Notes to Figure 13:**

(1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.

(2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.

(4) After power-up, before and during configuration, CONF_DONE is low.

(5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.

(7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.

(8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model | | Slow Model | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.793 | 2.793 | 2.992 | 3.192 | 2.811 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.838 | 0.838 | 0.924 | 1.011 | 0.843 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.415 | 0.415 | 0.458 | 0.503 | 0.418 | 0.456 | 0.499 | ns |

**Notes to Table 58:**

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

(2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)**

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $D_{OUTBUF}$ | Rising and/or falling edge delay | 0 (default) | ps |
| | | 25 | ps |
| | | 50 | ps |
| | | 75 | ps |

**Note to Table 59:**

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

# Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| **A**<br>B<br>C | — | — |
| **D** | — | — |
| **E** | — | — |
| **F** | $f_{HSCLK}$ | Left and right PLL input clock frequency. |
| | $f_{HSDR}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| | $f_{HSDRDPA}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |

**Table 60. Glossary (Part 4 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| V | $V_{CM(DC)}$ | DC common mode input voltage. |
| | $V_{ICM}$ | Input common mode voltage—The common mode of the differential signal at the receiver. |
| | $V_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| | $V_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage |
| | $V_{IH(DC)}$ | High-level DC input voltage |
| | $V_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage |
| | $V_{IL(DC)}$ | Low-level DC input voltage |
| | $V_{OCM}$ | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| | $V_{OD}$ | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| | $V_{SWING}$ | Differential input voltage |
| | $V_X$ | Input differential cross point voltage |
| | $V_{OX}$ | Output differential cross point voltage |
| W | W | High-speed I/O block—clock boost factor |
| X<br>Y<br>Z | — | — |

# Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

| Date | Version | Changes |
|---|---|---|
| June 2018 | 3.9 | ■ Added the “Stratix V Device Overshoot Duration” figure. |
| April 2017 | 3.8 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “PS Timing Parameters for Stratix V Devices” table.<br>■ Changed the condition for 100-Ω $R_D$ in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table. |
| June 2016 | 3.7 | ■ Added the $V_{ID}$ minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table<br>■ Added the $I_{OUT}$ specification to the “Absolute Maximum Ratings for Stratix V Devices” table. |
| December 2015 | 3.6 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. |
| December 2015 | 3.5 | ■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table. |
| July 2015 | 3.4 | ■ Changed the data rate specification for transceiver speed grade 3 in the following tables:<br>  ■ “Transceiver Specifications for Stratix V GX and GS Devices”<br>  ■ “Stratix V Standard PCS Approximate Maximum Date Rate”<br>  ■ “Stratix V 10G PCS Approximate Maximum Data Rate”<br>■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the $t_{CO}$ maximum value in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table.<br>■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table. |