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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 359250 |
| Number of Logic Elements/Cells | 952000 |
| Total RAM Bits | 53248000 |
| Number of I/O | 840 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1932-BBGA, FCBGA |
| Supplier Device Package | 1932-FBGA, FC (45x45) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5seebf45i3ln |

Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

| Symbol | Description | Condition | Min ⁽⁴⁾ | Typ | Max ⁽⁴⁾ | Unit |
|-----------------------------------|---|------------|--------------------|------|--------------------|------|
| V _{CC} | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades) | — | 0.87 | 0.9 | 0.93 | V |
| | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾ | — | 0.82 | 0.85 | 0.88 | V |
| V _{CCPT} | Power supply for programmable power technology | — | 1.45 | 1.50 | 1.55 | V |
| V _{CC_AUX} | Auxiliary supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCPD} ⁽¹⁾ | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCIO} | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.35 V) power supply | — | 1.283 | 1.35 | 1.45 | V |
| | I/O buffers (1.25 V) power supply | — | 1.19 | 1.25 | 1.31 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| V _{CCPGM} | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| V _{CCA_FPLL} | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCD_FPLL} | PLL digital voltage regulator power supply | — | 1.45 | 1.5 | 1.55 | V |
| V _{CCBAT} ⁽²⁾ | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| V _I | DC input voltage | — | −0.5 | — | 3.6 | V |
| V _O | Output voltage | — | 0 | — | V _{CCIO} | V |
| T _J | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | −40 | — | 100 | °C |

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

| Symbol | Description | Condition | Min ⁽⁴⁾ | Typ | Max ⁽⁴⁾ | Unit |
|-------------------|------------------------|--------------|--------------------|-----|--------------------|------|
| t _{RAMP} | Power supply ramp time | Standard POR | 200 μ s | — | 100 ms | — |
| | | Fast POR | 200 μ s | — | 4 ms | — |

Notes to Table 6:

- (1) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.
- (2) If you do not use the design security feature in Stratix V devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V_{CCBAT}. Stratix V devices will not exit POR if V_{CCBAT} stays at logic low.
- (3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.
- (4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

| Symbol | Description | Devices | Minimum ⁽⁴⁾ | Typical | Maximum ⁽⁴⁾ | Unit |
|-----------------------------------|---|------------|------------------------|---------|------------------------|------|
| V _{CCA_GXBL} (1), (3) | Transceiver channel PLL power supply (left side) | GX, GS, GT | 2.85 | 3.0 | 3.15 | V |
| | | | 2.375 | 2.5 | 2.625 | |
| V _{CCA_GXBR} (1), (3) | Transceiver channel PLL power supply (right side) | GX, GS | 2.85 | 3.0 | 3.15 | V |
| | | | 2.375 | 2.5 | 2.625 | |
| V _{CCA_GTBR} | Transceiver channel PLL power supply (right side) | GT | 2.85 | 3.0 | 3.15 | V |
| V _{CCHIP_L} | Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| V _{CCHIP_R} | Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| V _{CCHSSI_L} | Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| V _{CCHSSI_R} | Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| V _{CCR_GXBL} (2) | Receiver analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9. I/O Pin Leakage Current for Stratix V Devices ⁽¹⁾

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------|--------------------|--|-----|-----|-----|---------------|
| I_I | Input pin | $V_I = 0 \text{ V to } V_{CCIO\text{MAX}}$ | -30 | — | 30 | μA |
| I_{OZ} | Tri-stated I/O pin | $V_O = 0 \text{ V to } V_{CCIO\text{MAX}}$ | -30 | — | 30 | μA |

Note to Table 9:

(1) If $V_O = V_{CCIO}$ to $V_{CCIO\text{MAX}}$, 100 μA of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

| Parameter | Symbol | Conditions | V _{CCIO} | | | | | | | | | | Unit |
|-------------------------|-------------------|--|-------------------|------|-------|------|-------|------|-------|------|-------|------|------|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | I _{SUSL} | V _{IN} > V _{IL} (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | μA |
| High sustaining current | I _{SUSH} | V _{IN} < V _{IH} (minimum) | −22.5 | — | −25.0 | — | −30.0 | — | −50.0 | — | −70.0 | — | μA |
| Low overdrive current | I _{ODL} | 0V < V _{IN} < V _{CCIO} | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | μA |
| High overdrive current | I _{ODH} | 0V < V _{IN} < V _{CCIO} | — | −120 | — | −160 | — | −200 | — | −300 | — | −500 | μA |
| Bus-hold trip point | V _{TRIP} | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|--------------------|---|---|----------------------|----------|----------------|----------|------|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 25- Ω R_S | Internal series termination with calibration (25- Ω setting) | $V_{\text{CCIO}} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$ | ± 15 | ± 15 | ± 15 | ± 15 | % |

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 2 of 2)

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|--|--|---|----------------------|------------|----------------|------------|------|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 50-Ω R _S | Internal series termination with calibration (50-Ω setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 34-Ω and 40-Ω R _S | Internal series termination with calibration (34-Ω and 40-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting) | V _{CCIO} = 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 50-Ω R _T | Internal parallel termination with calibration (50-Ω setting) | V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T | Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 60-Ω and 120-Ω R _T | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | V _{CCIO} = 1.2 | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 25-Ω R _{S_left_shift} | Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|-----------------------------|--|-----------------------------------|----------------------|-------|-----------------|--------|------|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 25-Ω R, 50-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 3.0 and 2.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) ⁽¹⁾

| Symbol | Description | V _{CCIO} (V) | Typical | Unit |
|--------|--|-----------------------|---------|-------------------|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/ ^o C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

Note to Table 13:

(1) Valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C.

Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

Table 14. Pin Capacitance for Stratix V Devices

| Symbol | Description | Value | Unit |
|--------------------|--|-------|------|
| C _{IOTB} | Input capacitance on the top and bottom I/O pins | 6 | pF |
| C _{IOLR} | Input capacitance on the left and right I/O pins | 6 | pF |
| C _{OUTFB} | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

Table 15. Hot Socketing Specifications for Stratix V Devices

| Symbol | Description | Maximum |
|---------------------------|--|---------------------|
| I _{IOPIN} (DC) | DC current per I/O pin | 300 μ A |
| I _{IOPIN} (AC) | AC current per I/O pin | 8 mA ⁽¹⁾ |
| I _{XCVR-TX} (DC) | DC current per transceiver transmitter pin | 100 mA |
| I _{XCVR-RX} (DC) | DC current per transceiver receiver pin | 50 mA |

Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C \, dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices ^{(1), (2)}

| Symbol | Description | V _{CCIO} Conditions (V) ⁽³⁾ | Value ⁽⁴⁾ | Unit |
|-----------------|---|---|----------------------|------|
| R _{PU} | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5% | 25 | kΩ |
| | | 2.5 ±5% | 25 | kΩ |
| | | 1.8 ±5% | 25 | kΩ |
| | | 1.5 ±5% | 25 | kΩ |
| | | 1.35 ±5% | 25 | kΩ |
| | | 1.25 ±5% | 25 | kΩ |
| | | 1.2 ±5% | 25 | kΩ |

Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to “Glossary” on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

| I/O Standard | V _{CCIO} (V) | | | V _{IL} (V) | | V _{IH} (V) | | V _{OL} (V) | V _{OH} (V) | I _{OL} (mA) | I _{OH} (mA) |
|--------------|-----------------------|-----|-------|---------------------|-----------------------------|-----------------------------|-------------------------|-----------------------------|-----------------------------|----------------------|----------------------|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTTL | 2.85 | 3 | 3.15 | −0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | −2 |
| LVC MOS | 2.85 | 3 | 3.15 | −0.3 | 0.8 | 1.7 | 3.6 | 0.2 | V _{CCIO} − 0.2 | 0.1 | −0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | −0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | −1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | −0.3 | 0.35 * V _{CCIO} | 0.65 * V _{CCIO} | V _{CCIO} + 0.3 | 0.45 | V _{CCIO} − 0.45 | 2 | −2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | −0.3 | 0.35 * V _{CCIO} | 0.65 * V _{CCIO} | V _{CCIO} + 0.3 | 0.25 * V _{CCIO} | 0.75 * V _{CCIO} | 2 | −2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | −0.3 | 0.35 * V _{CCIO} | 0.65 * V _{CCIO} | V _{CCIO} + 0.3 | 0.25 * V _{CCIO} | 0.75 * V _{CCIO} | 2 | −2 |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 2 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|----------------------------------|-------------------|------|----------------------------------|-------------------|------|----------------------------------|-----------------------|------|-------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Spread-spectrum downspread | PCIe | — | 0 to -0.5 | — | — | 0 to -0.5 | — | — | 0 to -0.5 | — | % |
| On-chip termination resistors ⁽²¹⁾ | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Absolute V_{MAX} ⁽⁵⁾ | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | |
| Absolute V_{MIN} | — | -0.4 | — | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | 200 | — | 1600 | mV |
| V_{ICM} (AC coupled) ⁽³⁾ | Dedicated reference clock pin | 1050/1000/900/850 ⁽²⁾ | | | 1050/1000/900/850 ⁽²⁾ | | | 1050/1000/900/850 ⁽²⁾ | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 ⁽⁴⁾ | | | 1.0/0.9/0.85 ⁽⁴⁾ | | | 1.0/0.9/0.85 ⁽⁴⁾ | | | V |
| V_{ICM} (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise (622 MHz) ⁽²⁰⁾ | 100 Hz | — | — | -70 | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | — | — | -90 | dBc/Hz |
| | 10 kHz | — | — | -100 | — | — | -100 | — | — | -100 | dBc/Hz |
| | 100 kHz | — | — | -110 | — | — | -110 | — | — | -110 | dBc/Hz |
| | ≥ 1 MHz | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁷⁾ | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | — | — | 3 | ps (rms) |
| R_{REF} ⁽¹⁹⁾ | — | — | 1800 $\pm 1\%$ | — | — | 1800 $\pm 1\%$ | — | — | 180 0 $\pm 1\%$ | — | Ω |
| Transceiver Clocks | | | | | | | | | | | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | — | 100 or 125 | — | MHz |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 3 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|--|-----|-------|------------------------------|-----|-------|------------------------------|-----|-------------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reconfiguration clock (<code>mgmt_clk_clk</code>) frequency | — | 100 | — | 125 | 100 | — | 125 | 100 | — | 125 | MHz |
| Receiver | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Data rate (Standard PCS) ^{(9), (23)} | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| Data rate (10G PCS) ^{(9), (23)} | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| Absolute V_{MAX} for a receiver pin ⁽⁵⁾ | — | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V_{MIN} for a receiver pin | — | −0.4 | — | — | −0.4 | — | — | −0.4 | — | — | V |
| Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) before device configuration ⁽²²⁾ | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) after device configuration ^{(18), (22)} | $V_{CCR_GXB} = 1.0\text{ V}/1.05\text{ V}$ ($V_{ICM} = 0.70\text{ V}$) | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | V |
| | $V_{CCR_GXB} = 0.90\text{ V}$ ($V_{ICM} = 0.6\text{ V}$) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| | $V_{CCR_GXB} = 0.85\text{ V}$ ($V_{ICM} = 0.6\text{ V}$) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins ^{(6), (22), (27)} | — | 85 | — | — | 85 | — | — | 85 | — | — | mV |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to- channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| CMU PLL | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁶⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| ATX PLL | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 (24) | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁶⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| fPLL | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 ⁽²⁵⁾ | 600 | — | 3250/ 3125 ⁽²⁵⁾ | 600 | — | 3250/ 3125 ⁽²⁵⁾ | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications ⁽¹⁾

| Clock Network | ATX PLL | | | CMU PLL ⁽²⁾ | | | fPLL | | |
|--------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|
| | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span |
| x1 ⁽³⁾ | 14.1 | — | 6 | 12.5 | — | 6 | 3.125 | — | 3 |
| x6 ⁽³⁾ | — | 14.1 | 6 | — | 12.5 | 6 | — | 3.125 | 6 |
| x6 PLL Feedback ⁽⁴⁾ | — | 14.1 | Side-wide | — | 12.5 | Side-wide | — | — | — |
| xN (PCIe) | — | 8.0 | 8 | — | 5.0 | 8 | — | — | — |
| xN (Native PHY IP) | 8.0 | 8.0 | Up to 13 channels above and below PLL | 7.99 | 7.99 | Up to 13 channels above and below PLL | 3.125 | 3.125 | Up to 13 channels above and below PLL |
| | — | 8.01 to 9.8304 | Up to 7 channels above and below PLL | | | | | | |

Notes to Table 24:

- (1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.
- (2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
- (3) Channel span is within a transceiver bank.
- (4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 27 shows the V_{OD} settings for the GX channel.

Table 27. Typical V_{OD} Setting for GX Channel, TX Termination = 100 Ω ⁽²⁾

| Symbol | V_{OD} Setting | V_{OD} Value (mV) | V_{OD} Setting | V_{OD} Value (mV) |
|---|------------------|---------------------|------------------|---------------------|
| V_{OD} differential peak to peak typical ⁽³⁾ | 0 ⁽¹⁾ | 0 | 32 | 640 |
| | 1 ⁽¹⁾ | 20 | 33 | 660 |
| | 2 ⁽¹⁾ | 40 | 34 | 680 |
| | 3 ⁽¹⁾ | 60 | 35 | 700 |
| | 4 ⁽¹⁾ | 80 | 36 | 720 |
| | 5 ⁽¹⁾ | 100 | 37 | 740 |
| | 6 | 120 | 38 | 760 |
| | 7 | 140 | 39 | 780 |
| | 8 | 160 | 40 | 800 |
| | 9 | 180 | 41 | 820 |
| | 10 | 200 | 42 | 840 |
| | 11 | 220 | 43 | 860 |
| | 12 | 240 | 44 | 880 |
| | 13 | 260 | 45 | 900 |
| | 14 | 280 | 46 | 920 |
| | 15 | 300 | 47 | 940 |
| | 16 | 320 | 48 | 960 |
| | 17 | 340 | 49 | 980 |
| | 18 | 360 | 50 | 1000 |
| | 19 | 380 | 51 | 1020 |
| | 20 | 400 | 52 | 1040 |
| | 21 | 420 | 53 | 1060 |
| | 22 | 440 | 54 | 1080 |
| | 23 | 460 | 55 | 1100 |
| | 24 | 480 | 56 | 1120 |
| | 25 | 500 | 57 | 1140 |
| | 26 | 520 | 58 | 1160 |
| | 27 | 540 | 59 | 1180 |
| | 28 | 560 | 60 | 1200 |
| | 29 | 580 | 61 | 1220 |
| | 30 | 600 | 62 | 1240 |
| | 31 | 620 | 63 | 1260 |

Note to Table 27:

- (1) If TX termination resistance = 100 Ω , this VOD setting is illegal.
- (2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.
- (3) Refer to Figure 2.

Figure 2 shows the differential transmitter output waveform.

Figure 2. Differential Transmitter Output Waveform

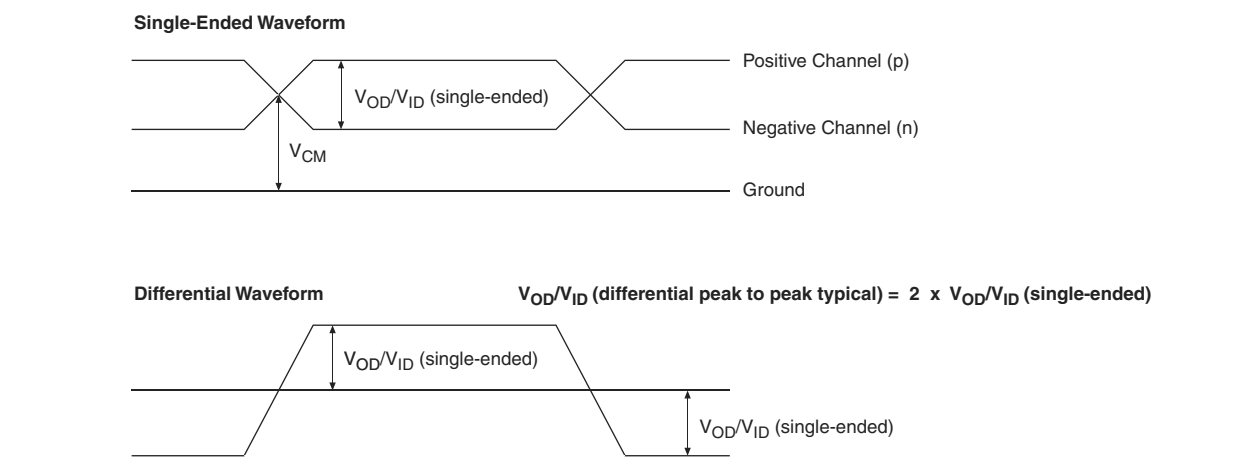


Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|--|---------------|--------|------------------------------|---------------|--------|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁸⁾ | 100 Hz | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | |
| | 10 kHz | — | — | -100 | — | — | -100 | |
| | 100 kHz | — | — | -110 | — | — | -110 | |
| | ≥ 1 MHz | — | — | -120 | — | — | -120 | |
| Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾ | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | ps (rms) |
| RREF ⁽¹⁷⁾ | — | — | 1800 ± 1% | — | — | 1800 ± 1% | — | Ω |
| Transceiver Clocks | | | | | | | | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | MHz |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | MHz |
| Receiver | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Data rate (Standard PCS) ⁽²¹⁾ | GX channels | 600 | — | 8500 | 600 | — | 8500 | Mbps |
| Data rate (10G PCS) ⁽²¹⁾ | GX channels | 600 | — | 12,500 | 600 | — | 12,500 | Mbps |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Absolute V _{MAX} for a receiver pin ⁽³⁾ | GT channels | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V _{MIN} for a receiver pin | GT channels | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾ | GT channels | — | — | 1.6 | — | — | 1.6 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration ⁽¹⁶⁾ , ⁽²⁰⁾ | GT channels V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V) | — | — | 2.2 | — | — | 2.2 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Minimum differential eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾ | GT channels | 200 | — | — | 200 | — | — | mV |
| | GX channels | ⁽⁸⁾ | | | | | | |

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|------------------------------|-----|--------------------------------|------------------------------|-----|--------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Differential on-chip termination resistors | GT channels | — | 100 | — | — | 100 | — | Ω |
| | GX channels | (8) | | | | | | |
| V _{OCM} (AC coupled) | GT channels | — | 500 | — | — | 500 | — | mV |
| | GX channels | (8) | | | | | | |
| Rise/Fall time | GT channels | — | 15 | — | — | 15 | — | ps |
| | GX channels | (8) | | | | | | |
| Intra-differential pair skew | GX channels | (8) | | | | | | |
| Intra-transceiver block transmitter channel-to- channel skew | GX channels | (8) | | | | | | |
| Inter-transceiver block transmitter channel-to- channel skew | GX channels | (8) | | | | | | |
| CMU PLL | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 8500 | Mbps |
| t _{pll_powerdown} ⁽¹³⁾ | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |
| ATX PLL | | | | | | | | |
| Supported Data Rate Range for GX Channels | VCO post- divider L=2 | 8000 | — | 12500 | 8000 | — | 8500 | Mbps |
| | L=4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| Supported Data Rate Range for GT Channels | VCO post- divider L=2 | 9800 | — | 14025 | 9800 | — | 12890 | Mbps |
| t _{pll_powerdown} ⁽¹³⁾ | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |
| fPLL | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3.125 ⁽²³⁾ | 600 | — | 3250/ 3.125 ⁽²³⁾ | Mbps |
| t _{pll_powerdown} ⁽¹³⁾ | — | 1 | — | — | 1 | — | — | μs |

PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------|--|-----|-----|--------------------|------|
| f_{IN} | Input clock frequency (C1, C2, C2L, I2, and I2L speed grades) | 5 | — | 800 ⁽¹⁾ | MHz |
| | Input clock frequency (C3, I3, I3L, and I3YY speed grades) | 5 | — | 800 ⁽¹⁾ | MHz |
| | Input clock frequency (C4, I4 speed grades) | 5 | — | 650 ⁽¹⁾ | MHz |
| f_{INPFD} | Input frequency to the PFD | 5 | — | 325 | MHz |
| f_{FINPFD} | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| f_{VCO} ⁽⁹⁾ | PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C3, I3, I3L, I3YY speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grades) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| f_{OUT} | Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades) | — | — | 717 ⁽²⁾ | MHz |
| | Output frequency for an internal global or regional clock (C3, I3, I3L speed grades) | — | — | 650 ⁽²⁾ | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grades) | — | — | 580 ⁽²⁾ | MHz |
| f_{OUT_EXT} | Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades) | — | — | 800 ⁽²⁾ | MHz |
| | Output frequency for an external clock output (C3, I3, I3L speed grades) | — | — | 667 ⁽²⁾ | MHz |
| | Output frequency for an external clock output (C4, I4 speed grades) | — | — | 553 ⁽²⁾ | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to 50%) | 45 | 50 | 55 | % |
| t_{FCOMP} | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic Configuration Clock used for <code>mgmt_clk</code> and <code>scanclk</code> | — | — | 100 | MHz |
| t_{LOCK} | Time required to lock from the end-of-device configuration or deassertion of <code>areset</code> | — | — | 1 | ms |
| t_{DLOCK} | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| f_{CLBW} | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth ⁽⁷⁾ | — | 4 | — | MHz |
| t_{PLL_PSERR} | Accuracy of PLL phase shift | — | — | ±50 | ps |
| t_{ARESET} | Minimum pulse width on the <code>areset</code> signal | 10 | — | — | ns |

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|------------|--|----------------|--------|-------------|---------|-----|-----|---------|---------------|-----|------|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| M20K Block | Single-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port with the read-during-write option set to Old Data , all supported widths | 0 | 1 | 525 | 525 | 455 | 400 | 525 | 455 | 400 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 0 | 1 | 450 | 450 | 400 | 350 | 450 | 400 | 350 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |
| | True dual port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | ROM, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |

Notes to Table 33:

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.
- (3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time | Resolution | Minimum Resolution with no Missing Codes |
|-------------------|----------|--------------------------|----------------|-----------------|------------|--|
| –40°C to 100°C | ±8°C | No | 1 MHz, 500 KHz | < 100 ms | 8 bits | 8 bits |

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

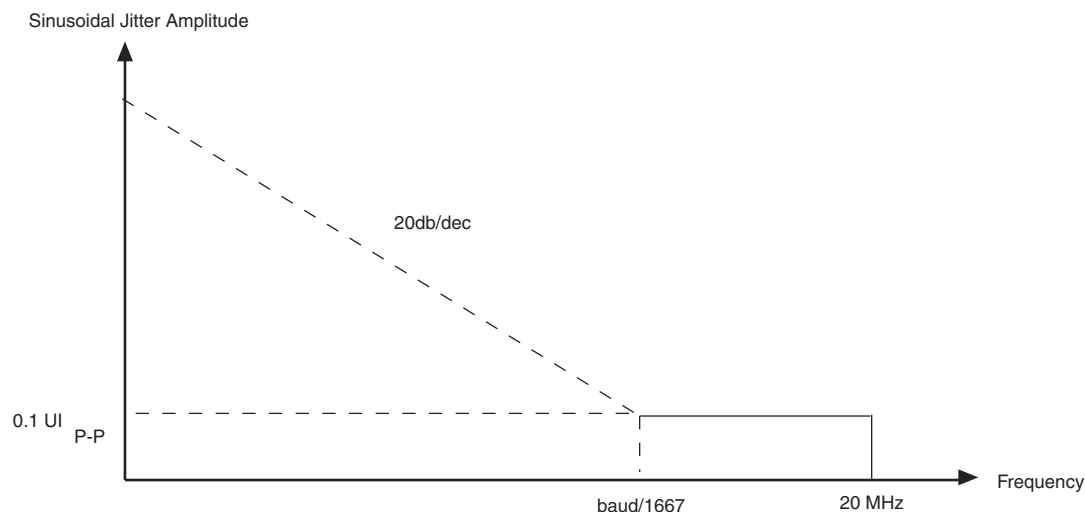
Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

| Description | Min | Typ | Max | Unit |
|--|-------|-------|-------|------|
| I _{bias} , diode source current | 8 | — | 200 | μA |
| V _{bias} , voltage across diode | 0.3 | — | 0.9 | V |
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|-----------------------|------------|------------------------|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps

DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices ⁽¹⁾

| C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|---------|------------------|-------------------|---------|------|
| 300-933 | 300-933 | 300-890 | 300-890 | MHz |

Note to Table 39:

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

| Speed Grade | Min | Max | Unit |
|------------------|-----|-----|------|
| C1 | 8 | 14 | ps |
| C2, C2L, I2, I2L | 8 | 14 | ps |
| C3,I3, I3L, I3YY | 8 | 15 | ps |

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices ⁽¹⁾

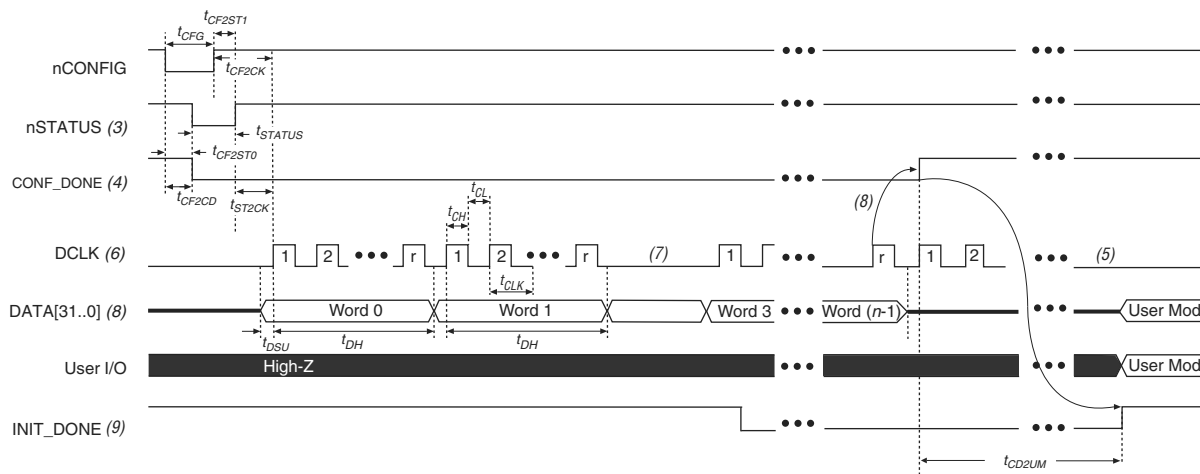
| Symbol | Parameter | Minimum | Maximum | Units |
|-----------------------------------|---|--|----------------------|-------|
| t _{CF2CD} | nCONFIG low to CONF_DONE low | — | 600 | ns |
| t _{CF2ST0} | nCONFIG low to nSTATUS low | — | 600 | ns |
| t _{CFG} | nCONFIG low pulse width | 2 | — | μs |
| t _{STATUS} | nSTATUS low pulse width | 268 | 1,506 ⁽²⁾ | μs |
| t _{CF2ST1} | nCONFIG high to nSTATUS high | — | 1,506 ⁽³⁾ | μs |
| t _{CF2CK} ⁽⁶⁾ | nCONFIG high to first rising edge on DCLK | 1,506 | — | μs |
| t _{ST2CK} ⁽⁶⁾ | nSTATUS high to first rising edge of DCLK | 2 | — | μs |
| t _{DSU} | DATA [] setup time before rising edge on DCLK | 5.5 | — | ns |
| t _{DH} | DATA [] hold time after rising edge on DCLK | 0 | — | ns |
| t _{CH} | DCLK high time | $0.45 \times 1/f_{\text{MAX}}$ | — | s |
| t _{CL} | DCLK low time | $0.45 \times 1/f_{\text{MAX}}$ | — | s |
| t _{CLK} | DCLK period | $1/f_{\text{MAX}}$ | — | s |
| f _{MAX} | DCLK frequency (FPP $\times 8/\times 16$) | — | 125 | MHz |
| | DCLK frequency (FPP $\times 32$) | — | 100 | MHz |
| t _{CD2UM} | CONF_DONE high to user mode ⁽⁴⁾ | 175 | 437 | μs |
| t _{CD2CU} | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| t _{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | t _{CD2CU} + (8576 × CLKUSR period) ⁽⁵⁾ | — | — |

Notes to Table 50:

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)**Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 60. Glossary (Part 4 of 4)

| Letter | Subject | Definitions |
|----------|---------------|--|
| V | $V_{CM(DC)}$ | DC common mode input voltage. |
| | V_{ICM} | Input common mode voltage—The common mode of the differential signal at the receiver. |
| | V_{ID} | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| | V_{IH} | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage |
| | $V_{IH(DC)}$ | High-level DC input voltage |
| | V_{IL} | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage |
| | $V_{IL(DC)}$ | Low-level DC input voltage |
| | V_{OCM} | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| | V_{OD} | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| | V_{SWING} | Differential input voltage |
| | V_X | Input differential cross point voltage |
| | V_{OX} | Output differential cross point voltage |
| W | W | High-speed I/O block—clock boost factor |
| X | | |
| Y | — | — |
| Z | | |