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Details

Product Status	Obsolete
Number of LABs/CLBs	262400
Number of Logic Elements/Cells	695000
Total RAM Bits	51200000
Number of I/O	840
Number of Gates	
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgsed8n3f45i3n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Minimum	Maximum	Unit
V _{CCD_FPLL}	PLL digital power supply	-0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	-0.5	3.4	V
VI	DC input voltage	-0.5	3.8	V
TJ	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (No bias)	-65	150	°C
I _{OUT}	DC output current per pin	-25	40	mA

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V _{CCA_GXBL}	Transceiver channel PLL power supply (left side)	GX, GS, GT	-0.5	3.75	V
V _{CCA_GXBR}	Transceiver channel PLL power supply (right side)	GX, GS	-0.5	3.75	V
V _{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	-0.5	3.75	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V _{CCT_GXBL}	Transmitter analog power supply (left side)	GX, GS, GT	-0.5	1.35	V
V _{CCT_GXBR}	Transmitter analog power supply (right side)	GX, GS, GT	-0.5	1.35	V
V _{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	-0.5	1.35	V
V _{CCL_GTBR}	Transmitter clock network power supply (right side)	GT	-0.5	1.35	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	-0.5	1.8	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	-0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min ⁽⁴⁾	Тур	Max ⁽⁴⁾	Unit
	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	_	0.87	0.9	0.93	V
V _{CC}	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾		0.82	0.85	0.88	V
V _{CCPT}	Power supply for programmable power technology	_	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology		2.375	2.5	2.625	V
VI (1)	I/O pre-driver (3.0 V) power supply	_	2.85	3.0	3.15	V
VCCPD	I/O pre-driver (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (3.0 V) power supply	_	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply		2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	_	1.71	1.8	1.89	V
V _{CCIO}	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply		1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	_	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	_	1.14	1.2	1.26	V
	Configuration pins (3.0 V) power supply		2.85	3.0	3.15	V
V _{CCPGM}	Configuration pins (2.5 V) power supply	_	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	-	1.71	1.8	1.89	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply		2.375	2.5	2.625	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	-	1.45	1.5	1.55	V
V _{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	_	1.2	_	3.0	V
VI	DC input voltage	_	-0.5	—	3.6	V
V ₀	Output voltage		0	_	V _{CCIO}	V
т	Operating junction temperature	Commercial	0	—	85	°C
IJ		Industrial	-40	_	100	°C

			Calibration Accura		n Accuracy		
Symbol	Description	Conditions	C1	C2,I2	C3,I3, I3YY	C4,14	Unit
50-Ω R _S	Internal series termination with calibration (50- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%
34- Ω and 40- Ω R _S	Internal series termination with calibration (34- Ω and 40- Ω setting)	V _{CCI0} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48- Ω , 60- Ω , 80- Ω , and 240- Ω setting)	V _{CCI0} = 1.2 V	±15	±15	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCI0} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R _T	Internal parallel termination with calibration ($20 - \Omega$, $30 - \Omega$, $40 - \Omega$, $60 - \Omega$, and $120 - \Omega$ setting)	V _{CCI0} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
60- $Ω$ and 120- $Ω$ R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCI0} = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%
$25-\Omega \\ R_{S_left_shift}$	Internal left shift series termination with calibration ($25-\Omega$ R _{S_left_shift} setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

Table II. OUI Valiblation Accuracy specifications for Stratix V Devices' / (Latt 2 OF	Table 11.	OCT Calibration A	ccuracy Specificati	ons for Stratix V D	Devices ⁽¹⁾ (Part 2 of
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Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance to PVT changes.

Table 12.	OCT Without Calibration	Resistance 1	Tolerance	Specifications	for Stratix	V Devices	(Part 1	of 2)
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			Resistance Tolerance				
Symbol	Description Conditions		C1	C2,I2	C3, I3, I3YY	C4, I4	Unit
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25-Ω setting)	$V_{CCIO} = 3.0$ and 2.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCI0} = 1.8 and 1.5 V	±30	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCI0} = 1.2 V	±35	±35	±50	±50	%

			Re	esistance	Tolerance		
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	$V_{CCIO} = 1.8$ and 1.5 V	±30	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCI0} = 1.2 V	±35	±35	±50	±50	%
100-Ω R _D	Internal differential termination (100- Ω setting)	V _{CCPD} = 2.5 V	±25	±25	±25	±25	%

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration for Stratix V Devices (1), (2), (3), (4), (5), (6)

$$R_{OCT} \,=\, R_{SCAL} \Big(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle \Big) \label{eq:ROCT}$$

Notes to Equation 1:

- (1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO} .
- (2) R_{SCAL} is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power-up.
- (4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
- (5) dR/dT is the percentage change of R_{SCAL} with temperature.
- (6) dR/dV is the percentage change of $\mathsf{R}_{\mathsf{SCAL}}$ with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2)
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Symbol	Description	V _{CCIO} (V)	Typical	Unit
		3.0	0.0297	
		2.5	0.0344	
dR/dV	dR/dV OCT variation with voltage without recalibration	1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Symbol	Description	V _{CCIO} Conditions (V) ⁽³⁾	Value ⁽⁴⁾	Unit
		3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
R _{PU}	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ
	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ
	pull-up resistor option.	1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a $\pm 10\%$ tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

I/O		V _{ccio} (V)		VII	∟ (V)	VIH	(V)	V _{OL} (V)	V _{OH} (V)	I _{OL}	I _{oh}
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCI0} + 0.3	0.45	V _{CCI0} – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V _{CCI0}	0.65 * V _{CCI0}	V _{CCI0} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard –	V _{IL(DI}	_{c)} (V)	V _{IH(D}	_{C)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{ol} (V)	V _{oh} (V)	I (mA)	l _{oh}
i/U Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	1 ₀₁ (11174)	(mA)
HSTL-18 Class I	—	V _{REF} – 0.1	V _{REF} + 0.1	_	$V_{REF} - 0.2$	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	8	-8
HSTL-18 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	8	-8
HSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	16	-16
HSUL-12	—	V _{REF} - 0.13	V _{REF} + 0.13	_	V _{REF} – 0.22	V _{REF} + 0.22	0.1* V _{CCIO}	0.9* V _{CCI0}	_	

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard		V _{ccio} (V)		V _{SWIN}	_{G(DC)} (V)	V _{X(AC)} (V)			V _{SWING(}	V _{SWING(AC)} (V)	
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCI0} + 0.6	V _{CCI0} /2- 0.2	_	V _{CCI0} /2 + 0.2	0.62	V _{CCI0} + 0.6	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCI0} /2- 0.175	_	V _{CCI0} /2 + 0.175	0.5	V _{CCI0} + 0.6	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V _{CCI0} /2- 0.15	_	V _{CCI0} /2 + 0.15	0.35	_	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V _{CCI0} /2- 0.15	V _{CCI0} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V _{CCI0} /2- 0.15	V _{CCI0} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V _{REF} 0.15	V _{CCI0} /2	V _{REF} + 0.15	-0.30	0.30	

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits $(V_{IH(DC)} \text{ and } V_{IL(DC)})$.

I/O	V _{CCIO} (V)			V _{DIF(}	V _{DIF(DC)} (V) V _{X(AC)} (V) V _{CM(DC)} (V)				V _{DIF(/}	_{AC)} (V)			
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	r Speed Transceiver Speed 2 Grade 3				
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
	DC Gain Setting = 0		0	_	_	0	_	_	0	—	dB	
	DC Gain Setting = 1	_	2		_	2	_	_	2	_	dB	
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB	
	DC Gain Setting = 3	_	6	_	_	6	_	_	6	_	dB	
	DC Gain Setting = 4		8			8	_		8	_	dB	
Transmitter												
Supported I/O Standards	_				-	1.4-V ar	nd 1.5-V PC	ML				
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps	
Data rate (10G PCS)	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps	
	85-Ω setting	_	85 ± 20%	_	_	85 ± 20%	_	_	85 ± 20%	—	Ω	
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω	
chip termination resistors	120-Ω setting		120 ± 20%	_		120 ± 20%	_		120 ± 20%	_	Ω	
	150-Ω setting	_	150 ± 20%			150 ± 20%	_		150 ± 20%	_	Ω	
V _{OCM} (AC coupled)	0.65-V setting	_	650		_	650	_	_	650	—	mV	
V _{OCM} (DC coupled)	_	_	650	_	_	650		_	650	_	mV	
Rise time ⁽⁷⁾	20% to 80%	30	—	160	30	—	160	30	—	160	ps	
Fall time ⁽⁷⁾	80% to 20%	30		160	30		160	30	—	160	ps	
Intra-differential pair skew	Tx V _{CM} = 0.5 V and slew rate of 15 ps	_	_	15			15		_	15	ps	
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	_	_	120	_	_	120	_		120	ps	

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 5 of 7)

	Table 28.	Transceiver S	pecifications	for Stratix V	GT Devices	(Part 4 of 5) (1)
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Symbol/	Conditions	s	Transceive peed Grade	r 2	ר Sp	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Data rate	GT channels	19,600	_	28,050	19,600		25,780	Mbps
Differential on-chip	GT channels	_	100	—		100	_	Ω
termination resistors	GX channels				(8)			
	GT channels	_	500	_		500	_	mV
V _{OCM} (AC Coupled)	GX channels		•	•	(8)		•	
Dice/Fell time	GT channels	_	15	—	—	15	—	ps
Rise/Fail lime	GX channels				(8)			
Intra-differential pair skew	GX channels				(8)			
Intra-transceiver block transmitter channel-to- channel skew	GX channels				(8)			
Inter-transceiver block transmitter channel-to- channel skew	GX channels				(8)			
CMU PLL								
Supported Data Range	—	600		12500	600		8500	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	_	—	μs
t _{pll_lock} ⁽¹⁴⁾	—	_	—	10	_	_	10	μs
ATX PLL								
	VCO post- divider L=2	8000	_	12500	8000	_	8500	Mbps
	L=4	4000	—	6600	4000	_	6600	Mbps
Supported Data Rate	L=8	2000	—	3300	2000	_	3300	Mbps
Range for GX Channels	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	_	14025	9800	_	12890	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	_	—	μs
t _{pll_lock} ⁽¹⁴⁾	—	_	—	10	_	_	10	μs
fPLL								
Supported Data Range		600		3250/ 3.125 ⁽²³⁾	600		3250/ 3.125 ⁽²³⁾	Mbps
t _{pll_powerdown} ⁽¹³⁾	—	1	—	—	1	—	—	μs

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

		Resour	ces Used			Pe	erforman	ce			
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	525	525	455	400	525	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50**% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

(3) The F_{MAX} specification is only achievable with Fitter options, MLAB Implementation In 16-Bit Deep Mode enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35.	External	Temperature	Sensing D	iode Speci	fications f	for Stratix V	Devices
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Description	Min	Тур	Max	Unit
I _{bias} , diode source current	8	—	200	μA
V _{bias,} voltage across diode	0.3	—	0.9	V
Series resistance	—	_	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	_

Symbol	Conditiono		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I 3YY		C4,14	4	Ilait
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Transmitter														
	SERDES factor J = 3 to 10 ⁽⁹⁾ , ⁽¹¹⁾ , ⁽¹²⁾ , ⁽¹³⁾ , ⁽¹⁴⁾ , ⁽¹⁵⁾ , ⁽¹⁶⁾	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)		1050	Mbps
True Differential I/O Standards	SERDES factor J ≥ 4 LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
- f _{HSDR} (data rate)	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾	SERDES factor J = 4 to 10 (17)	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t _{x Jitter} - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160		_	160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps		_	0.1		_	0.1	_	_	0.1	_	_	0.1	UI
t _{x Jitter} - Emulated Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_		300	_	_	300	_		325	ps
External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 4)

	Conditiono		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I 3YY		C4,I	4	
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t _{duty}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
	True Differential I/O Standards	_	_	160	_	_	160	_	_	200	_	_	200	ps
t _{rise} & t _{fall}	Emulated Differential I/O Standards with three external output resistor networks			250			250			250			300	ps
	True Differential I/O Standards	_	_	150	_	_	150	_	_	150	_	_	150	ps
TCCS	Emulated Differential I/O Standards			300			300	_		300			300	ps
Receiver														
	SERDES factor J = 3 to 10 (11), (12), (13), (14), (15), (16)	150		1434	150	_	1434	150	_	1250	150	_	1050	Mbps
True Differential I/O Standards - f _{HSDRDPA} (data rate)	SERDES factor J ≥ 4 LVDS RX with DPA (12), (14), (15), (16)	150	_	1600	150	_	1600	150	_	1600	150	_	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 3 of 4)

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices ⁽¹⁾

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is ± 78 ps or ± 39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	^{),} (Part 1 of 2) ^{(2), (3)}
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Clock	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit	
NELWURK		-	Min	Max	Min	Max	Min	Max	Min	Max		
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps	
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps	
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps	
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps	
Global	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-150	150	-150	150	-165	165	-165	165	ps	
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-75	75	-90	90	-90	90	ps	

	Member Code		Active Serial ⁽¹⁾)	Fast Passive Parallel ⁽²⁾			
Variant		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)	
	D3	4	100	0.344	32	100	0.043	
	D4	4	100	0.534	32	100	0.067	
GS	D4	4	100	0.344	32	100	0.043	
	D5	4	100	0.534	32	100	0.067	
	D6	4	100	0.741	32	100	0.093	
	D8	4	100	0.741	32	100	0.093	
F	E9	4	100	0.857	32	100	0.107	
Ľ	EB	4	100	0.857	32	100	0.107	

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[]ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[]ratio for each combination.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	1
177 ×0	Enabled	Disabled	2
	Enabled	Enabled	2
	Disabled	Disabled	1
FPP ×16	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

 Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 1 of 2)



Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)

Notes to Figure 13:

- (1) Use this timing waveform and parameters when the DCLK-to-DATA [] ratio is >1. To find out the DCLK-to-DATA [] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA [] ratio. For the DCLK-to-DATA [] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA [31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Fable 52.	DCLK Frequency	Specification in th	e AS Configuration	Scheme ^{(1),}	(2)
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Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.





Notes to Figure 14:

- (1) If you are using AS $\times 4$ mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS $\times 1$ and AS $\times 4$ configurations in Stratix V devices.

Table JS. As fining falancees for as $\times 1$ and as $\times 4$ configurations in straits V devices $(2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3,$	Table 53.	AS Timing	Parameters for AS	\times 1 and AS \times 4 Confi	gurations in Stratix V	/ Devices ^{(1), (2)}	(Part 1 of 2)
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Symbol	Parameter	Minimum	Maximum	Units
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5	_	ns
t _H	Data hold time after falling edge on DCLK	0	_	ns

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions		
	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown: Bit Time 0.5 x TCCS RSKM Sampling Window RSKM 0.5 x TCCS RSKM		
S	Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: <i>Single-Ended Voltage Referenced I/O Standard</i> 		
	t _C	High-speed receiver and transmitter input and output clock period.		
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under SW in this table).		
	t _{duty}	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.		
т		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and the data sampling window.		
		(TUI = 1/(receiver input clock frequency multiplication factor) = t_c/w)		
	t _{FALL}	Signal high-to-low transition time (80-20%)		
	t _{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.		
	t _{outpj_i0}	Period jitter on the general purpose I/O driven by a PLL.		
	t _{outpj_dc}	Period jitter on the dedicated clock output driven by a PLL.		
	t _{RISE}	Signal low-to-high transition time (20-80%)		
U	—	_		

Letter	Subject	Definitions	
	V _{CM(DC)}	DC common mode input voltage.	
	V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.	
	V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.	
	V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.	
	V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.	
	V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.	
	V _{IH(AC)}	High-level AC input voltage	
	V _{IH(DC)}	High-level DC input voltage	
V	V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.	
	V _{IL(AC)}	Low-level AC input voltage	
	V _{IL(DC)}	Low-level DC input voltage	
	V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.	
	V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.	
	V _{SWING}	Differential input voltage	
	V _X	Input differential cross point voltage	
	V _{OX}	Output differential cross point voltage	
W	W	High-speed I/O block—clock boost factor	
X			
Y	—	—	
Z			

Table 60. Glossary (Part 4 of 4)

Document Revision History

Table 61 lists the revision history for this chapter.

 Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes	
June 2018	3.9	 Added the "Stratix V Device Overshoot Duration" figure. 	
April 2017		Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
	3.8	 Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Stratix V Devices" table. 	
		 Changed the condition for 100-Ω R_D in the "OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices" table. 	
		 Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table 	
		 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1" table. 	
		 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1" table. 	
		 Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency" table. 	
June 2016	3.7	 Added the V_{ID} minimum specification for LVPECL in the "Differential I/O Standard Specifications for Stratix V Devices" table 	
		 Added the I_{OUT} specification to the "Absolute Maximum Ratings for Stratix V Devices" table. 	
December 2015	3.6	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.	
December 2015	3.5	 Changed the transmitter, receiver, and ATX PLL data rate specifications in the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	
		 Changed the configuration .rbf sizes in the "Uncompressed .rbf Sizes for Stratix V Devices" table. 	
	3.4	• Changed the data rate specification for transceiver speed grade 3 in the following tables:	
		 "Transceiver Specifications for Stratix V GX and GS Devices" 	
		 "Stratix V Standard PCS Approximate Maximum Date Rate" 	
		 "Stratix V 10G PCS Approximate Maximum Data Rate" 	
July 2015		 Changed the conditions for reference clock rise and fall time, and added a note to the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	
		 Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	
		 Changed the t_{c0} maximum value in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table. 	
		 Removed the CDR ppm tolerance specification from the "Transceiver Specifications for Stratix V GX and GS Devices" table. 	