Intel - 5SGSMD3E3H29I3N Datasheet





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Details

Product Status	Obsolete
Number of LABs/CLBs	89000
Number of Logic Elements/Cells	236000
Total RAM Bits	13312000
Number of I/O	360
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-HBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgsmd3e3h29i3n

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			Resistance Tolerance					
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit	
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	$V_{CCIO} = 1.8$ and 1.5 V	±30	±30	±40	±40	%	
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCI0} = 1.2 V	±35	±35	±50	±50	%	
100-Ω R _D	Internal differential termination (100- Ω setting)	V _{CCPD} = 2.5 V	±25	±25	±25	±25	%	

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration for Stratix V Devices (1), (2), (3), (4), (5), (6)

$$R_{OCT} \,=\, R_{SCAL} \Big(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle \Big) \label{eq:ROCT}$$

Notes to Equation 1:

- (1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO} .
- (2) R_{SCAL} is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power-up.
- (4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
- (5) dR/dT is the percentage change of R_{SCAL} with temperature.
- (6) dR/dV is the percentage change of $\mathsf{R}_{\mathsf{SCAL}}$ with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2)
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Symbol	Description	V _{CCIO} (V)	Typical	Unit
		3.0	0.0297	
dR/dV		2.5	0.0344	
	OCT variation with voltage without recalibration	1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	

I/O Standard	V _{IL(DI}	_{c)} (V)	V _{IH(D}	_{C)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{ol} (V)	V _{oh} (V)	I (mA)	l _{oh}
i/U Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	1 ₀₁ (11174)	(mA)
HSTL-18 Class I	—	V _{REF} – 0.1	V _{REF} + 0.1	_	$V_{REF} - 0.2$	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	8	-8
HSTL-18 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	8	-8
HSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCI0} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	0.25* V _{CCI0}	0.75* V _{CCI0}	16	-16
HSUL-12	—	V _{REF} - 0.13	V _{REF} + 0.13	_	V _{REF} – 0.22	V _{REF} + 0.22	0.1* V _{CCIO}	0.9* V _{CCI0}	_	

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard	V _{CCIO} (V)			V _{SWING(DC)} (V)		V _{X(AC)} (V)			V _{SWING(AC)} (V)	
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCI0} + 0.6	V _{CCI0} /2- 0.2	_	V _{CCI0} /2 + 0.2	0.62	V _{CCI0} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCI0} /2- 0.175	_	V _{CCI0} /2 + 0.175	0.5	V _{CCI0} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V _{CCI0} /2- 0.15	_	V _{CCI0} /2 + 0.15	0.35	_
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V _{CCI0} /2- 0.15	V _{CCI0} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V _{CCI0} /2- 0.15	V _{CCI0} /2	V _{CCI0} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V _{REF} 0.15	V _{CCI0} /2	V _{REF} + 0.15	-0.30	0.30

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits $(V_{IH(DC)} \text{ and } V_{IL(DC)})$.

I/O	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)				V _{CM(DC)} (V	V _{DIF(AC)} (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	Transceiver Speed Grade 2			Transceiver Speed Grade 3			
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
	DC Gain Setting = 0		0	_	_	0	_	_	0	—	dB	
	DC Gain Setting = 1	_	2		_	2	_	_	2	_	dB	
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB	
	DC Gain Setting = 3	_	6	_	_	6	_	_	6	_	dB	
	DC Gain Setting = 4		8			8	_		8	_	dB	
Transmitter												
Supported I/O Standards	_				-	1.4-V ar	nd 1.5-V PC	ML				
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps	
Data rate (10G PCS)	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps	
	85-Ω setting	_	85 ± 20%	_	_	85 ± 20%	_	_	85 ± 20%	—	Ω	
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω	
chip termination resistors	120-Ω setting		120 ± 20%	_		120 ± 20%	_		120 ± 20%	_	Ω	
	150-Ω setting	_	150 ± 20%			150 ± 20%	_		150 ± 20%	_	Ω	
V _{OCM} (AC coupled)	0.65-V setting	_	650		_	650	_	_	650	—	mV	
V _{OCM} (DC coupled)	_	_	650	_	_	650		_	650	_	mV	
Rise time ⁽⁷⁾	20% to 80%	30	—	160	30	—	160	30	—	160	ps	
Fall time ⁽⁷⁾	80% to 20%	30		160	30		160	30	—	160	ps	
Intra-differential pair skew	Tx V _{CM} = 0.5 V and slew rate of 15 ps	_	_	15			15		_	15	ps	
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	_	_	120	_	_	120	_		120	ps	

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 5 of 7)

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trar	isceive Grade	r Speed 2	Tran	isceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	_	_	500	_	_	500	_	_	500	ps
CMU PLL	•									•	
Supported Data Range	_	600	_	12500	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	—	1			1			1			μs
t _{pll_lock} ⁽¹⁶⁾		—		10	—	_	10	—	_	10	μs
ATX PLL											
	VCO post-divider L=2	8000	_	14100	8000	_	12500	8000	_	8500/ 10312.5 (24)	Mbps
Supported Data	L=4	4000	_	7050	4000	_	6600	4000	—	6600	Mbps
Rate Range	L=8	2000		3525	2000		3300	2000		3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	1000	_	1762.5	Mbps
t _{pll_powerdown} (15)	—	1	_	—	1	_	—	1	_	—	μs
t _{pll_lock} (16)	—		—	10		—	10	—		10	μs
fPLL	•									•	
Supported Data Range	_	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	600	_	3250/ 3125 ⁽²⁵⁾	Mbps
t _{pll_powerdown} ⁽¹⁵⁾	_	1	—		1	—		1			μs

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

		ATX PLL			CMU PLL ⁽²⁾)	fPLL			
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	
x1 ⁽³⁾	14.1	_	6	12.5	_	6	3.125	—	3	
x6 ⁽³⁾	_	14.1	6	—	12.5	6	—	3.125	6	
x6 PLL Feedback ⁽⁴⁾	_	14.1	Side- wide	_	12.5	Side- wide	_	_	_	
xN (PCIe)	_	8.0	8	—	5.0	8	—	—	—	
xN (PCIE) xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7 00	7 00	Up to 13 channels above	3 125	3 125	Up to 13 channels above	
	_	8.01 to 9.8304	Up to 7 channels above and below PLL	7.99	7.99	and below PLL	0.120	0.120	and below PLL	

Notes to Table 24:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Symbol/	Conditions	s	Transceive peed Grade	r 2	S	Transceive peed Grade	r 3	Unit				
Description		Min	Тур	Max	Min	Тур	Max					
Reference Clock								1				
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	IL, 1.4-V PC	ML, 1.5-V P(CML, 2.5-V I and HCSL	PCML, Diffe	rential LVPE	ECL, LVDS,				
otanuarus	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾	_	40	_	710	40	_	710	MHz				
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	_	100	_	710	100	_	710	MHz				
Rise time	20% to 80%	_		400	_	_	400					
Fall time	80% to 20%			400	—	_	400	ps				
Duty cycle	—	45	_	55	45	_	55	%				
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz				
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%				
On-chip termination resistors ⁽¹⁹⁾	_	_	100	_	_	100	_	Ω				
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V				
	RX reference clock pin	_	_	1.2	_	_	1.2					
Absolute V _{MIN}	—	-0.4		—	-0.4	—		V				
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV				
V _{ICM} (AC coupled)	Dedicated reference clock pin		1050/1000 ^{(,}	2)	1	050/1000 (2)	mV				
	RX reference clock pin	1	.0/0.9/0.85 (22)	1.	0/0.9/0.85 ((22)	V				
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250		550	mV				

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)⁽¹⁾

Symbol/	Conditions	S	Transceive peed Grade	2	S	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Differential on-chip termination resistors ⁽⁷⁾	GT channels		100	_	_	100	_	Ω
	85- Ω setting	_	85 ± 30%	_	_	85 ± 30%	_	Ω
Differential on-chip	100-Ω setting	_	100 ± 30%	_	_	100 ± 30%	_	Ω
for GX channels ⁽¹⁹⁾	120-Ω setting	_	120 ± 30%	_	—	120 ± 30%	—	Ω
	150-Ω setting	_	150 ± 30%	_	_	150 ± 30%	_	Ω
V _{ICM} (AC coupled)	GT channels	_	650	_	—	650	—	mV
	VCCR_GXB = 0.85 V or 0.9 V	_	600	_	_	600	_	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 1.0 V full bandwidth	_	700		_	700	_	mV
	VCCR_GXB = 1.0 V half bandwidth	_	750	_	_	750	_	mV
t _{LTR} ⁽⁹⁾	—	_	—	10	—	—	10	μs
t _{LTD} ⁽¹⁰⁾		4			4	_	_	μs
t _{LTD_manual} ⁽¹¹⁾		4	_		4	_	_	μs
t _{LTR_LTD_manual} ⁽¹²⁾	—	15	—	_	15	—	—	μs
Run Lenath	GT channels		—	72	—	—	72	CID
	GX channels				(8)			
CDR PPM	GT channels	_	—	1000	—	—	1000	± PPM
	GX channels				(8)			
Programmable	GT channels	_		14		_	14	dB
(AC Gain) ⁽⁵⁾	GX channels				(8)			
Programmable	GT channels	_		7.5	_	_	7.5	dB
DC gain ⁽⁶⁾	GX channels				(8)			
Differential on-chip termination resistors ⁽⁷⁾	GT channels	_	100	—	_	100	_	Ω
Transmitter								
Supported I/O Standards	_	1.4-V and 1.5-V PCML						
Data rate (Standard PCS)	GX channels	600	_	8500	600		8500	Mbps
Data rate (10G PCS)	GX channels	600		12,500	600		12,500	Mbps

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5)⁽¹⁾

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

	Performance							
Symbol	Symbol C1, C2, C2L, I2, and I2L		C4, I4	Unit				
Global and Regional Clock	717	650	580	MHz				
Periphery Clock	550	500	500	MHz				

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
Modes using Three DSPs								
One complex 18 x 25	425	425	415	340	340	275	265	MHz
Modes using Four DSPs								
One complex 27 x 27	465	465	465	380	380	300	290	MHz

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

		Resources Used		Performance							
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
WILAD	Simple dual-port, x16 depth ⁽³⁾	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices ⁽¹⁾

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is ± 78 ps or ± 39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	^{),} (Part 1 of 2) ^{(2), (3)}
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Clock	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit
NELWURK			Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	t _{JIT(duty)}	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	t _{JIT(cc)}	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{\text{JIT}(\text{duty})}$	-75	75	-75	75	-90	90	-90	90	ps

Clock	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit
NELWURK			Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	_	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn_term_ctrl signals.

Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C1		C2, C2	C2, C2L, I2, I2L		C3, I3, I3L, I3YY		4,14	Unit	
	Min	Max	Min	Max	Min	Max	Min	Max		
Output Duty Cycle	45	55	45	55	45	55	45	55	%	

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum		
Fast	4 ms	12 ms		
Standard	100 ms	300 ms		

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period ⁽²⁾	30		ns
t _{JCP}	TCK clock period ⁽²⁾	167	—	ns
t _{JCH}	TCK clock high time ⁽²⁾	14	—	ns
t _{JCL}	TCK clock low time ⁽²⁾	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	_	ns

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
Stratix V E ⁽¹⁾	5SEE9	—	342,742,976	700,888
	5SEEB	—	342,742,976	700,888

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Notes to Table 47:

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.

(2) 36-transceiver devices.

(3) 24-transceiver devices.

(4) File size for the periphery image.

(5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.ttf) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

• For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices.* For creating configuration files, refer to the *Quartus II Help.*

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devi
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Variant	Marchar	Active Serial ⁽¹⁾			Fast Passive Parallel ⁽²⁾		
	Code	Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
	٨٥	4	100	0.534	32	100	0.067
	AJ	4	100	0.344	32	100	0.043
	A4	4	100	0.534	32	100	0.067
	A5	4	100	0.675	32	100	0.084
	A7	4	100	0.675	32	100	0.084
GX	A9	4	100	0.857	32	100	0.107
	AB	4	100	0.857	32	100	0.107
	B5	4	100	0.676	32	100	0.085
	B6	4	100	0.676	32	100	0.085
	B9	4	100	0.857	32	100	0.107
	BB	4	100	0.857	32	100	0.107
ст	C5	4	100	0.675	32	100	0.084
GI	C7	4	100	0.675	32	100	0.084

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
FPP ×32	Disabled	Enabled	4
	Enabled	Disabled	8
	Enabled	Enabled	8

Table 49.	DCLK-to-DATA[]	Ratio ⁽¹⁾	(Part 2 of 2)
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Note to Table 49:

(1) Depending on the DCLK-to-DATA [] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA [] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

Figure 11. Single Device FPP Configuration Using an External Host



Notes to Figure 11:

- (1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device. V_{CCPGM} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with V_{CCPGM} .
- (2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.
- (3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (4) If you use FPP ×8, use DATA [7..0]. If you use FPP ×16, use DATA [15..0].

IF the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.





Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nstatus low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP ×16, use DATA [15..0]. For FPP ×8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT DONE goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μS
t _{status}	nSTATUS low pulse width	268	1,506 ⁽¹⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μS
t _{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t _{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2	—	μS
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t _{CL}	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f _{MAX}	DCLK frequency	—	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t _{cd2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) ⁽⁴⁾	_	_

Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	Clock Source	e Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles ⁽¹⁾
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP ⁽²⁾	125 MHz	8576
DCLK	PS, FPP	125 MHz	

Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

Table 60. Glossary (Part 2 of 4)

Letter	Subject	Definitions
G H I	JTAG Timing Specifications	High-speed I/O block—Deserialization factor (width of parallel data bus). JTAG Timing Specifications: TMS
K L M N O		
Ρ	PLL Specifications	Diagram of PLL Specifications ⁽¹⁾
Q	—	—
R	RL	Receiver differential input discrete resistor (external to the Stratix V device).

Document Revision History

Table 61 lists the revision history for this chapter.

 Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes			
June 2018	3.9	 Added the "Stratix V Device Overshoot Duration" figure. 			
		Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.			
		 Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Stratix V Devices" table. 			
		 Changed the condition for 100-Ω R_D in the "OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices" table. 			
April 2017	3.8	 Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table 			
		 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1" table. 			
		 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1" table. 			
		 Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency" table. 			
June 2016	3.7	 Added the V_{ID} minimum specification for LVPECL in the "Differential I/O Standard Specifications for Stratix V Devices" table 			
		 Added the I_{OUT} specification to the "Absolute Maximum Ratings for Stratix V Devices" table. 			
December 2015	3.6	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.			
December 2015	3.5	 Changed the transmitter, receiver, and ATX PLL data rate specifications in the "Transceiver Specifications for Stratix V GX and GS Devices" table. 			
December 2015		 Changed the configuration .rbf sizes in the "Uncompressed .rbf Sizes for Stratix V Devices" table. 			
		• Changed the data rate specification for transceiver speed grade 3 in the following tables:			
		 "Transceiver Specifications for Stratix V GX and GS Devices" 			
		 "Stratix V Standard PCS Approximate Maximum Date Rate" 			
		 "Stratix V 10G PCS Approximate Maximum Data Rate" 			
July 2015	3.4	 Changed the conditions for reference clock rise and fall time, and added a note to the "Transceiver Specifications for Stratix V GX and GS Devices" table. 			
		 Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Transceiver Specifications for Stratix V GX and GS Devices" table. 			
		 Changed the t_{c0} maximum value in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table. 			
		 Removed the CDR ppm tolerance specification from the "Transceiver Specifications for Stratix V GX and GS Devices" table. 			

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes		
		 Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. 		
		 Added the I3YY speed grade to the V_{CC} description in Table 6. 		
		 Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. 		
		■ Added 240-Ω to Table 11.		
		Changed CDR PPM tolerance in Table 23.		
		 Added additional max data rate for fPLL in Table 23. 		
		 Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. 		
		 Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. 		
		 Changed CDR PPM tolerance in Table 28. 		
		 Added additional max data rate for fPLL in Table 28. 		
		 Changed the mode descriptions for MLAB and M20K in Table 33. 		
		 Changed the Max value of f_{HSCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. 		
November 2014	3.3	 Changed the frequency ranges for C1 and C2 in Table 39. 		
		 Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47. 		
		 Added note about nSTATUS to Table 50, Table 51, Table 54. 		
		 Changed the available settings in Table 58. 		
		 Changed the note in "Periphery Performance". 		
		 Updated the "I/O Standard Specifications" section. 		
		 Updated the "Raw Binary File Size" section. 		
		 Updated the receiver voltage input range in Table 22. 		
		 Updated the max frequency for the LVDS clock network in Table 36. 		
		■ Updated the DCLK note to Figure 11.		
		 Updated Table 23 VO_{CM} (DC Coupled) condition. 		
		Updated Table 6 and Table 7.		
		 Added the DCLK specification to Table 55. 		
		Updated the notes for Table 47.		
		 Updated the list of parameters for Table 56. 		
November 2013	3.2	Updated Table 28		
November 2013	3.1	Updated Table 33		
November 2013	3.0	Updated Table 23 and Table 28		
October 2013	2.9	 Updated the "Transceiver Characterization" section 		
		 Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 		
Uctober 2013	2.8	 Added Figure 1 and Figure 3 		
		 Added the "Transceiver Characterization" section 		
		 Removed all "Preliminary" designations. 		