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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 89000 |
| Number of Logic Elements/Cells | 236000 |
| Total RAM Bits | 13312000 |
| Number of I/O | 360 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 780-BBGA, FCBGA |
| Supplier Device Package | 780-HBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgsmd3e3h29i4n |

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)**

| Symbol | Description | Condition | Min (4) | Typ | Max (4) | Unit |
|---|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
| | | Fast POR | 200 µs | — | 4 ms | — |

**Notes to Table 6:**

(1) $V_{CCPD}$ must be 2.5 V when $V_{CCIO}$ is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. $V_{CCPD}$ must be 3.0 V when $V_{CCIO}$ is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect $V_{CCBAT}$ to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors $V_{CCBAT}$. Stratix V devices will not exit POR if $V_{CCBAT}$ stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)**

| Symbol | Description | Devices | Minimum (4) | Typical | Maximum (4) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ (1), (3) | Transceiver channel PLL power supply (left side) | GX, GS, GT | 2.85 | 3.0 | 3.15 | V |
| | | | 2.375 | 2.5 | 2.625 | |
| $V_{CCA\_GXBR}$ (1), (3) | Transceiver channel PLL power supply (right side) | GX, GS | 2.85 | 3.0 | 3.15 | V |
| | | | 2.375 | 2.5 | 2.625 | |
| $V_{CCA\_GTBR}$ | Transceiver channel PLL power supply (right side) | GT | 2.85 | 3.0 | 3.15 | V |
| $V_{CCHIP\_L}$ | Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHIP\_R}$ | Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_L}$ | Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_R}$ | Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
| | Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCR\_GXBL}$ (2) | Receiver analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements**

| Conditions | Core Speed Grade | VCCR_GXB & VCCT_GXB (2) | VCCA_GXB | VCCH_GXB | Unit |
|---|---|---|---|---|---|
| If BOTH of the following conditions are true:<br>■ Data rate > 10.3 Gbps.<br>■ DFE is used. | All | 1.05 | 3.0 | 1.5 | V |
| If ANY of the following conditions are true (1):<br>■ ATX PLL is used.<br>■ Data rate > 6.5Gbps.<br>■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. | All | 1.0 | | | |
| If ALL of the following conditions are true:<br>■ ATX PLL is not used.<br>■ Data rate ≤ 6.5Gbps.<br>■ DFE, AEQ, and EyeQ are not used. | C1, C2, I2, and I3YY | 0.90 | 2.5 | | |
| | C2L, C3, C4, I2L, I3, I3L, and I4 | 0.85 | 2.5 | | |

**Notes to Table 8:**

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

### Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

**Table 9. I/O Pin Leakage Current for Stratix V Devices (1)**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

**Note to Table 9:**

(1) If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

### Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

**Table 10. Bus Hold Parameters for Stratix V Devices**

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |
| High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (minimum) | –22.5 | — | –25.0 | — | –30.0 | — | –50.0 | — | –70.0 | — | µA |
| Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | –120 | — | –160 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices (1) (Part 1 of 2)**

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 25-Ω $R_S$ | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

## Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

**Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)**

| Symbol | Description | $V_{CCIO}$ Conditions (V) (3) | Value (4) | Unit |
|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5% | 25 | kΩ |
| | | 2.5 ±5% | 25 | kΩ |
| | | 1.8 ±5% | 25 | kΩ |
| | | 1.5 ±5% | 25 | kΩ |
| | | 1.35 ±5% | 25 | kΩ |
| | | 1.25 ±5% | 25 | kΩ |
| | | 1.2 ±5% | 25 | kΩ |

**Notes to Table 16:**

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

## I/O Standard Specifications

Table 17 through Table 22 list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

**Table 17. Single-Ended I/O Standards for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-12 Class I, II | 1.14 | 1.20 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.53 * $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | — | — | — |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 16 | –16 |
| SSTL-135 Class I, II | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-125 Class I, II | — | $V_{REF}$ – 0.85 | $V_{REF}$ + 0.85 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-12 Class I, II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 2 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5 | — | — | 0 to –0.5 | — | — | 0 to –0.5 | — | % |
| On-chip termination resistors (21) | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Absolute $V_{MAX}$ (5) | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | |
| Absolute $V_{MIN}$ | — | –0.4 | — | — | –0.4 | — | — | –0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | 200 | — | 1600 | mV |
| $V_{ICM}$ (AC coupled) (3) | Dedicated reference clock pin | 1050/1000/900/850 (2) | | | 1050/1000/900/850 (2) | | | 1050/1000/900/850 (2) | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 (4) | | | 1.0/0.9/0.85 (4) | | | 1.0/0.9/0.85 (4) | | | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise (622 MHz) (20) | 100 Hz | — | — | -70 | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | — | — | -90 | dBc/Hz |
| | 10 kHz | — | — | -100 | — | — | -100 | — | — | -100 | dBc/Hz |
| | 100 kHz | — | — | -110 | — | — | -110 | — | — | -110 | dBc/Hz |
| | ≥1 MHz | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (100 MHz) (17) | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | — | — | 3 | ps (rms) |
| $R_{REF}$ (19) | — | — | 1800 ±1% | — | — | 1800 ±1% | — | — | 1800 ±1% | — | Ω |
| **Transceiver Clocks** | | | | | | | | | | | |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | — | 100 or 125 | — | MHz |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 3 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | 100 | — | 125 | MHz |
| **Receiver** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Data rate (Standard PCS) (9), (23) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) (9), (23) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Absolute $V_{MAX}$ for a receiver pin (5) | — | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | –0.4 | — | — | –0.4 | — | — | –0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration (22) | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration (18), (22) | $V_{CCR\_GXB}$ = 1.0 V/1.05 V ($V_{ICM}$ = 0.70 V) | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | V |
| | $V_{CCR\_GXB}$ = 0.90 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| | $V_{CCR\_GXB}$ = 0.85 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins (6), (22), (27) | — | 85 | — | — | 85 | — | — | 85 | — | — | mV |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 6 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| **CMU PLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 (24) | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 7 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |

**Notes to Table 23:**

(1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the $V_{CCR\_GXB}$ power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

(4) This supply follows VCCR_GXB.

(5) The device cannot tolerate prolonged operation at this absolute maximum.

(6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(8) The input reference clock frequency options depend on the data rate and the device speed grade.

(9) The line data rate may be limited by PCS-FPGA interface speed grade.

(10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(11) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(12) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

(13) $t_{LTD\_manual}$ is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

(14) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

(15) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(16) $t_{pll\_lock}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(18) The maximum peak to peak differential input voltage $V_{ID}$ after device configuration is equal to 4 × (absolute $V_{MAX}$ for receiver pin - $V_{ICM}$).

(19) For ES devices, $R_{REF}$ is 2000 Ω ±1%.

(20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(22) Refer to Figure 2.

(23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(24) I3YY devices can achieve data rates up to 10.3125 Gbps.

(25) When you use fPLL as a TXPLL of the transceiver.

(26) `REFCLK` performance requires to meet transmitter `REFCLK` phase noise specification.

(27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Input Reference Clock Frequency (CMU PLL) (6) | — | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) (6) | — | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | 20% to 80% | — | — | 400 | — | — | 400 | ps |
| Fall time | 80% to 20% | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5 | — | — | 0 to –0.5 | — | % |
| On-chip termination resistors (19) | — | — | 100 | — | — | 100 | — | Ω |
| Absolute $V_{MAX}$ (3) | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | |
| Absolute $V_{MIN}$ | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| $V_{ICM}$ (AC coupled) | Dedicated reference clock pin | 1050/1000 (2) | | | 1050/1000 (2) | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 (22) | | | 1.0/0.9/0.85 (22) | | | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Differential on-chip termination resistors | GT channels | — | 100 | — | — | 100 | — | Ω |
| | GX channels | (8) | | | | | | |
| $V_{OCM}$ (AC coupled) | GT channels | — | 500 | — | — | 500 | — | mV |
| | GX channels | (8) | | | | | | |
| Rise/Fall time | GT channels | — | 15 | — | — | 15 | — | ps |
| | GX channels | (8) | | | | | | |
| Intra-differential pair skew | GX channels | (8) | | | | | | |
| Intra-transceiver block transmitter channel-to-channel skew | GX channels | (8) | | | | | | |
| Inter-transceiver block transmitter channel-to-channel skew | GX channels | (8) | | | | | | |
| **CMU PLL** | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 8500 | Mbps |
| $t_{pll\_powerdown}$ (13) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (14) | — | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | |
| Supported Data Rate Range for GX Channels | VCO post-divider L=2 | 8000 | — | 12500 | 8000 | — | 8500 | Mbps |
| | L=4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| Supported Data Rate Range for GT Channels | VCO post-divider L=2 | 9800 | — | 14025 | 9800 | — | 12890 | Mbps |
| $t_{pll\_powerdown}$ (13) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (14) | — | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3.125 (23) | 600 | — | 3250/ 3.125 (23) | Mbps |
| $t_{pll\_powerdown}$ (13) | — | 1 | — | — | 1 | — | — | µs |

Figure 6 shows the Stratix V DC gain curves for GT channels.

**Figure 6. DC Gain Curves for GT Channels**

## Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)**

| Mode | Peformance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | C1 | C2, C2L | I2, I2L | C3 | I3, I3L, I3YY | C4 | I4 | |
| **Modes using Three DSPs** | | | | | | | | |
| One complex 18 x 25 | 425 | 425 | 415 | 340 | 340 | 275 | 265 | MHz |
| **Modes using Four DSPs** | | | | | | | | |
| One complex 27 x 27 | 465 | 465 | 465 | 380 | 380 | 300 | 290 | MHz |

## Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

**Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 1 of 2)**

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| MLAB | Single port, all supported widths | 0 | 1 | 450 | 450 | 400 | 315 | 450 | 400 | 315 | MHz |
| | Simple dual-port, x32/x64 depth | 0 | 1 | 450 | 450 | 400 | 315 | 450 | 400 | 315 | MHz |
| | Simple dual-port, x16 depth (3) | 0 | 1 | 675 | 675 | 533 | 400 | 675 | 533 | 400 | MHz |
| | ROM, all supported widths | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |

**Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 2 of 2)**

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| M20K Block | Single-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port with the read-during-write option set to **Old Data**, all supported widths | 0 | 1 | 525 | 525 | 455 | 400 | 525 | 455 | 400 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 0 | 1 | 450 | 450 | 400 | 350 | 450 | 400 | 350 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |
| | True dual port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | ROM, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |

**Notes to Table 33:**

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in $F_{MAX}$.

(3) The $F_{MAX}$ specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

## Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

**Table 34. Internal Temperature Sensing Diode Specification**

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time | Resolution | Minimum Resolution with no Missing Codes |
|---|---|---|---|---|---|---|
| –40°C to 100°C | ±8°C | No | 1 MHz, 500 KHz | < 100 ms | 8 bits | 8 bits |

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

**Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices**

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $I_{bias}$, diode source current | 8 | — | 200 | μA |
| $V_{bias,}$ voltage across diode | 0.3 | — | 0.9 | V |
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

**Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)**

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (6) | — | (8) | (6) | — | (8) | (6) | — | (8) | (6) | — | (8) | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| **DPA Mode** | | | | | | | | | | | | | | |
| DPA run length | — | — | — | 10000 | — | — | 10000 | — | — | 10000 | — | — | 10000 | UI |
| **Soft CDR mode** | | | | | | | | | | | | | | |
| Soft-CDR PPM tolerance | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ± PPM |
| **Non DPA Mode** | | | | | | | | | | | | | | |
| Sampling Window | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |

**Notes to Table 36:**

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The $F_{MAX}$ specification is based on the fast clock used for serial data. The interface $F_{MAX}$ is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

**Table 49. DCLK-to-DATA[] Ratio (1) (Part 2 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×32 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 4 |
| | Enabled | Disabled | 8 |
| | Enabled | Enabled | 8 |

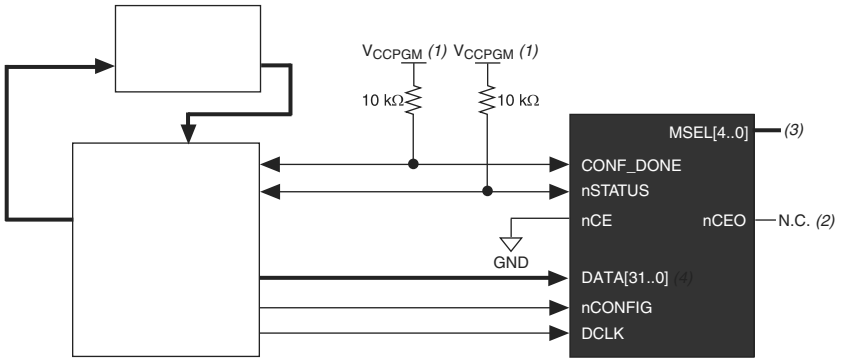
**Note to Table 49:**

(1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

**Figure 11. Single Device FPP Configuration Using an External Host**




**Notes to Figure 11:**

(1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device. $V_{CCPGM}$ must be high enough to meet the $V_{IH}$ specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with $V_{CCPGM}$.

(2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.

(3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(4) If you use FPP ×8, use DATA[7..0]. If you use FPP ×16, use DATA[15..0].

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is more than 1.

**Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1 (1)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (2) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (2) | µs |
| $t_{CF2CK}$ (5) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (5) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | N–1/$f_{DCLK}$ (5) | — | s |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_R$ | Input rise time | — | 40 | ns |
| $t_F$ | Input fall time | — | 40 | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode (3) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (4) | — | — |

**Notes to Table 51:**

(1) Use these timing parameters when you use the decompression and design security features.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(5) N is the DCLK-to-DATA ratio and $f_{DCLK}$ is the DCLK frequency the system is operating.

(6) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

**Table 61. Document Revision History (Part 2 of 3)**

| Date | Version | Changes |
|---|---|---|
| November 2014 | 3.3 | ■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.<br>■ Added the I3YY speed grade to the $V_{CC}$ description in Table 6.<br>■ Added the I3YY speed grade to $V_{CCHIP\_L}$, $V_{CCHIP\_R}$, $V_{CCHSSI\_L}$, and $V_{CCHSSI\_R}$ descriptions in Table 7.<br>■ Added 240-Ω to Table 11.<br>■ Changed CDR PPM tolerance in Table 23.<br>■ Added additional max data rate for fPLL in Table 23.<br>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.<br>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.<br>■ Changed CDR PPM tolerance in Table 28.<br>■ Added additional max data rate for fPLL in Table 28.<br>■ Changed the mode descriptions for MLAB and M20K in Table 33.<br>■ Changed the Max value of $f_{HSCLK\_OUT}$ for the C2, C2L, I2, I2L speed grades in Table 36.<br>■ Changed the frequency ranges for C1 and C2 in Table 39.<br>■ Changed the **.rbf** file sizes for 5SGSD6 and 5SGSD8 in Table 47.<br>■ Added note about `nSTATUS` to Table 50, Table 51, Table 54.<br>■ Changed the available settings in Table 58.<br>■ Changed the note in “Periphery Performance”.<br>■ Updated the “I/O Standard Specifications” section.<br>■ Updated the “Raw Binary File Size” section.<br>■ Updated the receiver voltage input range in Table 22.<br>■ Updated the max frequency for the LVDS clock network in Table 36.<br>■ Updated the `DCLK` note to Figure 11.<br>■ Updated Table 23 $VO_{CM}$ (DC Coupled) condition.<br>■ Updated Table 6 and Table 7.<br>■ Added the `DCLK` specification to Table 55.<br>■ Updated the notes for Table 47.<br>■ Updated the list of parameters for Table 56. |
| November 2013 | 3.2 | ■ Updated Table 28 |
| November 2013 | 3.1 | ■ Updated Table 33 |
| November 2013 | 3.0 | ■ Updated Table 23 and Table 28 |
| October 2013 | 2.9 | ■ Updated the “Transceiver Characterization” section |
| October 2013 | 2.8 | ■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59<br>■ Added Figure 1 and Figure 3<br>■ Added the “Transceiver Characterization” section<br>■ Removed all “Preliminary” designations. |