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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 135840 |
| Number of Logic Elements/Cells | 360000 |
| Total RAM Bits | 19456000 |
| Number of I/O | 360 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 780-BBGA, FCBGA |
| Supplier Device Package | 780-HBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgsmd4e3h29i3ln |

**Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CCD\_FPLL}$ | PLL digital power supply | –0.5 | 1.8 | V |
| $V_{CCA\_FPLL}$ | PLL analog power supply | –0.5 | 3.4 | V |
| $V_I$ | DC input voltage | –0.5 | 3.8 | V |
| $T_J$ | Operating junction temperature | –55 | 125 | °C |
| $T_{STG}$ | Storage temperature (No bias) | –65 | 150 | °C |
| $I_{OUT}$ | DC output current per pin | –25 | 40 | mA |

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

**Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices**

| Symbol | Description | Devices | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ | Transceiver channel PLL power supply (left side) | GX, GS, GT | –0.5 | 3.75 | V |
| $V_{CCA\_GXBR}$ | Transceiver channel PLL power supply (right side) | GX, GS | –0.5 | 3.75 | V |
| $V_{CCA\_GTBR}$ | Transceiver channel PLL power supply (right side) | GT | –0.5 | 3.75 | V |
| $V_{CCHIP\_L}$ | Transceiver hard IP power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCHIP\_R}$ | Transceiver hard IP power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCHSSI\_L}$ | Transceiver PCS power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCHSSI\_R}$ | Transceiver PCS power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCR\_GXBL}$ | Receiver analog power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCR\_GXBR}$ | Receiver analog power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCR\_GTBR}$ | Receiver analog power supply for GT channels (right side) | GT | –0.5 | 1.35 | V |
| $V_{CCT\_GXBL}$ | Transmitter analog power supply (left side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCT\_GXBR}$ | Transmitter analog power supply (right side) | GX, GS, GT | –0.5 | 1.35 | V |
| $V_{CCT\_GTBR}$ | Transmitter analog power supply for GT channels (right side) | GT | –0.5 | 1.35 | V |
| $V_{CCL\_GTBR}$ | Transmitter clock network power supply (right side) | GT | –0.5 | 1.35 | V |
| $V_{CCH\_GXBL}$ | Transmitter output buffer power supply (left side) | GX, GS, GT | –0.5 | 1.8 | V |
| $V_{CCH\_GXBR}$ | Transmitter output buffer power supply (right side) | GX, GS, GT | –0.5 | 1.8 | V |

### Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

## Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

**Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)**

| Symbol | Description | $V_{CCIO}$ Conditions (V) (3) | Value (4) | Unit |
|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5% | 25 | kΩ |
| | | 2.5 ±5% | 25 | kΩ |
| | | 1.8 ±5% | 25 | kΩ |
| | | 1.5 ±5% | 25 | kΩ |
| | | 1.35 ±5% | 25 | kΩ |
| | | 1.25 ±5% | 25 | kΩ |
| | | 1.2 ±5% | 25 | kΩ |

**Notes to Table 16:**

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

## I/O Standard Specifications

Table 17 through Table 22 list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

**Table 17. Single-Ended I/O Standards for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | –2 |

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5* $V_{CCIO}$ | — | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5*$V_{CCIO}$ – 0.12 | 0.5* $V_{CCIO}$ | 0.5*$V_{CCIO}$ + 0.12 | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.44 | 0.44 |

**Table 22. Differential I/O Standard Specifications for Stratix V Devices (7)**

| I/O Standard | $V_{CCIO}$ (V) (10) | | | $V_{ID}$ (mV) (8) | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) (6) | | | $V_{OCM}$ (V) (6) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18. | | | | | | | | | | | | | | |
| 2.5 V LVDS (1) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | $D_{MAX} \leq$ 700 Mbps | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| BLVDS (5) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |
| RSDS (HIO) (2) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) (3) | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL (4), (9) | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq$ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} >$ 700 Mbps | 1.6 | — | — | — | — | — | — |

**Notes to Table 22:**

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

(5) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. They depend on the system topology.

(6) RL range: $90 \leq RL \leq 110\ \Omega$ .

(7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.

(8) The minimum VID value is applicable over the entire common mode range, VCM.

(9) LVPECL is only supported on dedicated clock input pins.

(10) Differential inputs are powered by VCCPD which requires 2.5 V.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 4 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors (21) | 85–Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100–Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120–Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |
| | 150-Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |
| $V_{ICM}$ (AC and DC coupled) | $V_{CCR\_GXB}$ = 0.85 V or 0.9 V full bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR\_GXB}$ = 0.85 V or 0.9 V half bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR\_GXB}$ = 1.0 V/1.05 V full bandwidth | — | 700 | — | — | 700 | — | — | 700 | — | mV |
| | $V_{CCR\_GXB}$ = 1.0 V half bandwidth | — | 750 | — | — | 750 | — | — | 750 | — | mV |
| $t_{LTR}$ (11) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$ (12) | — | 4 | — | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD\_manual}$ (13) | — | 4 | — | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR\_LTD\_manual}$ (14) | — | 15 | — | — | 15 | — | — | 15 | — | — | µs |
| Run Length | — | — | — | 200 | — | — | 200 | — | — | 200 | UI |
| Programmable equalization (AC Gain) (10) | Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz) | — | — | 16 | — | — | 16 | — | — | 16 | dB |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 5 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 2 | — | — | 2 | — | — | 2 | — | dB |
| | DC Gain Setting = 2 | — | 4 | — | — | 4 | — | — | 4 | — | dB |
| | DC Gain Setting = 3 | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| | DC Gain Setting = 4 | — | 8 | — | — | 8 | — | — | 8 | — | dB |
| **Transmitter** | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Data rate (10G PCS) | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Rise time (7) | 20% to 80% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Fall time (7) | 80% to 20% | 30 | — | 160 | 30 | — | 160 | 30 | — | 160 | ps |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | — | — | 120 | ps |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 6 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| **CMU PLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 (24) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **ATX PLL** | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 (24) | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (16) | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| **fPLL** | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | 600 | — | 3250/ 3125 (25) | Mbps |
| $t_{pll\_powerdown}$ (15) | — | 1 | — | — | 1 | — | — | 1 | — | — | µs |

Table 26 shows the approximate maximum data rate using the 10G PCS.

**Table 26. Stratix V 10G PCS Approximate Maximum Data Rate** *(1)*

| Mode *(2)* | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|---|---|---|---|---|---|---|---|---|
| | | **PCS Width** | **64** | **66/67** | **50** | **40** | **64/66/67** | **32** |
| FIFO or Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 14.1 | 14.1 | 10.69 | 14.1 | 13.6 | 13.6 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 12.5 | 12.5 |
| | | C3, I3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 Gbps | | | | | |
| | | C3, I3, I3L core speed grade | | | | | | |
| | | C4, I4 core speed grade | | | | | | |
| | | I3YY core speed grade | 10.3125 Gbps | | | | | |

**Notes to Table 26**:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) (1)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors (7) | GT channels | — | 100 | — | — | 100 | — | Ω |
| Differential on-chip termination resistors for GX channels (19) | 85-Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100-Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120-Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |
| | 150-Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |
| $V_{ICM}$ (AC coupled) | GT channels | — | 650 | — | — | 650 | — | mV |
| VICM (AC and DC coupled) for GX Channels | VCCR_GXB = 0.85 V or 0.9 V | — | 600 | — | — | 600 | — | mV |
| | VCCR_GXB = 1.0 V full bandwidth | — | 700 | — | — | 700 | — | mV |
| | VCCR_GXB = 1.0 V half bandwidth | — | 750 | — | — | 750 | — | mV |
| $t_{LTR}$ (9) | — | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$ (10) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD\_manual}$ (11) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR\_LTD\_manual}$ (12) | — | 15 | — | — | 15 | — | — | µs |
| Run Length | GT channels | — | — | 72 | — | — | 72 | CID |
| | GX channels | (8) | | | | | | |
| CDR PPM | GT channels | — | — | 1000 | — | — | 1000 | ± PPM |
| | GX channels | (8) | | | | | | |
| Programmable equalization (AC Gain) (5) | GT channels | — | — | 14 | — | — | 14 | dB |
| | GX channels | (8) | | | | | | |
| Programmable DC gain (6) | GT channels | — | — | 7.5 | — | — | 7.5 | dB |
| | GX channels | (8) | | | | | | |
| Differential on-chip termination resistors (7) | GT channels | — | 100 | — | — | 100 | — | Ω |
| **Transmitter** | | | | | | | | |
| Supported I/O Standards | — | 1.4-V and 1.5-V PCML | | | | | | |
| Data rate (Standard PCS) | GX channels | 600 | — | 8500 | 600 | — | 8500 | Mbps |
| Data rate (10G PCS) | GX channels | 600 | — | 12,500 | 600 | — | 12,500 | Mbps |

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

# Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

## Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

**Table 30. Clock Tree Performance for Stratix V Devices** *(1)*

| Symbol | Performance | | | Unit |
|---|---|---|---|---|
| | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 | |
| Global and Regional Clock | 717 | 650 | 580 | MHz |
| Periphery Clock | 550 | 500 | 500 | MHz |

**Note to Table 30:**

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

## PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

**Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (C1, C2, C2L, I2, and I2L speed grades) | 5 | — | 800 (1) | MHz |
| | Input clock frequency (C3, I3, I3L, and I3YY speed grades) | 5 | — | 800 (1) | MHz |
| | Input clock frequency (C4, I4 speed grades) | 5 | — | 650 (1) | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{FINPFD}$ | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| $f_{VCO}$ (9) | PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C3, I3, I3L, I3YY speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grades) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades) | — | — | 717 (2) | MHz |
| | Output frequency for an internal global or regional clock (C3, I3, I3L speed grades) | — | — | 650 (2) | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grades) | — | — | 580 (2) | MHz |
| $f_{OUT\_EXT}$ | Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades) | — | — | 800 (2) | MHz |
| | Output frequency for an external clock output (C3, I3, I3L speed grades) | — | — | 667 (2) | MHz |
| | Output frequency for an external clock output (C4, I4 speed grades) | — | — | 553 (2) | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to **50%**) | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic Configuration Clock used for `mgmt_clk` and `scanclk` | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from the end-of-device configuration or deassertion of `areset` | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth (7) | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | 10 | — | — | ns |

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)**

| Mode | Peformance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | C1 | C2, C2L | I2, I2L | C3 | I3, I3L, I3YY | C4 | I4 | |
| **Modes using Three DSPs** | | | | | | | | |
| One complex 18 x 25 | 425 | 425 | 415 | 340 | 340 | 275 | 265 | MHz |
| **Modes using Four DSPs** | | | | | | | | |
| One complex 27 x 27 | 465 | 465 | 465 | 380 | 380 | 300 | 290 | MHz |

## Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

**Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 1 of 2)**

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| MLAB | Single port, all supported widths | 0 | 1 | 450 | 450 | 400 | 315 | 450 | 400 | 315 | MHz |
| | Simple dual-port, x32/x64 depth | 0 | 1 | 450 | 450 | 400 | 315 | 450 | 400 | 315 | MHz |
| | Simple dual-port, x16 depth (3) | 0 | 1 | 675 | 675 | 533 | 400 | 675 | 533 | 400 | MHz |
| | ROM, all supported widths | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices (1), (2) (Part 2 of 2)**

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C4,I4 | 8 | 16 | ps |

**Notes to Table 40:**

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

**Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{DQS\_PSERR}$) for Stratix V Devices (1)**

| Number of DQS Delay Buffers | C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|---|---|---|---|---|---|
| 1 | 28 | 28 | 30 | 32 | ps |
| 2 | 56 | 56 | 60 | 64 | ps |
| 3 | 84 | 84 | 90 | 96 | ps |
| 4 | 112 | 112 | 120 | 128 | ps |

**Notes to Table 41:**

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is ±78 ps or ±39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (2), (3) (Part 1 of 2)**

| Clock Network | Parameter | Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Regional | Clock period jitter | $t_{JIT(per)}$ | –50 | 50 | –50 | 50 | –55 | 55 | –55 | 55 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –100 | 100 | –100 | 100 | –110 | 110 | –110 | 110 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –50 | 50 | –50 | 50 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| Global | Clock period jitter | $t_{JIT(per)}$ | –75 | 75 | –75 | 75 | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –150 | 150 | –150 | 150 | –165 | 165 | –165 | 165 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –75 | 75 | –75 | 75 | –90 | 90 | –90 | 90 | ps |

### Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

**Table 44. Worst-Case DCD on Stratix V I/O Pins** *(1)*

| Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4,I4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |

**Note to Table 44:**

(1) The DCD numbers do not cover the core clock network.

# Configuration Specification

## POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

**Table 45. Fast and Standard POR Delay Specification** *(1)*

| POR Delay | Minimum | Maximum |
|---|---|---|
| Fast | 4 ms | 12 ms |
| Standard | 100 ms | 300 ms |

**Note to Table 45:**

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period *(2)* | 30 | — | ns |
| $t_{JCP}$ | TCK clock period *(2)* | 167 | — | ns |
| $t_{JCH}$ | TCK clock high time *(2)* | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time *(2)* | 14 | — | ns |
| $t_{JPSU\ (TDI)}$ | TDI JTAG port setup time | 2 | — | ns |
| $t_{JPSU\ (TMS)}$ | TMS JTAG port setup time | 3 | — | ns |

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) (4), (5) |
|---|---|---|---|---|
| Stratix V E (1) | 5SEE9 | — | 342,742,976 | 700,888 |
| | 5SEEB | — | 342,742,976 | 700,888 |

**Notes to Table 47:**

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
(2) 36-transceiver devices.
(3) 24-transceiver devices.
(4) File size for the periphery image.
(5) The IOCSR **.rbf** size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (**.hex**) or tabular text file (**.ttf**) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GX | A3 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | A4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | A5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | AB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | B5 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B6 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | BB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| GT | C5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | C7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial (1) | | | Fast Passive Parallel (2) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GS | D3 | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D5 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | D6 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| | D8 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| E | E9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | EB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |

**Notes to Table 48:**

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

## DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[] ratio for each combination.

**Table 49. DCLK-to-DATA[] Ratio (1) (Part 1 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

## Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

**Table 52. DCLK Frequency Specification in the AS Configuration Scheme (1), (2)**

| Minimum | Typical | Maximum | Unit |
|---|---|---|---|
| 5.3 | 7.9 | 12.5 | MHz |
| 10.6 | 15.7 | 25.0 | MHz |
| 21.3 | 31.4 | 50.0 | MHz |
| 42.6 | 62.9 | 100.0 | MHz |

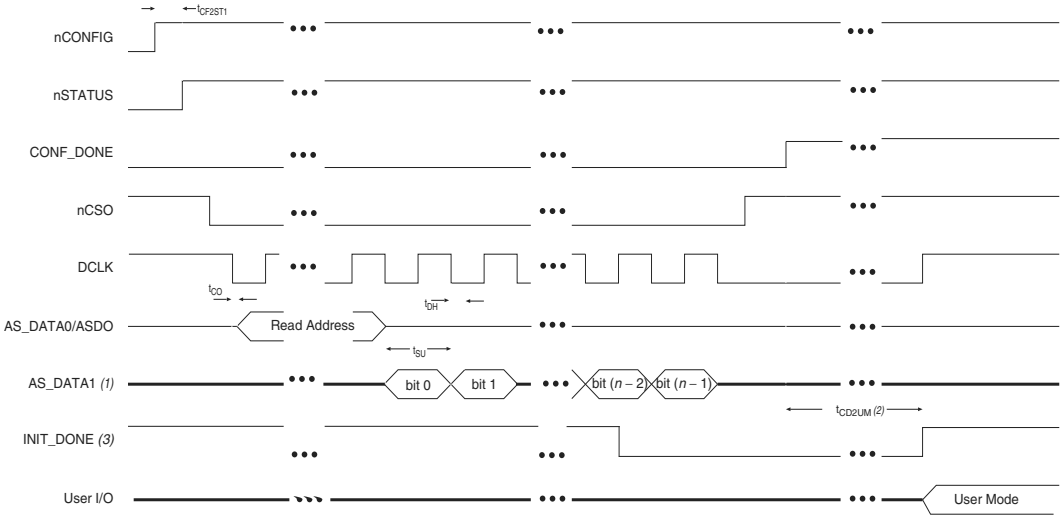
**Notes to Table 52:**

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

**Figure 14. AS Configuration Timing**




**Notes to Figure 14:**

(1) If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.

(2) The initialization clock can be from internal oscillator or CLKUSR pin.

(3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices (1), (2) (Part 1 of 2)**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CO}$ | DCLK falling edge to AS_DATA0/ASDO output | — | 2 | ns |
| $t_{SU}$ | Data setup time before falling edge on DCLK | 1.5 | — | ns |
| $t_{H}$ | Data hold time after falling edge on DCLK | 0 | — | ns |

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model | | Slow Model | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.793 | 2.793 | 2.992 | 3.192 | 2.811 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.838 | 0.838 | 0.924 | 1.011 | 0.843 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.415 | 0.415 | 0.458 | 0.503 | 0.418 | 0.456 | 0.499 | ns |

**Notes to Table 58:**

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

(2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)**

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $D_{OUTBUF}$ | Rising and/or falling edge delay | 0 (default) | ps |
| | | 25 | ps |
| | | 50 | ps |
| | | 75 | ps |

**Note to Table 59:**

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

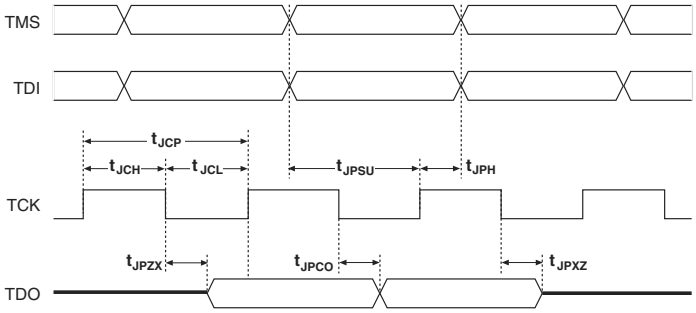
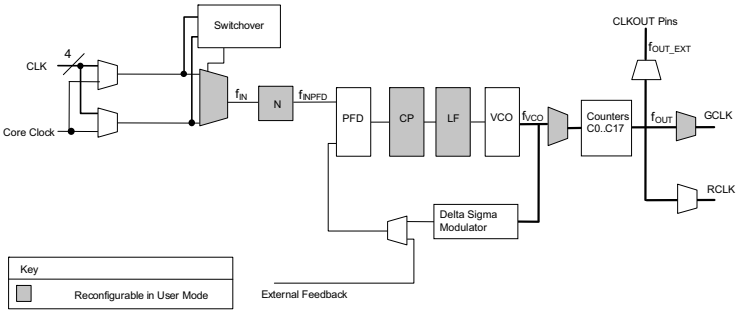
# Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| **A**<br>B<br>C | — | — |
| **D** | — | — |
| **E** | — | — |
| **F** | $f_{HSCLK}$ | Left and right PLL input clock frequency. |
| | $f_{HSDR}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| | $f_{HSDRDPA}$ | High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |

**Table 60. Glossary (Part 2 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| G<br>H<br>I | — | — |
| J | J | High-speed I/O block—Deserialization factor (width of parallel data bus). |
| J | JTAG Timing Specifications | JTAG Timing Specifications:<br>  <br> |
| K<br>L<br>M<br>N<br>O | — | — |
| P | **PLL Specifications** | **Diagram of PLL Specifications** *(1)*<br>  <br><br>**Note:**<br>(1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs. |
| Q | — | — |
| R | $R_L$ | Receiver differential input discrete resistor (external to the Stratix V device). |

# Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

| Date | Version | Changes |
|---|---|---|
| June 2018 | 3.9 | ■ Added the “Stratix V Device Overshoot Duration” figure. |
| April 2017 | 3.8 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “PS Timing Parameters for Stratix V Devices” table.<br>■ Changed the condition for 100-Ω $R_D$ in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1” table.<br>■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table. |
| June 2016 | 3.7 | ■ Added the $V_{ID}$ minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table<br>■ Added the $I_{OUT}$ specification to the “Absolute Maximum Ratings for Stratix V Devices” table. |
| December 2015 | 3.6 | ■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table. |
| December 2015 | 3.5 | ■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table. |
| July 2015 | 3.4 | ■ Changed the data rate specification for transceiver speed grade 3 in the following tables:<br>  ■ “Transceiver Specifications for Stratix V GX and GS Devices”<br>  ■ “Stratix V Standard PCS Approximate Maximum Date Rate”<br>  ■ “Stratix V 10G PCS Approximate Maximum Data Rate”<br>■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.<br>■ Changed the $t_{CO}$ maximum value in the “AS Timing Parameters for AS ´1 and AS ´4 Configurations in Stratix V Devices” table.<br>■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table. |