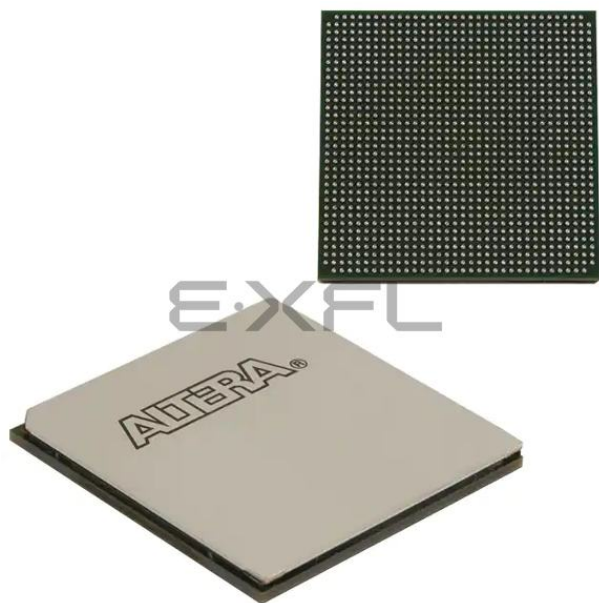




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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

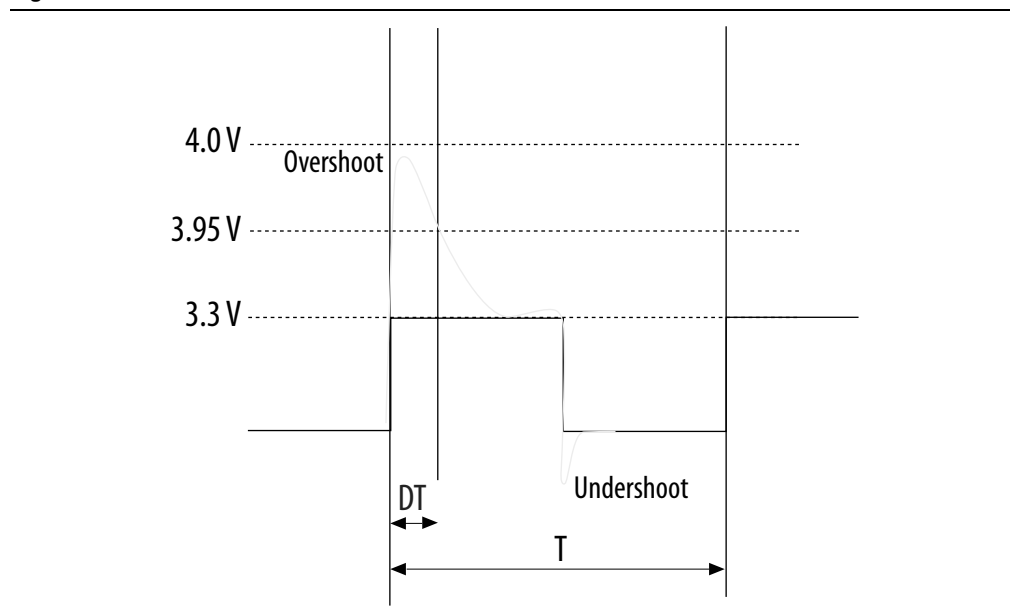
|                                |                                                                                                                                     |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                            |
| Number of LABs/CLBs            | 135840                                                                                                                              |
| Number of Logic Elements/Cells | 360000                                                                                                                              |
| Total RAM Bits                 | 19456000                                                                                                                            |
| Number of I/O                  | 432                                                                                                                                 |
| Number of Gates                | -                                                                                                                                   |
| Voltage - Supply               | 0.82V ~ 0.88V                                                                                                                       |
| Mounting Type                  | Surface Mount                                                                                                                       |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                                  |
| Package / Case                 | 1152-BBGA, FCBGA                                                                                                                    |
| Supplier Device Package        | 1152-FBGA (35x35)                                                                                                                   |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/5sgsmd4h3f35i4n">https://www.e-xfl.com/product-detail/intel/5sgsmd4h3f35i4n</a> |

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

**Table 5. Maximum Allowed Overshoot During Transitions**

| Symbol     | Description      | Condition (V) | Overshoot Duration as %<br>@ $T_J = 100^\circ\text{C}$ | Unit |
|------------|------------------|---------------|--------------------------------------------------------|------|
| $V_i$ (AC) | AC input voltage | 3.8           | 100                                                    | %    |
|            |                  | 3.85          | 64                                                     | %    |
|            |                  | 3.9           | 36                                                     | %    |
|            |                  | 3.95          | 21                                                     | %    |
|            |                  | 4             | 12                                                     | %    |
|            |                  | 4.05          | 7                                                      | %    |
|            |                  | 4.1           | 4                                                      | %    |
|            |                  | 4.15          | 2                                                      | %    |
|            |                  | 4.2           | 1                                                      | %    |

**Figure 1. Stratix V Device Overshoot Duration**



**Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)**

| Symbol               | Description                                                    | Conditions                        | Resistance Tolerance |        |              |        | Unit |
|----------------------|----------------------------------------------------------------|-----------------------------------|----------------------|--------|--------------|--------|------|
|                      |                                                                |                                   | C1                   | C2, I2 | C3, I3, I3YY | C4, I4 |      |
| 50-Ω R <sub>S</sub>  | Internal series termination without calibration (50-Ω setting) | V <sub>CCIO</sub> = 1.8 and 1.5 V | ±30                  | ±30    | ±40          | ±40    | %    |
| 50-Ω R <sub>S</sub>  | Internal series termination without calibration (50-Ω setting) | V <sub>CCIO</sub> = 1.2 V         | ±35                  | ±35    | ±50          | ±50    | %    |
| 100-Ω R <sub>D</sub> | Internal differential termination (100-Ω setting)              | V <sub>CCPD</sub> = 2.5 V         | ±25                  | ±25    | ±25          | ±25    | %    |

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

**Equation 1. OCT Variation Without Recalibration for Stratix V Devices <sup>(1), (2), (3), (4), (5), (6)</sup>**

$$R_{OCT} = R_{SCAL} \left( 1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

**Notes to Equation 1:**

- (1) The R<sub>OCT</sub> value shows the range of OCT resistance with the variation of temperature and V<sub>CCIO</sub>.
- (2) R<sub>SCAL</sub> is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power-up.
- (4) ΔV is the variation of voltage with respect to the V<sub>CCIO</sub> at power-up.
- (5) dR/dT is the percentage change of R<sub>SCAL</sub> with temperature.
- (6) dR/dV is the percentage change of R<sub>SCAL</sub> with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2) <sup>(1)</sup>**

| Symbol | Description                                      | V <sub>CCIO</sub> (V) | Typical | Unit   |
|--------|--------------------------------------------------|-----------------------|---------|--------|
| dR/dV  | OCT variation with voltage without recalibration | 3.0                   | 0.0297  | % / mV |
|        |                                                  | 2.5                   | 0.0344  |        |
|        |                                                  | 1.8                   | 0.0499  |        |
|        |                                                  | 1.5                   | 0.0744  |        |
|        |                                                  | 1.2                   | 0.1241  |        |

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) <sup>(1)</sup>**

| Symbol | Description                                          | V <sub>CCIO</sub> (V) | Typical | Unit              |
|--------|------------------------------------------------------|-----------------------|---------|-------------------|
| dR/dT  | OCT variation with temperature without recalibration | 3.0                   | 0.189   | %/ <sup>o</sup> C |
|        |                                                      | 2.5                   | 0.208   |                   |
|        |                                                      | 1.8                   | 0.266   |                   |
|        |                                                      | 1.5                   | 0.273   |                   |
|        |                                                      | 1.2                   | 0.317   |                   |

**Note to Table 13:**

(1) Valid for a V<sub>CCIO</sub> range of  $\pm 5\%$  and a temperature range of 0° to 85°C.

**Pin Capacitance**

Table 14 lists the Stratix V device family pin capacitance.

**Table 14. Pin Capacitance for Stratix V Devices**

| Symbol             | Description                                                      | Value | Unit |
|--------------------|------------------------------------------------------------------|-------|------|
| C <sub>IOTB</sub>  | Input capacitance on the top and bottom I/O pins                 | 6     | pF   |
| C <sub>IOLR</sub>  | Input capacitance on the left and right I/O pins                 | 6     | pF   |
| C <sub>OUTFB</sub> | Input capacitance on dual-purpose clock output and feedback pins | 6     | pF   |

**Hot Socketing**

Table 15 lists the hot socketing specifications for Stratix V devices.

**Table 15. Hot Socketing Specifications for Stratix V Devices**

| Symbol                    | Description                                | Maximum             |
|---------------------------|--------------------------------------------|---------------------|
| I <sub>IOPIN</sub> (DC)   | DC current per I/O pin                     | 300 $\mu$ A         |
| I <sub>IOPIN</sub> (AC)   | AC current per I/O pin                     | 8 mA <sup>(1)</sup> |
| I <sub>XCVR-TX</sub> (DC) | DC current per transceiver transmitter pin | 100 mA              |
| I <sub>XCVR-RX</sub> (DC) | DC current per transceiver receiver pin    | 50 mA               |

**Note to Table 15:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns,  $|I_{IOPIN}| = C \, dv/dt$ , in which C is the I/O pin capacitance and dv/dt is the slew rate.

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard            | $V_{CCIO}$ (V) |      |       | $V_{REF}$ (V)     |                  |                   | $V_{TT}$ (V)      |                  |                   |
|-------------------------|----------------|------|-------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|
|                         | Min            | Typ  | Max   | Min               | Typ              | Max               | Min               | Typ              | Max               |
| SSTL-2<br>Class I, II   | 2.375          | 2.5  | 2.625 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.833             | 0.9              | 0.969             | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-135<br>Class I, II | 1.283          | 1.35 | 1.418 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-125<br>Class I, II | 1.19           | 1.25 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-12<br>Class I, II  | 1.14           | 1.20 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| HSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.85              | 0.9              | 0.95              | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | 0.68              | 0.75             | 0.9               | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-12<br>Class I, II  | 1.14           | 1.2  | 1.26  | $0.47 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.53 * V_{CCIO}$ | —                 | $V_{CCIO}/2$     | —                 |
| HSUL-12                 | 1.14           | 1.2  | 1.3   | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | —                 | —                | —                 |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard            | $V_{IL(DC)}$ (V) |                   | $V_{IH(DC)}$ (V)  |                  | $V_{IL(AC)}$ (V)  | $V_{IH(AC)}$ (V)  | $V_{OL}$ (V)     | $V_{OH}$ (V)      | $I_{OI}$ (mA) | $I_{OH}$ (mA) |
|-------------------------|------------------|-------------------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|---------------|---------------|
|                         | Min              | Max               | Min               | Max              | Max               | Min               | Max              | Min               |               |               |
| SSTL-2<br>Class I       | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.608$ | $V_{TT} + 0.608$  | 8.1           | -8.1          |
| SSTL-2<br>Class II      | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.81$  | $V_{TT} + 0.81$   | 16.2          | -16.2         |
| SSTL-18<br>Class I      | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | $V_{TT} - 0.603$ | $V_{TT} + 0.603$  | 6.7           | -6.7          |
| SSTL-18<br>Class II     | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | 0.28             | $V_{CCIO} - 0.28$ | 13.4          | -13.4         |
| SSTL-15<br>Class I      | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 8             | -8            |
| SSTL-15<br>Class II     | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 16            | -16           |
| SSTL-135<br>Class I, II | —                | $V_{REF} - 0.09$  | $V_{REF} + 0.09$  | —                | $V_{REF} - 0.16$  | $V_{REF} + 0.16$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-125<br>Class I, II | —                | $V_{REF} - 0.85$  | $V_{REF} + 0.85$  | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-12<br>Class I, II  | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)**

| I/O Standard     | $V_{IL(DC)}$ (V) |                  | $V_{IH(DC)}$ (V) |                   | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V)      | $V_{OH}$ (V)      | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|------------------|------------------|------------------|------------------|-------------------|------------------|------------------|-------------------|-------------------|---------------|---------------|
|                  | Min              | Max              | Min              | Max               | Max              | Min              | Max               | Min               |               |               |
| HSTL-18 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 8             | -8            |
| HSTL-18 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 16            | -16           |
| HSTL-15 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 8             | -8            |
| HSTL-15 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$  | $V_{REF} + 0.2$  | 0.4               | $V_{CCIO} - 0.4$  | 16            | -16           |
| HSTL-12 Class I  | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 8             | -8            |
| HSTL-12 Class II | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 16            | -16           |
| HSUL-12          | —                | $V_{REF} - 0.13$ | $V_{REF} + 0.13$ | —                 | $V_{REF} - 0.22$ | $V_{REF} + 0.22$ | $0.1^* V_{CCIO}$  | $0.9^* V_{CCIO}$  | —             | —             |

**Table 20. Differential SSTL I/O Standards for Stratix V Devices**

| I/O Standard         | $V_{CCIO}$ (V) |      |       | $V_{SWING(DC)}$ (V) |                  | $V_{X(AC)}$ (V)      |              |                      | $V_{SWING(AC)}$ (V)       |                           |
|----------------------|----------------|------|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------------|---------------------------|
|                      | Min            | Typ  | Max   | Min                 | Max              | Min                  | Typ          | Max                  | Min                       | Max                       |
| SSTL-2 Class I, II   | 2.375          | 2.5  | 2.625 | 0.3                 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$   | —            | $V_{CCIO}/2 + 0.2$   | 0.62                      | $V_{CCIO} + 0.6$          |
| SSTL-18 Class I, II  | 1.71           | 1.8  | 1.89  | 0.25                | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | —            | $V_{CCIO}/2 + 0.175$ | 0.5                       | $V_{CCIO} + 0.6$          |
| SSTL-15 Class I, II  | 1.425          | 1.5  | 1.575 | 0.2                 | (1)              | $V_{CCIO}/2 - 0.15$  | —            | $V_{CCIO}/2 + 0.15$  | 0.35                      | —                         |
| SSTL-135 Class I, II | 1.283          | 1.35 | 1.45  | 0.2                 | (1)              | $V_{CCIO}/2 - 0.15$  | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$  | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19           | 1.25 | 1.31  | 0.18                | (1)              | $V_{CCIO}/2 - 0.15$  | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$  | $2(V_{IH(AC)} - V_{REF})$ | —                         |
| SSTL-12 Class I, II  | 1.14           | 1.2  | 1.26  | 0.18                | —                | $V_{REF} - 0.15$     | $V_{CCIO}/2$ | $V_{REF} + 0.15$     | -0.30                     | 0.30                      |

**Note to Table 20:**

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)**

| I/O Standard        | $V_{CCIO}$ (V) |     |       | $V_{DIF(DC)}$ (V) |     | $V_{X(AC)}$ (V) |     |      | $V_{CM(DC)}$ (V) |     |      | $V_{DIF(AC)}$ (V) |     |
|---------------------|----------------|-----|-------|-------------------|-----|-----------------|-----|------|------------------|-----|------|-------------------|-----|
|                     | Min            | Typ | Max   | Min               | Max | Min             | Typ | Max  | Min              | Typ | Max  | Min               | Max |
| HSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.2               | —   | 0.78            | —   | 1.12 | 0.78             | —   | 1.12 | 0.4               | —   |
| HSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.2               | —   | 0.68            | —   | 0.9  | 0.68             | —   | 0.9  | 0.4               | —   |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) <sup>(1)</sup>**

| Symbol/<br>Description                                         | Conditions                                             | Transceiver<br>Speed Grade 2                                                           |           |      | Transceiver<br>Speed Grade 3 |           |      | Unit |
|----------------------------------------------------------------|--------------------------------------------------------|----------------------------------------------------------------------------------------|-----------|------|------------------------------|-----------|------|------|
|                                                                |                                                        | Min                                                                                    | Typ       | Max  | Min                          | Typ       | Max  |      |
| Reference Clock                                                |                                                        |                                                                                        |           |      |                              |           |      |      |
| Supported I/O<br>Standards                                     | Dedicated<br>reference<br>clock pin                    | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS,<br>and HCSL |           |      |                              |           |      |      |
|                                                                | RX reference<br>clock pin                              | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS                                   |           |      |                              |           |      |      |
| Input Reference Clock<br>Frequency (CMU<br>PLL) <sup>(6)</sup> | —                                                      | 40                                                                                     | —         | 710  | 40                           | —         | 710  | MHz  |
| Input Reference Clock<br>Frequency (ATX PLL) <sup>(6)</sup>    | —                                                      | 100                                                                                    | —         | 710  | 100                          | —         | 710  | MHz  |
| Rise time                                                      | 20% to 80%                                             | —                                                                                      | —         | 400  | —                            | —         | 400  | ps   |
| Fall time                                                      | 80% to 20%                                             | —                                                                                      | —         | 400  | —                            | —         | 400  |      |
| Duty cycle                                                     | —                                                      | 45                                                                                     | —         | 55   | 45                           | —         | 55   | %    |
| Spread-spectrum<br>modulating clock<br>frequency               | PCI Express<br>(PCIe)                                  | 30                                                                                     | —         | 33   | 30                           | —         | 33   | kHz  |
| Spread-spectrum<br>downspread                                  | PCIe                                                   | —                                                                                      | 0 to −0.5 | —    | —                            | 0 to −0.5 | —    | %    |
| On-chip termination<br>resistors <sup>(19)</sup>               | —                                                      | —                                                                                      | 100       | —    | —                            | 100       | —    | Ω    |
| Absolute V <sub>MAX</sub> <sup>(3)</sup>                       | Dedicated<br>reference<br>clock pin                    | —                                                                                      | —         | 1.6  | —                            | —         | 1.6  | V    |
|                                                                | RX reference<br>clock pin                              | —                                                                                      | —         | 1.2  | —                            | —         | 1.2  |      |
| Absolute V <sub>MIN</sub>                                      | —                                                      | -0.4                                                                                   | —         | —    | -0.4                         | —         | —    | V    |
| Peak-to-peak<br>differential input<br>voltage                  | —                                                      | 200                                                                                    | —         | 1600 | 200                          | —         | 1600 | mV   |
| V <sub>ICM</sub> (AC coupled)                                  | Dedicated<br>reference<br>clock pin                    | 1050/1000 <sup>(2)</sup>                                                               |           |      | 1050/1000 <sup>(2)</sup>     |           |      | mV   |
|                                                                | RX reference<br>clock pin                              | 1.0/0.9/0.85 <sup>(22)</sup>                                                           |           |      | 1.0/0.9/0.85 <sup>(22)</sup> |           |      | V    |
| V <sub>ICM</sub> (DC coupled)                                  | HCSL I/O<br>standard for<br>PCIe<br>reference<br>clock | 250                                                                                    | —         | 550  | 250                          | —         | 550  | mV   |

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) <sup>(1)</sup>**

| Symbol/<br>Description                                                                                                                              | Conditions                                                                        | Transceiver<br>Speed Grade 2                         |               |        | Transceiver<br>Speed Grade 3 |               |        | Unit     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|------------------------------------------------------|---------------|--------|------------------------------|---------------|--------|----------|
|                                                                                                                                                     |                                                                                   | Min                                                  | Typ           | Max    | Min                          | Typ           | Max    |          |
| Transmitter REFCLK<br>Phase Noise (622<br>MHz) <sup>(18)</sup>                                                                                      | 100 Hz                                                                            | —                                                    | —             | -70    | —                            | —             | -70    | dBc/Hz   |
|                                                                                                                                                     | 1 kHz                                                                             | —                                                    | —             | -90    | —                            | —             | -90    |          |
|                                                                                                                                                     | 10 kHz                                                                            | —                                                    | —             | -100   | —                            | —             | -100   |          |
|                                                                                                                                                     | 100 kHz                                                                           | —                                                    | —             | -110   | —                            | —             | -110   |          |
|                                                                                                                                                     | ≥ 1 MHz                                                                           | —                                                    | —             | -120   | —                            | —             | -120   |          |
| Transmitter REFCLK<br>Phase Jitter (100<br>MHz) <sup>(15)</sup>                                                                                     | 10 kHz to<br>1.5 MHz<br>(PCIe)                                                    | —                                                    | —             | 3      | —                            | —             | 3      | ps (rms) |
| RREF <sup>(17)</sup>                                                                                                                                | —                                                                                 | —                                                    | 1800<br>± 1%  | —      | —                            | 1800<br>± 1%  | —      | Ω        |
| <b>Transceiver Clocks</b>                                                                                                                           |                                                                                   |                                                      |               |        |                              |               |        |          |
| fixedclk clock<br>frequency                                                                                                                         | PCIe<br>Receiver<br>Detect                                                        | —                                                    | 100 or<br>125 | —      | —                            | 100 or<br>125 | —      | MHz      |
| Reconfiguration clock<br>(mgmt_clk_clk)<br>frequency                                                                                                | —                                                                                 | 100                                                  | —             | 125    | 100                          | —             | 125    | MHz      |
| <b>Receiver</b>                                                                                                                                     |                                                                                   |                                                      |               |        |                              |               |        |          |
| Supported I/O<br>Standards                                                                                                                          | —                                                                                 | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS |               |        |                              |               |        |          |
| Data rate<br>(Standard PCS) <sup>(21)</sup>                                                                                                         | GX channels                                                                       | 600                                                  | —             | 8500   | 600                          | —             | 8500   | Mbps     |
| Data rate<br>(10G PCS) <sup>(21)</sup>                                                                                                              | GX channels                                                                       | 600                                                  | —             | 12,500 | 600                          | —             | 12,500 | Mbps     |
| Data rate                                                                                                                                           | GT channels                                                                       | 19,600                                               | —             | 28,050 | 19,600                       | —             | 25,780 | Mbps     |
| Absolute V <sub>MAX</sub> for a<br>receiver pin <sup>(3)</sup>                                                                                      | GT channels                                                                       | —                                                    | —             | 1.2    | —                            | —             | 1.2    | V        |
| Absolute V <sub>MIN</sub> for a<br>receiver pin                                                                                                     | GT channels                                                                       | -0.4                                                 | —             | —      | -0.4                         | —             | —      | V        |
| Maximum peak-to-peak<br>differential input<br>voltage V <sub>ID</sub> (diff p-p)<br>before device<br>configuration <sup>(20)</sup>                  | GT channels                                                                       | —                                                    | —             | 1.6    | —                            | —             | 1.6    | V        |
|                                                                                                                                                     | GX channels                                                                       | <sup>(8)</sup>                                       |               |        |                              |               |        |          |
| Maximum peak-to-peak<br>differential input<br>voltage V <sub>ID</sub> (diff p-p)<br>after device<br>configuration <sup>(16)</sup> , <sup>(20)</sup> | GT channels<br>V <sub>CCR_GTB</sub> =<br>1.05 V<br>(V <sub>ICM</sub> =<br>0.65 V) | —                                                    | —             | 2.2    | —                            | —             | 2.2    | V        |
|                                                                                                                                                     | GX channels                                                                       | <sup>(8)</sup>                                       |               |        |                              |               |        |          |
| Minimum differential<br>eye opening at receiver<br>serial input pins <sup>(4)</sup> , <sup>(20)</sup>                                               | GT channels                                                                       | 200                                                  | —             | —      | 200                          | —             | —      | mV       |
|                                                                                                                                                     | GX channels                                                                       | <sup>(8)</sup>                                       |               |        |                              |               |        |          |

Table 29 shows the  $V_{OD}$  settings for the GT channel.

**Table 29. Typical  $V_{OD}$  Setting for GT Channel, TX Termination = 100  $\Omega$**

| Symbol                                                                      | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|-----------------------------------------------------------------------------|------------------|---------------------|
| <b><math>V_{OD}</math> differential peak to peak typical <sup>(1)</sup></b> | 0                | 0                   |
|                                                                             | 1                | 200                 |
|                                                                             | 2                | 400                 |
|                                                                             | 3                | 600                 |
|                                                                             | 4                | 800                 |
|                                                                             | 5                | 1000                |

**Note:**

(1) Refer to Figure 4.

## PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

**Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)**

| Symbol                   | Parameter                                                                                                | Min | Typ | Max                | Unit |
|--------------------------|----------------------------------------------------------------------------------------------------------|-----|-----|--------------------|------|
| $f_{IN}$                 | Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)                                            | 5   | —   | 800 <sup>(1)</sup> | MHz  |
|                          | Input clock frequency (C3, I3, I3L, and I3YY speed grades)                                               | 5   | —   | 800 <sup>(1)</sup> | MHz  |
|                          | Input clock frequency (C4, I4 speed grades)                                                              | 5   | —   | 650 <sup>(1)</sup> | MHz  |
| $f_{INPFD}$              | Input frequency to the PFD                                                                               | 5   | —   | 325                | MHz  |
| $f_{FINPFD}$             | Fractional Input clock frequency to the PFD                                                              | 50  | —   | 160                | MHz  |
| $f_{VCO}$ <sup>(9)</sup> | PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)                                              | 600 | —   | 1600               | MHz  |
|                          | PLL VCO operating range (C3, I3, I3L, I3YY speed grades)                                                 | 600 | —   | 1600               | MHz  |
|                          | PLL VCO operating range (C4, I4 speed grades)                                                            | 600 | —   | 1300               | MHz  |
| $t_{EINDUTY}$            | Input clock or external feedback clock input duty cycle                                                  | 40  | —   | 60                 | %    |
| $f_{OUT}$                | Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)            | —   | —   | 717 <sup>(2)</sup> | MHz  |
|                          | Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)                     | —   | —   | 650 <sup>(2)</sup> | MHz  |
|                          | Output frequency for an internal global or regional clock (C4, I4 speed grades)                          | —   | —   | 580 <sup>(2)</sup> | MHz  |
| $f_{OUT\_EXT}$           | Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)                        | —   | —   | 800 <sup>(2)</sup> | MHz  |
|                          | Output frequency for an external clock output (C3, I3, I3L speed grades)                                 | —   | —   | 667 <sup>(2)</sup> | MHz  |
|                          | Output frequency for an external clock output (C4, I4 speed grades)                                      | —   | —   | 553 <sup>(2)</sup> | MHz  |
| $t_{OUTDUTY}$            | Duty cycle for a dedicated external clock output (when set to 50%)                                       | 45  | 50  | 55                 | %    |
| $t_{FCOMP}$              | External feedback clock compensation time                                                                | —   | —   | 10                 | ns   |
| $f_{DYCONFIGCLK}$        | Dynamic Configuration Clock used for <code>mgmt_clk</code> and <code>scanclk</code>                      | —   | —   | 100                | MHz  |
| $t_{LOCK}$               | Time required to lock from the end-of-device configuration or deassertion of <code>areset</code>         | —   | —   | 1                  | ms   |
| $t_{DLOCK}$              | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | —   | —   | 1                  | ms   |
| $f_{CLBW}$               | PLL closed-loop low bandwidth                                                                            | —   | 0.3 | —                  | MHz  |
|                          | PLL closed-loop medium bandwidth                                                                         | —   | 1.5 | —                  | MHz  |
|                          | PLL closed-loop high bandwidth <sup>(7)</sup>                                                            | —   | 4   | —                  | MHz  |
| $t_{PLL\_PSERR}$         | Accuracy of PLL phase shift                                                                              | —   | —   | ±50                | ps   |
| $t_{ARESET}$             | Minimum pulse width on the <code>areset</code> signal                                                    | 10  | —   | —                  | ns   |

## Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface.

General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.



The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 1 of 4)**

| Symbol                                                                                     | Conditions                                         | C1  |     |     | C2, C2L, I2, I2L |     |     | C3, I3, I3L, I3YY |     |                    | C4,I4 |     |                    | Unit |
|--------------------------------------------------------------------------------------------|----------------------------------------------------|-----|-----|-----|------------------|-----|-----|-------------------|-----|--------------------|-------|-----|--------------------|------|
|                                                                                            |                                                    | Min | Typ | Max | Min              | Typ | Max | Min               | Typ | Max                | Min   | Typ | Max                |      |
| $f_{\text{HCLK\_in}}$ (input clock frequency)<br>True Differential I/O Standards           | Clock boost factor<br>$W = 1$ to 40 <sup>(4)</sup> | 5   | —   | 800 | 5                | —   | 800 | 5                 | —   | 625                | 5     | —   | 525                | MHz  |
| $f_{\text{HCLK\_in}}$ (input clock frequency)<br>Single Ended I/O Standards <sup>(3)</sup> | Clock boost factor<br>$W = 1$ to 40 <sup>(4)</sup> | 5   | —   | 800 | 5                | —   | 800 | 5                 | —   | 625                | 5     | —   | 525                | MHz  |
| $f_{\text{HCLK\_in}}$ (input clock frequency)<br>Single Ended I/O Standards                | Clock boost factor<br>$W = 1$ to 40 <sup>(4)</sup> | 5   | —   | 520 | 5                | —   | 520 | 5                 | —   | 420                | 5     | —   | 420                | MHz  |
| $f_{\text{HCLK\_OUT}}$<br>(output clock frequency)                                         | —                                                  | 5   | —   | 800 | 5                | —   | 800 | 5                 | —   | 625 <sup>(5)</sup> | 5     | —   | 525 <sup>(5)</sup> | MHz  |

**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 4)**

| Symbol                                                                                                                           | Conditions                                                                    | C1  |     |      | C2, C2L, I2, I2L |     |      | C3, I3, I3L, I3YY |     |      | C4,I4 |     |      | Unit |
|----------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----|-----|------|------------------|-----|------|-------------------|-----|------|-------|-----|------|------|
|                                                                                                                                  |                                                                               | Min | Typ | Max  | Min              | Typ | Max  | Min               | Typ | Max  | Min   | Typ | Max  |      |
| Transmitter                                                                                                                      |                                                                               |     |     |      |                  |     |      |                   |     |      |       |     |      |      |
| True Differential I/O Standards - f <sub>HSDR</sub> (data rate)                                                                  | SERDES factor J = 3 to 10 <sup>(9), (11), (12), (13), (14), (15), (16)</sup>  | (6) | —   | 1600 | (6)              | —   | 1434 | (6)               | —   | 1250 | (6)   | —   | 1050 | Mbps |
|                                                                                                                                  | SERDES factor J ≥ 4<br><br>LVDS TX with DPA <sup>(12), (14), (15), (16)</sup> | (6) | —   | 1600 | (6)              | —   | 1600 | (6)               | —   | 1600 | (6)   | —   | 1250 | Mbps |
|                                                                                                                                  | SERDES factor J = 2,<br>uses DDR Registers                                    | (6) | —   | (7)  | (6)              | —   | (7)  | (6)               | —   | (7)  | (6)   | —   | (7)  | Mbps |
|                                                                                                                                  | SERDES factor J = 1,<br>uses SDR Register                                     | (6) | —   | (7)  | (6)              | —   | (7)  | (6)               | —   | (7)  | (6)   | —   | (7)  | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup> | SERDES factor J = 4 to 10 <sup>(17)</sup>                                     | (6) | —   | 1100 | (6)              | —   | 1100 | (6)               | —   | 840  | (6)   | —   | 840  | Mbps |
| t <sub>x Jitter</sub> - True Differential I/O Standards                                                                          | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps                               | —   | —   | 160  | —                | —   | 160  | —                 | —   | 160  | —     | —   | 160  | ps   |
|                                                                                                                                  | Total Jitter for Data Rate < 600 Mbps                                         | —   | —   | 0.1  | —                | —   | 0.1  | —                 | —   | 0.1  | —     | —   | 0.1  | UI   |
| t <sub>x Jitter</sub> - Emulated Differential I/O Standards with Three External Output Resistor Network                          | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps                               | —   | —   | 300  | —                | —   | 300  | —                 | —   | 300  | —     | —   | 325  | ps   |
|                                                                                                                                  | Total Jitter for Data Rate < 600 Mbps                                         | —   | —   | 0.2  | —                | —   | 0.2  | —                 | —   | 0.2  | —     | —   | 0.25 | UI   |

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

**Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled**

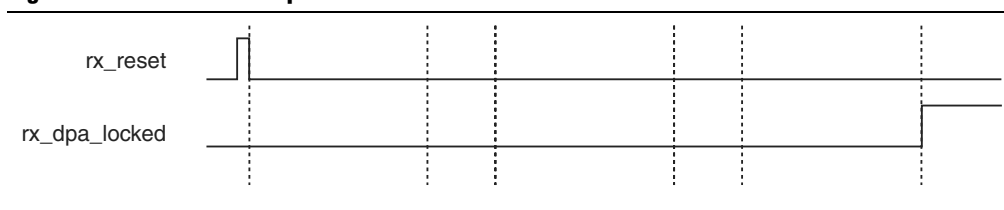


Table 37 lists the DPA lock time specifications for Stratix V devices.

**Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only <sup>(1), (2), (3)</sup>**

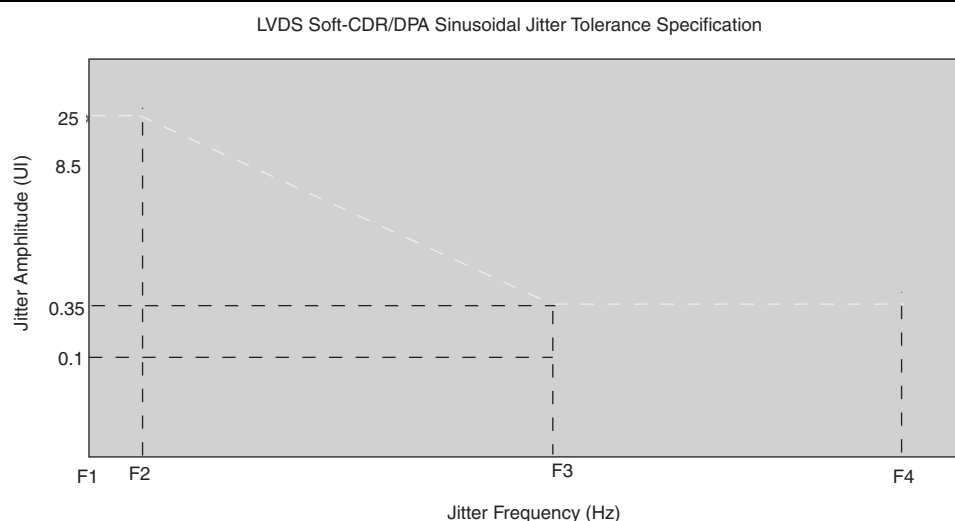
| Standard           | Training Pattern     | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions <sup>(4)</sup> | Maximum              |
|--------------------|----------------------|----------------------------------------------------------------------|---------------------------------------------------------------|----------------------|
| SPI-4              | 00000000001111111111 | 2                                                                    | 128                                                           | 640 data transitions |
| Parallel Rapid I/O | 00001111             | 2                                                                    | 128                                                           | 640 data transitions |
|                    | 10010000             | 4                                                                    | 64                                                            | 640 data transitions |
| Miscellaneous      | 10101010             | 8                                                                    | 32                                                            | 640 data transitions |
|                    | 01010101             | 8                                                                    | 32                                                            | 640 data transitions |

**Notes to Table 37:**

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq 1.25$  Gbps. Table 38 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq 1.25$  Gbps.

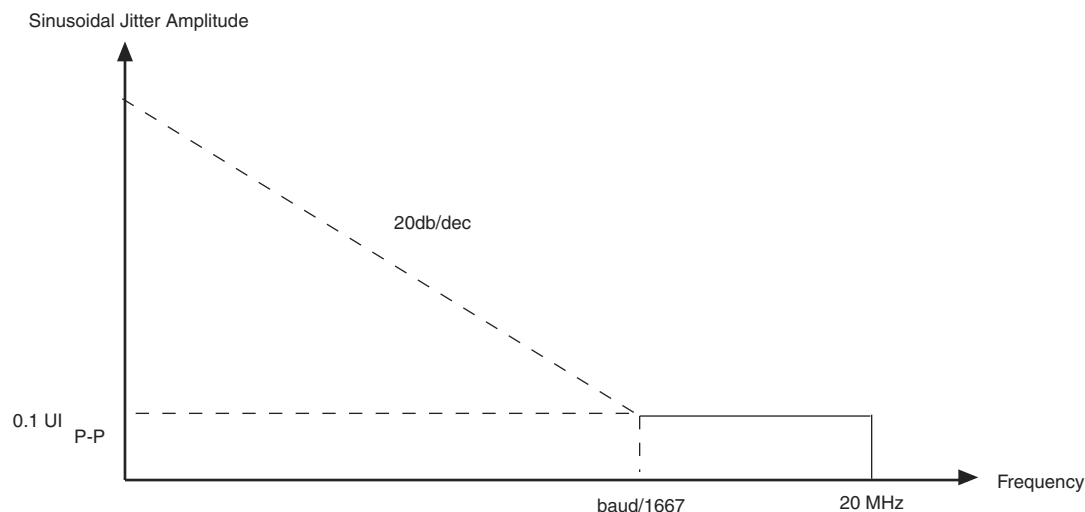
**Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $\geq 1.25$  Gbps**



**Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate  $\geq 1.25$  Gbps**

| Jitter Frequency (Hz) |            | Sinusoidal Jitter (UI) |
|-----------------------|------------|------------------------|
| F1                    | 10,000     | 25.000                 |
| F2                    | 17,565     | 25.000                 |
| F3                    | 1,493,000  | 0.350                  |
| F4                    | 50,000,000 | 0.350                  |

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $< 1.25$  Gbps.

**Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $< 1.25$  Gbps**

### DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 39. DLL Range Specifications for Stratix V Devices <sup>(1)</sup>**

| C1      | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4   | Unit |
|---------|------------------|-------------------|---------|------|
| 300-933 | 300-933          | 300-890           | 300-890 | MHz  |

**Note to Table 39:**

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

| Speed Grade      | Min | Max | Unit |
|------------------|-----|-----|------|
| C1               | 8   | 14  | ps   |
| C2, C2L, I2, I2L | 8   | 14  | ps   |
| C3,I3, I3L, I3YY | 8   | 15  | ps   |

**Table 49. DCLK-to-DATA[] Ratio <sup>(1)</sup> (Part 2 of 2)**

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|----------------------|---------------|-----------------|----------------------|
| FPP ×32              | Disabled      | Disabled        | 1                    |
|                      | Disabled      | Enabled         | 4                    |
|                      | Enabled       | Disabled        | 8                    |
|                      | Enabled       | Enabled         | 8                    |

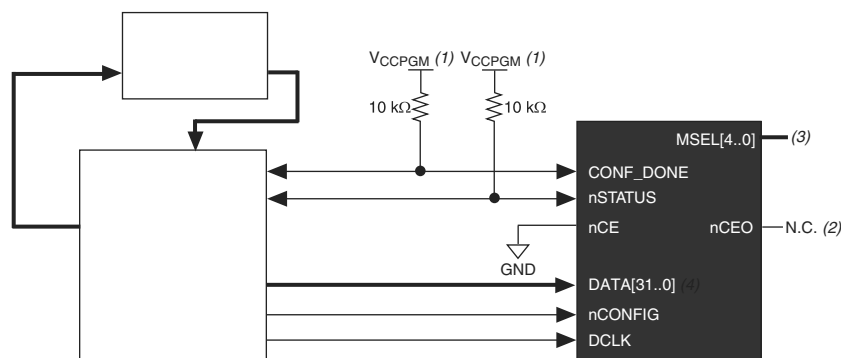
**Note to Table 49:**

- (1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

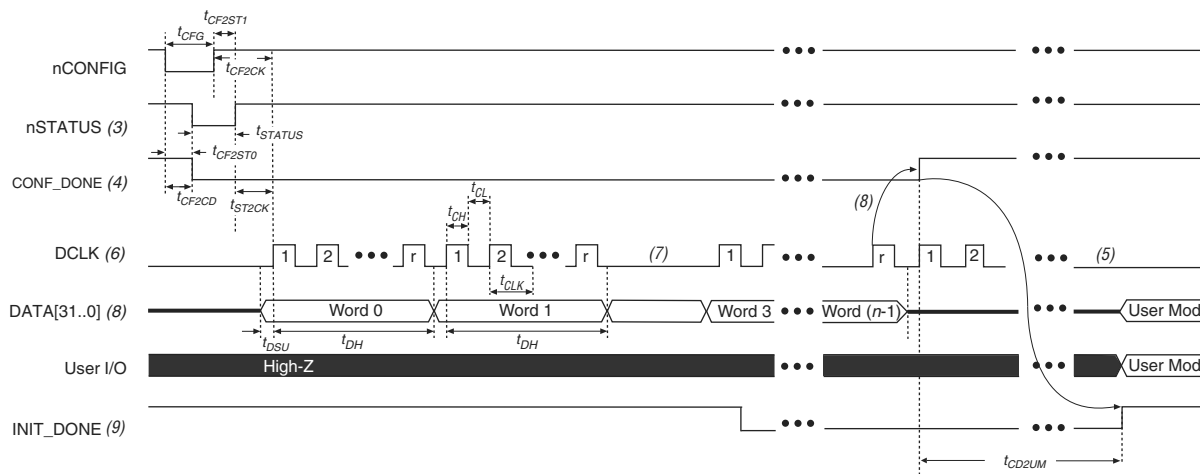


If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

**Figure 11. Single Device FPP Configuration Using an External Host****Notes to Figure 11:**

- (1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device.  $V_{CCPGM}$  must be high enough to meet the  $V_{IH}$  specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with  $V_{CCPGM}$ .
- (2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.
- (3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (4) If you use FPP ×8, use DATA[7..0]. If you use FPP ×16, use DATA[15..0].

**Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)****Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

**Table 54. PS Timing Parameters for Stratix V Devices**

| Symbol                     | Parameter                                         | Minimum                                                         | Maximum              | Units   |
|----------------------------|---------------------------------------------------|-----------------------------------------------------------------|----------------------|---------|
| $t_{CF2CD}$                | nCONFIG low to CONF_DONE low                      | —                                                               | 600                  | ns      |
| $t_{CF2ST0}$               | nCONFIG low to nSTATUS low                        | —                                                               | 600                  | ns      |
| $t_{CFG}$                  | nCONFIG low pulse width                           | 2                                                               | —                    | $\mu$ s |
| $t_{STATUS}$               | nSTATUS low pulse width                           | 268                                                             | 1,506 <sup>(1)</sup> | $\mu$ s |
| $t_{CF2ST1}$               | nCONFIG high to nSTATUS high                      | —                                                               | 1,506 <sup>(2)</sup> | $\mu$ s |
| $t_{CF2CK}$ <sup>(5)</sup> | nCONFIG high to first rising edge on DCLK         | 1,506                                                           | —                    | $\mu$ s |
| $t_{ST2CK}$ <sup>(5)</sup> | nSTATUS high to first rising edge of DCLK         | 2                                                               | —                    | $\mu$ s |
| $t_{DSU}$                  | DATA [] setup time before rising edge on DCLK     | 5.5                                                             | —                    | ns      |
| $t_{DH}$                   | DATA [] hold time after rising edge on DCLK       | 0                                                               | —                    | ns      |
| $t_{CH}$                   | DCLK high time                                    | $0.45 \times 1/f_{MAX}$                                         | —                    | s       |
| $t_{CL}$                   | DCLK low time                                     | $0.45 \times 1/f_{MAX}$                                         | —                    | s       |
| $t_{CLK}$                  | DCLK period                                       | $1/f_{MAX}$                                                     | —                    | s       |
| $f_{MAX}$                  | DCLK frequency                                    | —                                                               | 125                  | MHz     |
| $t_{CD2UM}$                | CONF_DONE high to user mode <sup>(3)</sup>        | 175                                                             | 437                  | $\mu$ s |
| $t_{CD2CU}$                | CONF_DONE high to CLKUSR enabled                  | 4 × maximum DCLK period                                         | —                    | —       |
| $t_{CD2UMC}$               | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (8576 \times \text{CLKUSR period})$ <sup>(4)</sup> | —                    | —       |

**Notes to Table 54:**

- (1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section.
- (5) If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

## Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

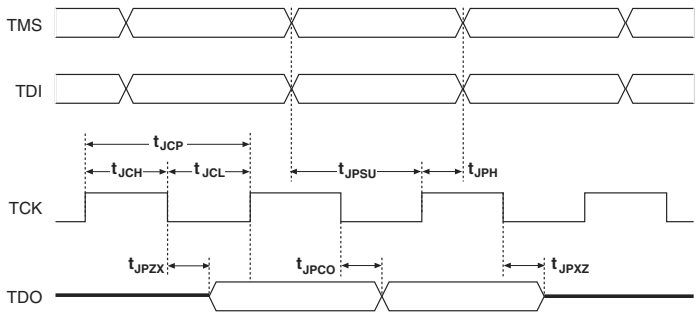
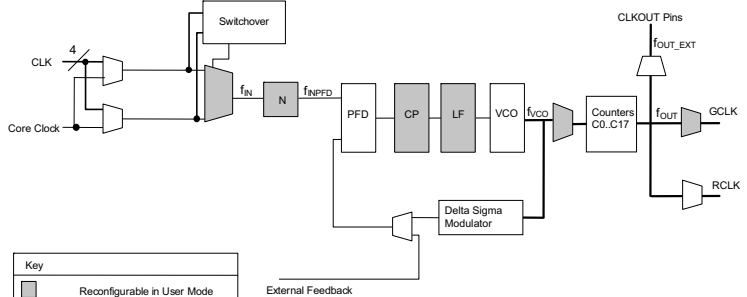
**Table 55. Initialization Clock Source Option and the Maximum Frequency**

| Initialization Clock Source | Configuration Schemes      | Maximum Frequency | Minimum Number of Clock Cycles <sup>(1)</sup> |
|-----------------------------|----------------------------|-------------------|-----------------------------------------------|
| Internal Oscillator         | AS, PS, FPP                | 12.5 MHz          | 8576                                          |
| CLKUSR                      | AS, PS, FPP <sup>(2)</sup> | 125 MHz           |                                               |
| DCLK                        | PS, FPP                    | 125 MHz           |                                               |

**Notes to Table 55:**

- (1) The minimum number of clock cycles required for device initialization.
- (2) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Table 60. Glossary (Part 2 of 4)

| Letter                | Subject                    | Definitions                                                                                                                                                                                                                                          |
|-----------------------|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| G<br>H<br>I           | —                          | —                                                                                                                                                                                                                                                    |
| J                     | JTAG Timing Specifications | <p>High-speed I/O block—Deserialization factor (width of parallel data bus).</p> <p>JTAG Timing Specifications:</p>                                                |
| K<br>L<br>M<br>N<br>O | —                          | —                                                                                                                                                                                                                                                    |
| P                     | PLL Specifications         | <p><b>Diagram of PLL Specifications <sup>(1)</sup></b></p>  <p><b>Note:</b><br/>(1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p> |
| Q                     | —                          | —                                                                                                                                                                                                                                                    |
| R                     | R <sub>L</sub>             | Receiver differential input discrete resistor (external to the Stratix V device).                                                                                                                                                                    |

## Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

| Date          | Version | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| June 2018     | 3.9     | <ul style="list-style-type: none"> <li>Added the “Stratix V Device Overshoot Duration” figure.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| April 2017    | 3.8     | <ul style="list-style-type: none"> <li>Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the “PS Timing Parameters for Stratix V Devices” table.</li> <li>Changed the condition for <math>100\text{-}\Omega</math> <math>R_D</math> in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table.</li> </ul> |
| June 2016     | 3.7     | <ul style="list-style-type: none"> <li>Added the <math>V_{ID}</math> minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table</li> <li>Added the <math>I_{OUT}</math> specification to the “Absolute Maximum Ratings for Stratix V Devices” table.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| December 2015 | 3.6     | <ul style="list-style-type: none"> <li>Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| December 2015 | 3.5     | <ul style="list-style-type: none"> <li>Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| July 2015     | 3.4     | <ul style="list-style-type: none"> <li>Changed the data rate specification for transceiver speed grade 3 in the following tables:               <ul style="list-style-type: none"> <li>“Transceiver Specifications for Stratix V GX and GS Devices”</li> <li>“Stratix V Standard PCS Approximate Maximum Date Rate”</li> <li>“Stratix V 10G PCS Approximate Maximum Data Rate”</li> </ul> </li> <li>Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>Changed the <math>t_{CO}</math> maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table.</li> <li>Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> </ul>                                      |

**Table 61. Document Revision History (Part 3 of 3)**

| Date          | Version | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| May 2013      | 2.7     | <ul style="list-style-type: none"> <li>■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60</li> <li>■ Added Table 24, Table 48</li> <li>■ Updated Figure 9, Figure 10, Figure 11, Figure 12</li> </ul>                                                                                                                                                                                                                                                                                                                               |
| February 2013 | 2.6     | <ul style="list-style-type: none"> <li>■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46</li> <li>■ Updated “Maximum Allowed Overshoot and Undershoot Voltage”</li> </ul>                                                                                                                                                                                                                                                                                                                                               |
| December 2012 | 2.5     | <ul style="list-style-type: none"> <li>■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35</li> <li>■ Added Table 33</li> <li>■ Added “Fast Passive Parallel Configuration Timing”</li> <li>■ Added “Active Serial Configuration Timing”</li> <li>■ Added “Passive Serial Configuration Timing”</li> <li>■ Added “Remote System Upgrades”</li> <li>■ Added “User Watchdog Internal Circuitry Timing Specification”</li> <li>■ Added “Initialization”</li> <li>■ Added “Raw Binary File Size”</li> </ul> |
| June 2012     | 2.4     | <ul style="list-style-type: none"> <li>■ Added Figure 1, Figure 2, and Figure 3.</li> <li>■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.</li> <li>■ Various edits throughout to fix bugs.</li> <li>■ Changed title of document to <i>Stratix V Device Datasheet</i>.</li> <li>■ Removed document from the Stratix V handbook and made it a separate document.</li> </ul>                            |
| February 2012 | 2.3     | <ul style="list-style-type: none"> <li>■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| December 2011 | 2.2     | <ul style="list-style-type: none"> <li>■ Added Table 2–31.</li> <li>■ Updated Table 2–28 and Table 2–34.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| November 2011 | 2.1     | <ul style="list-style-type: none"> <li>■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.</li> <li>■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.</li> <li>■ Various edits throughout to fix SPRs.</li> </ul>                                                                                                                                                                                                                                                                                          |
| May 2011      | 2.0     | <ul style="list-style-type: none"> <li>■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.</li> <li>■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title.</li> <li>■ Chapter moved to Volume 1.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                                                     |
| December 2010 | 1.1     | <ul style="list-style-type: none"> <li>■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.</li> <li>■ Converted chapter to the new template.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                           |
| July 2010     | 1.0     | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

