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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 220000 |
| Number of Logic Elements/Cells | 583000 |
| Total RAM Bits | 46080000 |
| Number of I/O | 696 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-FBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgsmd6k3f40i3ln |

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 5. Maximum Allowed Overshoot During Transitions

| Symbol | Description | Condition (V) | Overshoot Duration as % @ $T_J = 100^\circ\text{C}$ | Unit |
|------------|------------------|---------------|--|------|
| V_i (AC) | AC input voltage | 3.8 | 100 | % |
| | | 3.85 | 64 | % |
| | | 3.9 | 36 | % |
| | | 3.95 | 21 | % |
| | | 4 | 12 | % |
| | | 4.05 | 7 | % |
| | | 4.1 | 4 | % |
| | | 4.15 | 2 | % |
| | | 4.2 | 1 | % |

Figure 1. Stratix V Device Overshoot Duration

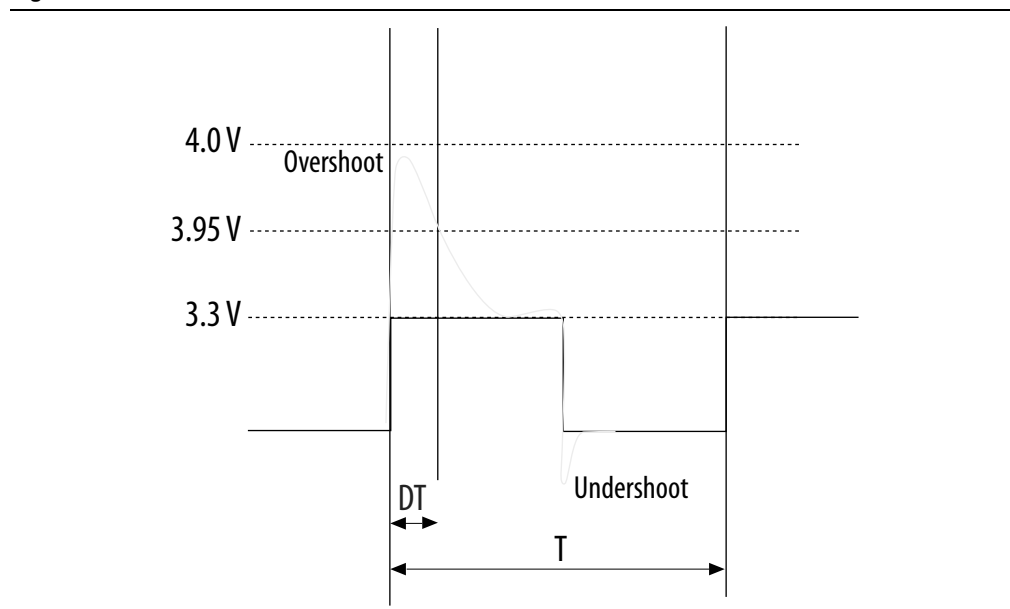


Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)

| Symbol | Description | Devices | Minimum ⁽⁴⁾ | Typical | Maximum ⁽⁴⁾ | Unit |
|------------------------|--|------------|------------------------|---------|------------------------|------|
| V_{CCR_GXBR} (2) | Receiver analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCR_GTBR} | Receiver analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCT_GXBL} (2) | Transmitter analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCT_GXBR} (2) | Transmitter analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCT_GTBR} | Transmitter analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCL_GTBR} | Transmitter clock network power supply | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCH_GXBL} | Transmitter output buffer power supply (left side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |
| V_{CCH_GXBR} | Transmitter output buffer power supply (right side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |

Notes to Table 7:

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9. I/O Pin Leakage Current for Stratix V Devices ⁽¹⁾

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------|--------------------|--|-----|-----|-----|---------------|
| I_I | Input pin | $V_I = 0 \text{ V to } V_{CCIO\text{MAX}}$ | -30 | — | 30 | μA |
| I_{OZ} | Tri-stated I/O pin | $V_O = 0 \text{ V to } V_{CCIO\text{MAX}}$ | -30 | — | 30 | μA |

Note to Table 9:

(1) If $V_O = V_{CCIO}$ to $V_{CCIO\text{MAX}}$, 100 μA of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

| Parameter | Symbol | Conditions | V _{CCIO} | | | | | | | | | | Unit |
|-------------------------|-------------------|--|-------------------|------|-------|------|-------|------|-------|------|-------|------|------|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | I _{SUSL} | V _{IN} > V _{IL} (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | μA |
| High sustaining current | I _{SUSH} | V _{IN} < V _{IH} (minimum) | −22.5 | — | −25.0 | — | −30.0 | — | −50.0 | — | −70.0 | — | μA |
| Low overdrive current | I _{ODL} | 0V < V _{IN} < V _{CCIO} | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | μA |
| High overdrive current | I _{ODH} | 0V < V _{IN} < V _{CCIO} | — | −120 | — | −160 | — | −200 | — | −300 | — | −500 | μA |
| Bus-hold trip point | V _{TRIP} | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|--------------------|---|---|----------------------|----------|----------------|----------|------|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 25- Ω R_S | Internal series termination with calibration (25- Ω setting) | $V_{\text{CCIO}} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$ | ± 15 | ± 15 | ± 15 | ± 15 | % |

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|----------------------|--|-----------------------------------|----------------------|--------|--------------|--------|------|
| | | | C1 | C2, I2 | C3, I3, I3YY | C4, I4 | |
| 50-Ω R _S | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 50-Ω R _S | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |
| 100-Ω R _D | Internal differential termination (100-Ω setting) | V _{CCPD} = 2.5 V | ±25 | ±25 | ±25 | ±25 | % |

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration for Stratix V Devices ^{(1), (2), (3), (4), (5), (6)}

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

Notes to Equation 1:

- (1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- (2) R_{SCAL} is the OCT resistance value at power-up.
- (3) ΔT is the variation of temperature with respect to the temperature at power-up.
- (4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
- (5) dR/dT is the percentage change of R_{SCAL} with temperature.
- (6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2) ⁽¹⁾

| Symbol | Description | V _{CCIO} (V) | Typical | Unit |
|--------|--|-----------------------|---------|------|
| dR/dV | OCT variation with voltage without recalibration | 3.0 | 0.0297 | %/mV |
| | | 2.5 | 0.0344 | |
| | | 1.8 | 0.0499 | |
| | | 1.5 | 0.0744 | |
| | | 1.2 | 0.1241 | |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 2 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|----------------------------------|-------------------|------|----------------------------------|-------------------|------|----------------------------------|-----------------------|------|-------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Spread-spectrum downspread | PCIe | — | 0 to -0.5 | — | — | 0 to -0.5 | — | — | 0 to -0.5 | — | % |
| On-chip termination resistors ⁽²¹⁾ | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Absolute V_{MAX} ⁽⁵⁾ | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | |
| Absolute V_{MIN} | — | -0.4 | — | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | 200 | — | 1600 | mV |
| V_{ICM} (AC coupled) ⁽³⁾ | Dedicated reference clock pin | 1050/1000/900/850 ⁽²⁾ | | | 1050/1000/900/850 ⁽²⁾ | | | 1050/1000/900/850 ⁽²⁾ | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 ⁽⁴⁾ | | | 1.0/0.9/0.85 ⁽⁴⁾ | | | 1.0/0.9/0.85 ⁽⁴⁾ | | | V |
| V_{ICM} (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise (622 MHz) ⁽²⁰⁾ | 100 Hz | — | — | -70 | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | — | — | -90 | dBc/Hz |
| | 10 kHz | — | — | -100 | — | — | -100 | — | — | -100 | dBc/Hz |
| | 100 kHz | — | — | -110 | — | — | -110 | — | — | -110 | dBc/Hz |
| | ≥ 1 MHz | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁷⁾ | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | — | — | 3 | ps (rms) |
| R_{REF} ⁽¹⁹⁾ | — | — | 1800 $\pm 1\%$ | — | — | 1800 $\pm 1\%$ | — | — | 180 0 $\pm 1\%$ | — | Ω |
| Transceiver Clocks | | | | | | | | | | | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | — | 100 or 125 | — | MHz |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 7 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{pll_lock}^{(16)}$ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |

Notes to Table 23:

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows V_{CCR_GXB} .
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.
- (13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.
- (16) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz \times 100/f.
- (18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (19) For ES devices, R_{REF} is $2000 \Omega \pm 1\%$.
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + $20 \times \log(f/622)$.
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100Ω . The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate ⁽¹⁾, ⁽³⁾

| Mode ⁽²⁾ | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---------------------|-------------------------|---------------------------------------|---------|---------|---------|---------|-----|-----|------|------|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| FIFO | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 | 8.5 | 8.5 | 8.5 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.8 | 4.2 | 3.84 | 3.44 |
| Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

Notes to Table 25:

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|--|---------------|--------|------------------------------|---------------|--------|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁸⁾ | 100 Hz | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | |
| | 10 kHz | — | — | -100 | — | — | -100 | |
| | 100 kHz | — | — | -110 | — | — | -110 | |
| | ≥ 1 MHz | — | — | -120 | — | — | -120 | |
| Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾ | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | ps (rms) |
| RREF ⁽¹⁷⁾ | — | — | 1800 ± 1% | — | — | 1800 ± 1% | — | Ω |
| Transceiver Clocks | | | | | | | | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | MHz |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | MHz |
| Receiver | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Data rate (Standard PCS) ⁽²¹⁾ | GX channels | 600 | — | 8500 | 600 | — | 8500 | Mbps |
| Data rate (10G PCS) ⁽²¹⁾ | GX channels | 600 | — | 12,500 | 600 | — | 12,500 | Mbps |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Absolute V _{MAX} for a receiver pin ⁽³⁾ | GT channels | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V _{MIN} for a receiver pin | GT channels | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾ | GT channels | — | — | 1.6 | — | — | 1.6 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration ⁽¹⁶⁾ , ⁽²⁰⁾ | GT channels V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V) | — | — | 2.2 | — | — | 2.2 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Minimum differential eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾ | GT channels | 200 | — | — | 200 | — | — | mV |
| | GX channels | ⁽⁸⁾ | | | | | | |

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices ⁽¹⁾

| Symbol | Performance | | | Unit |
|---------------------------|--------------------------|-----------------------|--------|------|
| | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 | |
| Global and Regional Clock | 717 | 650 | 580 | MHz |
| Periphery Clock | 550 | 500 | 500 | MHz |

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|------------|--|----------------|--------|-------------|---------|-----|-----|---------|---------------|-----|------|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| M20K Block | Single-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | Simple dual-port with the read-during-write option set to Old Data , all supported widths | 0 | 1 | 525 | 525 | 455 | 400 | 525 | 455 | 400 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 0 | 1 | 450 | 450 | 400 | 350 | 450 | 400 | 350 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |
| | True dual port, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |
| | ROM, all supported widths | 0 | 1 | 700 | 700 | 650 | 550 | 700 | 500 | 450 | MHz |

Notes to Table 33:

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX} .
- (3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time | Resolution | Minimum Resolution with no Missing Codes |
|-------------------|----------|--------------------------|----------------|-----------------|------------|--|
| –40°C to 100°C | ±8°C | No | 1 MHz, 500 KHz | < 100 ms | 8 bits | 8 bits |

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

| Description | Min | Typ | Max | Unit |
|-----------------------------------|-------|-------|-------|------|
| I_{bias} , diode source current | 8 | — | 200 | μA |
| V_{bias} , voltage across diode | 0.3 | — | 0.9 | V |
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface.

General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.



The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices ⁽¹⁾, ⁽²⁾ (Part 1 of 4)

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|--|--|-----|-----|-----|------------------|-----|-----|-------------------|-----|--------------------|-------|-----|--------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{\text{HCLK_in}}$ (input clock frequency) True Differential I/O Standards | Clock boost factor $W = 1$ to 40 ⁽⁴⁾ | 5 | — | 800 | 5 | — | 800 | 5 | — | 625 | 5 | — | 525 | MHz |
| $f_{\text{HCLK_in}}$ (input clock frequency) Single Ended I/O Standards ⁽³⁾ | Clock boost factor $W = 1$ to 40 ⁽⁴⁾ | 5 | — | 800 | 5 | — | 800 | 5 | — | 625 | 5 | — | 525 | MHz |
| $f_{\text{HCLK_in}}$ (input clock frequency) Single Ended I/O Standards | Clock boost factor $W = 1$ to 40 ⁽⁴⁾ | 5 | — | 520 | 5 | — | 520 | 5 | — | 420 | 5 | — | 420 | MHz |
| $f_{\text{HCLK_OUT}}$ (output clock frequency) | — | 5 | — | 800 | 5 | — | 800 | 5 | — | 625 ⁽⁵⁾ | 5 | — | 525 ⁽⁵⁾ | MHz |

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

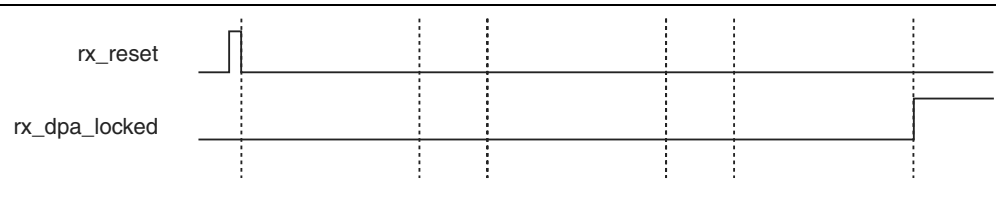


Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only ^{(1), (2), (3)}

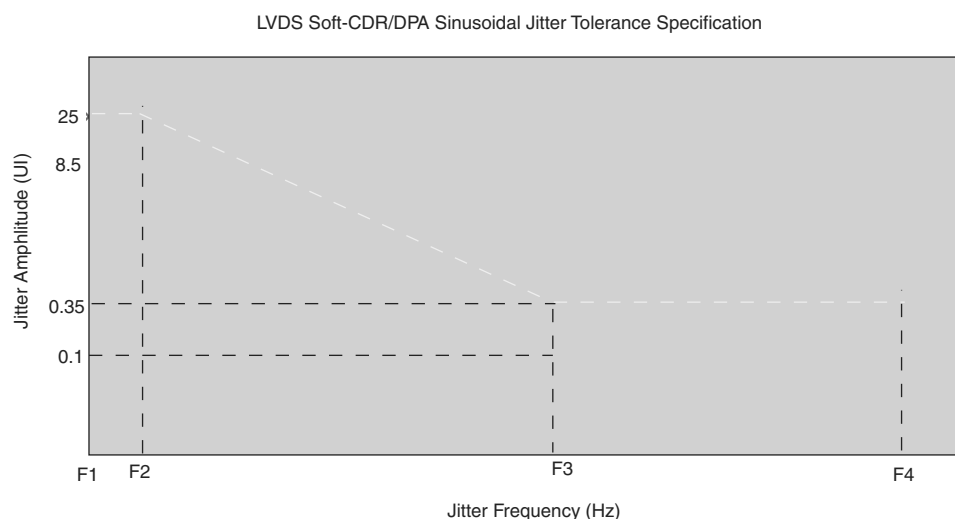
| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions ⁽⁴⁾ | Maximum |
|--------------------|----------------------|--|---|----------------------|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

Notes to Table 37:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps



Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins ⁽¹⁾

| Symbol | C1 | | C2, C2L, I2, I2L | | C3, I3, I3L, I3YY | | C4, I4 | | Unit |
|-------------------|-----|-----|------------------|-----|-------------------|-----|--------|-----|------|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification ⁽¹⁾

| POR Delay | Minimum | Maximum |
|-----------|---------|---------|
| Fast | 4 ms | 12 ms |
| Standard | 100 ms | 300 ms |

Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

| Symbol | Description | Min | Max | Unit |
|-------------------------|------------------------------------|-----|-----|------|
| t _{JCP} | TCK clock period ⁽²⁾ | 30 | — | ns |
| t _{JCP} | TCK clock period ⁽²⁾ | 167 | — | ns |
| t _{JCH} | TCK clock high time ⁽²⁾ | 14 | — | ns |
| t _{JCL} | TCK clock low time ⁽²⁾ | 14 | — | ns |
| t _{JPSU (TDI)} | TDI JTAG port setup time | 2 | — | ns |
| t _{JPSU (TMS)} | TMS JTAG port setup time | 3 | — | ns |

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) ^{(4), (5)} |
|----------------------------|--------|---------|--------------------------------|--|
| Stratix V E ⁽¹⁾ | 5SEE9 | — | 342,742,976 | 700,888 |
| | 5SEEB | — | 342,742,976 | 700,888 |

Notes to Table 47:

- (1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
- (2) 36-transceiver devices.
- (3) 24-transceiver devices.
- (4) File size for the periphery image.
- (5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.tff) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.



For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

| Variant | Member Code | Active Serial ⁽¹⁾ | | | Fast Passive Parallel ⁽²⁾ | | |
|---------|-------------|------------------------------|------------|---------------------|--------------------------------------|------------|---------------------|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GX | A3 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | A4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | A5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | AB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | B5 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B6 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | BB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| GT | C5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | C7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

| Variant | Member Code | Active Serial ⁽¹⁾ | | | Fast Passive Parallel ⁽²⁾ | | |
|---------|-------------|------------------------------|------------|---------------------|--------------------------------------|------------|---------------------|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GS | D3 | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | D5 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | D6 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| | D8 | 4 | 100 | 0.741 | 32 | 100 | 0.093 |
| E | E9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | EB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA [] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA [] ratio for each combination.

Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 1 of 2)

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|----------------------|---------------|-----------------|----------------------|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices ⁽¹⁾

| Symbol | Parameter | Minimum | Maximum | Units |
|-----------------------------------|---|--|----------------------|-------|
| t _{CF2CD} | nCONFIG low to CONF_DONE low | — | 600 | ns |
| t _{CF2ST0} | nCONFIG low to nSTATUS low | — | 600 | ns |
| t _{CFG} | nCONFIG low pulse width | 2 | — | μs |
| t _{STATUS} | nSTATUS low pulse width | 268 | 1,506 ⁽²⁾ | μs |
| t _{CF2ST1} | nCONFIG high to nSTATUS high | — | 1,506 ⁽³⁾ | μs |
| t _{CF2CK} ⁽⁶⁾ | nCONFIG high to first rising edge on DCLK | 1,506 | — | μs |
| t _{ST2CK} ⁽⁶⁾ | nSTATUS high to first rising edge of DCLK | 2 | — | μs |
| t _{DSU} | DATA [] setup time before rising edge on DCLK | 5.5 | — | ns |
| t _{DH} | DATA [] hold time after rising edge on DCLK | 0 | — | ns |
| t _{CH} | DCLK high time | $0.45 \times 1/f_{\text{MAX}}$ | — | s |
| t _{CL} | DCLK low time | $0.45 \times 1/f_{\text{MAX}}$ | — | s |
| t _{CLK} | DCLK period | $1/f_{\text{MAX}}$ | — | s |
| f _{MAX} | DCLK frequency (FPP $\times 8/\times 16$) | — | 125 | MHz |
| | DCLK frequency (FPP $\times 32$) | — | 100 | MHz |
| t _{CD2UM} | CONF_DONE high to user mode ⁽⁴⁾ | 175 | 437 | μs |
| t _{CD2CU} | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| t _{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | t _{CD2CU} + (8576 × CLKUSR period) ⁽⁵⁾ | — | — |

Notes to Table 50:

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model | | Slow Model | | | | | | | |
|------------------|-----------------------|----------------------|------------|------------|------------|-------|-------|-------|-------|-------------|-------|------|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.793 | 2.793 | 2.992 | 3.192 | 2.811 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.838 | 0.838 | 0.924 | 1.011 | 0.843 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.415 | 0.415 | 0.458 | 0.503 | 0.418 | 0.456 | 0.499 | ns |

Notes to Table 58:

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.
- (2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)

| Symbol | Parameter | Typical | Unit |
|---------------------|----------------------------------|-------------|------|
| D _{OUTBUF} | Rising and/or falling edge delay | 0 (default) | ps |
| | | 25 | ps |
| | | 50 | ps |
| | | 75 | ps |

Note to Table 59:

- (1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

| Letter | Subject | Definitions |
|--------|----------------------|---|
| A | — | — |
| B | | |
| C | | |
| D | — | — |
| E | — | — |
| F | f _{HCLK} | Left and right PLL input clock frequency. |
| | f _{HSDR} | High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA. |
| | f _{HSDRDPA} | High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA. |

Table 60. Glossary (Part 3 of 4)

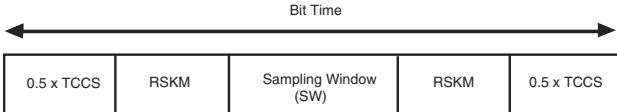
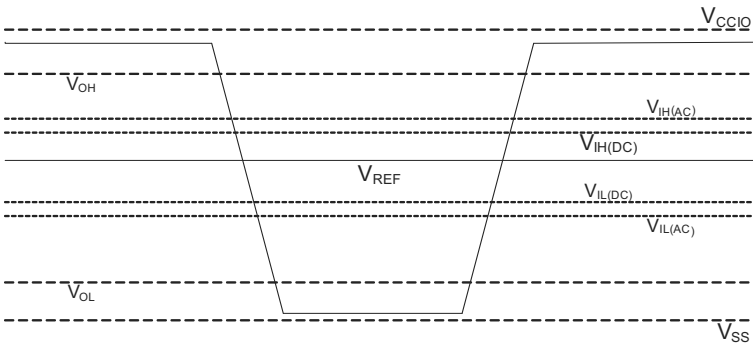
| Letter | Subject | Definitions |
|--------|--|--|
| S | SW (sampling window) | <p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p>  |
| | Single-ended voltage referenced I/O standard | <p>The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p>  |
| T | t_c | High-speed receiver and transmitter input and output clock period. |
| | TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under SW in this table). |
| | t_{DUTY} | <p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p>Timing Unit Interval (TUI)</p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_c/w$)</p> |
| | t_{FALL} | Signal high-to-low transition time (80-20%) |
| | t_{INCCJ} | Cycle-to-cycle jitter tolerance on the PLL clock input. |
| | t_{OUTPJ_IO} | Period jitter on the general purpose I/O driven by a PLL. |
| | t_{OUTPJ_DC} | Period jitter on the dedicated clock output driven by a PLL. |
| | t_{RISE} | Signal low-to-high transition time (20-80%) |
| U | — | — |

Table 60. Glossary (Part 4 of 4)

| Letter | Subject | Definitions |
|----------|---------------|--|
| V | $V_{CM(DC)}$ | DC common mode input voltage. |
| | V_{ICM} | Input common mode voltage—The common mode of the differential signal at the receiver. |
| | V_{ID} | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| | V_{IH} | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage |
| | $V_{IH(DC)}$ | High-level DC input voltage |
| | V_{IL} | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage |
| | $V_{IL(DC)}$ | Low-level DC input voltage |
| | V_{OCM} | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| | V_{OD} | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| | V_{SWING} | Differential input voltage |
| | V_X | Input differential cross point voltage |
| | V_{OX} | Output differential cross point voltage |
| W | W | High-speed I/O block—clock boost factor |
| X | — | — |
| Y | | |
| Z | | |

