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# Intel - 5SGSMD6N1F45I2N Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	220000
Number of Logic Elements/Cells	583000
Total RAM Bits	46080000
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgsmd6n1f45i2n

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			<b>Resistance Tolerance</b>						
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit		
50-Ω R <sub>S</sub>	Internal series termination without calibration (50- $\Omega$ setting)	$V_{CCIO} = 1.8$ and 1.5 V	±30	±30	±40	±40	%		
50-Ω R <sub>S</sub>	Internal series termination without calibration (50- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	±35	±35	±50	±50	%		
100-Ω R <sub>D</sub>	Internal differential termination (100- $\Omega$ setting)	V <sub>CCPD</sub> = 2.5 V	±25	±25	±25	±25	%		

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

# Equation 1. OCT Variation Without Recalibration for Stratix V Devices (1), (2), (3), (4), (5), (6)

$$R_{OCT} \,=\, R_{SCAL} \Big( 1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle \Big) \label{eq:ROCT}$$

#### Notes to Equation 1:

- (1) The  $R_{OCT}$  value shows the range of OCT resistance with the variation of temperature and  $V_{CCIO}$ .
- (2) R<sub>SCAL</sub> is the OCT resistance value at power-up.
- (3)  $\Delta T$  is the variation of temperature with respect to the temperature at power-up.
- (4)  $\Delta V$  is the variation of voltage with respect to the V<sub>CCIO</sub> at power-up.
- (5) dR/dT is the percentage change of  $R_{\text{SCAL}}$  with temperature.
- (6) dR/dV is the percentage change of  $\mathsf{R}_{\mathsf{SCAL}}$  with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2)
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Symbol	Description	V <sub>CCIO</sub> (V)	Typical	Unit
dR/dV		3.0	0.0297	
	OCT variation with voltage without	2.5	0.0344	
		1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	

## **Internal Weak Pull-Up Resistor**

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Symbol	Description	V <sub>CCIO</sub> Conditions (V) <sup>(3)</sup>	Value <sup>(4)</sup>	Unit
		3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ
R <sub>PU</sub>	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ
	pull-up resistor option.	1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k $\Omega$ .

- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V<sub>CCIO</sub>.
- (4) These specifications are valid with a  $\pm 10\%$  tolerance to cover changes over PVT.

# I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V<sub>IH</sub> and V<sub>IL</sub>), output voltage (V<sub>OH</sub> and V<sub>OL</sub>), and current drive characteristics (I<sub>OH</sub> and I<sub>OL</sub>) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V<sub>OL</sub> and V<sub>OH</sub> values are valid at the corresponding I<sub>OH</sub> and I<sub>OL</sub>, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012\_486.

I/O	V <sub>CCIO</sub> (V)			V <sub>IL</sub> (V)		VIH	(V)	V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	I <sub>OL</sub>	I <sub>oh</sub>
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V <sub>CCIO</sub>	0.65 * V <sub>CCIO</sub>	V <sub>CCI0</sub> + 0.3	0.45	V <sub>CCI0</sub> – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	-2

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard	V <sub>IL(DC)</sub> (V)		V <sub>IH(D</sub>	<sub>C)</sub> (V)	V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>ol</sub> (V)	V <sub>oh</sub> (V)	I (mA)	l <sub>oh</sub>
i/U Stanuaru	Min Max		Min Max		Max	Min	Max	Min	i <sub>ol</sub> (IIIA)	(mA)
HSTL-18 Class I	—	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	$V_{REF} - 0.2$	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	8	-8
HSTL-18 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	8	-8
HSTL-15 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	16	-16
HSUL-12	—	V <sub>REF</sub> – 0.13	V <sub>REF</sub> + 0.13	_	V <sub>REF</sub> – 0.22	V <sub>REF</sub> + 0.22	0.1* V <sub>CCIO</sub>	0.9* V <sub>CCI0</sub>	_	

## Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard	V <sub>CCIO</sub> (V)			V <sub>SWIN</sub>	V <sub>SWING(DC)</sub> (V)		V <sub>X(AC)</sub> (V)		V <sub>SWING(AC)</sub> (V)		
ijo Stanuaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V <sub>CCI0</sub> + 0.6	V <sub>CCI0</sub> /2- 0.2	_	V <sub>CCI0</sub> /2 + 0.2	0.62	V <sub>CCI0</sub> + 0.6	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V <sub>CCIO</sub> + 0.6	V <sub>CCI0</sub> /2- 0.175	_	V <sub>CCI0</sub> /2 + 0.175	0.5	V <sub>CCI0</sub> + 0.6	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	_	V <sub>CCI0</sub> /2 + 0.15	0.35	_	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCI0</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>IL(AC)</sub> - V <sub>REF</sub> )	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCI0</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V <sub>REF</sub> 0.15	V <sub>CCI0</sub> /2	V <sub>REF</sub> + 0.15	-0.30	0.30	

Note to Table 20:

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits  $(V_{IH(DC)} \text{ and } V_{IL(DC)})$ .

							. ,							
I/O	V <sub>CCIO</sub> (V)			V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)				V <sub>CM(DC)</sub> (V	V <sub>DIF(AC)</sub> (V)			
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max	
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_	
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_	

# **Switching Characteristics**

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

# **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Transceiver Speed Grade 2			Trai	er Speed e 3	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
Reference Clock												
Supported I/O	Dedicated reference clock pin	Dedicated reference clock pin 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL										
Standards	RX reference clock pin		1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	_	40	_	710	40	_	710	40	_	710	MHz	
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>		100		710	100		710	100		710	MHz	
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>			400	_		400			400	ns	
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>		_	400	_		400			400	ps	
Duty cycle		45		55	45		55	45	—	55	%	
Spread-spectrum modulating clock frequency	PCI Express® (PCIe <sup>®</sup> )	30		33	30		33	30	_	33	kHz	

Symbol/	Conditions	Conditions Transceiver Speed Grade 1		Trai	Transceiver Speed Grade 2			Transceiver Speed Grade 3			
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Spread-spectrum downspread	PCIe	_	0 to 0.5	_	_	0 to 0.5	_	_	0 to 0.5	_	%
On-chip termination resistors <sup>(21)</sup>	_	_	100		_	100		_	100		Ω
Absolute V <sub>MAX</sub> <sup>(5)</sup>	Dedicated reference clock pin	_	_	1.6	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_		1.2		_	1.2			1.2	
Absolute V <sub>MIN</sub>	—	-0.4	-	_	-0.4	-		-0.4	—		V
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	200	_	1600	mV
V <sub>ICM</sub> (AC	Dedicated reference clock pin	1050/1000/900/850 <sup>(2)</sup> 1.0/0.9/0.85 <sup>(4)</sup>		1050/1000/900/850 <sup>(2)</sup>			1050/1000/900/850 <sup>(2)</sup>			mV	
coupled) (9	RX reference clock pin			1.0/0.9/0.85 (4)			1.0/0.9/0.85 (4)			V	
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250		550	250		550	250	_	550	mV
	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
Transmitter	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
REFCLK Phase	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
(622 MHz) <sup>(20)</sup>	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120		—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(17)</sup>	10 kHz to 1.5 MHz (PCIe)	_	_	3	_	_	3	_	_	3	ps (rms)
R <sub>REF</sub> (19)	_	_	1800 ±1%	_	_	1800 ±1%	_	_	180 0 ±1%	_	Ω
Transceiver Clock	s										
fixedclk <b>clock</b> frequency	PCIe Receiver Detect		100 or 125			100 or 125		_	100 or 125		MHz

# Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

		ATX PLL			CMU PLL <sup>(2)</sup>	)		fPLL	
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 <sup>(3)</sup>	14.1	_	6	12.5	_	6	3.125	—	3
x6 <sup>(3)</sup>	_	14.1	6	—	12.5	6	—	3.125	6
x6 PLL Feedback <sup>(4)</sup>	_	14.1	Side- wide	_	12.5	Side- wide	_	_	_
xN (PCIe)	_	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7 00	7.99 7.99	Up to 13 channels above and below PLL	3.125	3 125	Up to 13 channels above
	_	8.01 to 9.8304	Up to 7 channels above and below PLL	7.99				0.120	and below PLL

Notes to Table 24:

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 26 shows the approximate maximum data rate using the 10G PCS.

Mada (2)	Transceiver	PMA Width	64	40	40	40	32	32		
Speed Grade		PCS Width	64	66/67	50	40	64/66/67	32		
	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6		
	0	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5		
2	Z	C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88		
FIFO or Register	0	C1, C2, C2L, I2, I2L core speed grade								
		C3, I3, I3L core speed grade	8.5 Gbps							
	5	C4, I4 core speed grade								
		I3YY core speed grade	10.3125 Gbps							

Notes to Table 26:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Symbol/	Conditions	Transceiver Speed Grade 2			S	Unit		
Description		Min	Тур	Max	Min	Тур	Max	
Reference Clock								1
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	IL, 1.4-V PC	ML, 1.5-V P(	CML, 2.5-V I and HCSL	PCML, Diffe	rential LVPE	ECL, LVDS,
otanuarus	RX reference clock pin		1.4-V PCML	., 1.5-V PCM	IL, 2.5-V PC	ML, LVPEC	L, and LVDS	6
Input Reference Clock Frequency (CMU PLL) <sup>(6)</sup>	_	40	_	710	40	_	710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(6)</sup>	_	100	_	710	100	_	710	MHz
Rise time	20% to 80%	_		400	_	_	400	
Fall time	80% to 20%			400	—	_	400	ps
Duty cycle	—	45	_	55	45	_	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%
On-chip termination resistors <sup>(19)</sup>	_	_	100	_	_	100	_	Ω
Absolute V <sub>MAX</sub> <sup>(3)</sup>	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_	_	1.2	_	_	1.2	
Absolute V <sub>MIN</sub>	—	-0.4		—	-0.4	_		V
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV
V <sub>ICM</sub> (AC coupled)	Dedicated reference clock pin		1050/1000 <sup>(,</sup>	2)	1050/1000 <sup>(2)</sup>			mV
	RX reference clock pin	1	.0/0.9/0.85 (	22)	1.0/0.9/0.85 (22)			V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250		550	mV

## Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)<sup>(1)</sup>

Table 29 shows the  $V_{\text{OD}}$  settings for the GT channel.

Symbol	V <sub>OD</sub> Setting	V <sub>od</sub> Value (mV)
	0	0
	1	200
V., differential neak to neak typical $(1)$	2	400
The fine contrar hear to hear the field to	3	600
	4	800
	5	1000

## Note:

(1) Refer to Figure 4.

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

# **Core Performance Specifications**

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

# **Clock Tree Specifications**

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

	Performance							
Symbol	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	Unit				
Global and Regional Clock	717	650	580	MHz				
Periphery Clock	550	500	500	MHz				

## Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Symbol	Parameter		Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ( $f_{REF} \ge 100 \text{ MHz}$ )			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f <sub>REF</sub> < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} $\geq$ 100 MHz)	_	_	175 <sup>(1)</sup>	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f <sub>OUT</sub> < 100 MHz)	_	_	17.5 <sup>(1)</sup>	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} < 100 \text{ MHz}$ )+		_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
t <sub>outpj 10</sub> (5),	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t <sub>foutpj 10</sub> <sup>(5),</sup>	Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>outccj_io</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>FOUTCCJ 10</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100$ MHz)		_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>CASC OUTPJ DC</sub>	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT}$ < 100 MHz)	_	_	17.5	mUI (p-p)
f <sub>DRIFT</sub>	Frequency drift after PFDENA is disabled for a duration of 100 $\mu s$		_	±10	%
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k <sub>VALUE</sub>	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
wiscellaneous	01010101	8	32	640 data transitions

#### Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps.





Jitter Free	Sinusoidal Jitter (UI)	
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

iadie 38. lvus sott-luk/upa sinusoidai jitter mask vaiues tor a uata kate > 1.2	25 G	.2	1.	1	>	>		Ì	e	F	Ł	đ	a	2	1	R	P							Ľ	I.		I.	Ì	1	3	a	3	a	2	2	2	ŀ	t	t	t	ſ	ľ	3	2	2	2	2	2	1	)	D		I		Ľ	1	2	2	ź	â	i		۴	۴	r	r		I	I	Ì	1	Π	٥	٢	i	F	f	f	1	1		5	S	S	S	2	2	e	E	I	U	h	I	١	a	ŀ	I	V	۱			ľ	٢	k	k	s	S	S	1	a	2	2		И	V	N			•	۴	r	r	1	1	1	2	2	2	2	e	e	e	E	t	t	i	ŀ	t	ľ	i	i	f	f	ŀ	ŀ	li
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Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.





# **DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications**

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

#### Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

# **Duty Cycle Distortion (DCD) Specifications**

Table 44 lists the worst-case DCD for Stratix V devices.

## Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C	1	C2, C2	L, 12, 12L	C3, I I3	3, I3L, IYY	C4	4,14	Unit
-	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

## Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

# **Configuration Specification**

# **POR Delay Specification**

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

#### Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

## Note to Table 45:

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

# **JTAG Configuration Specifications**

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	30		ns
t <sub>JCP</sub>	TCK clock period <sup>(2)</sup>	167	—	ns
t <sub>JCH</sub>	TCK clock high time <sup>(2)</sup>	14	—	ns
t <sub>JCL</sub>	TCK clock low time <sup>(2)</sup>	14		ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	2	—	ns
t <sub>JPSU (TMS)</sub>	TMS JTAG port setup time	3	_	ns

	Mombor		Active Serial <sup>(1)</sup>	)	Fast	t Passive Parall	el <sup>(2)</sup>
Variant	Code	Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
	D3	4	100	0.344	32	100	0.043
	D4	4	100	0.534	32	100	0.067
68	D4	4	100	0.344	32	100	0.043
03	D5	4	100	0.534	32	100	0.067
	D6	4	100	0.741	32	100	0.093
	D8	4	100	0.741	32	100	0.093
F	E9	4	100	0.857	32	100	0.107
Ľ	EB	4	100	0.857	32	100	0.107

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

#### Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

# **Fast Passive Parallel Configuration Timing**

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

# DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[]ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA[]ratio for each combination.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	1
111 ×0	Enabled	Disabled	2
	Enabled	Enabled	2
	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

 Table 49. DCLK-to-DATA[] Ratio <sup>(1)</sup> (Part 1 of 2)

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	4
IFF XJZ	Enabled	Disabled	8
	Enabled	Enabled	8

Table 49.	DCLK-to-DATA[]	Ratio <sup>(1)</sup>	(Part 2 of 2)
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Note to Table 49:

(1) Depending on the DCLK-to-DATA [] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA [] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

## Figure 11. Single Device FPP Configuration Using an External Host



#### Notes to Figure 11:

- (1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device.  $V_{CCPGM}$  must be high enough to meet the  $V_{IH}$  specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with  $V_{CCPGM}$ .
- (2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.
- (3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (4) If you use FPP ×8, use DATA [7..0]. If you use FPP ×16, use DATA [15..0].

IF the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Table 60.	Glossary	(Part 3 of 4)
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Letter	Subject	Definitions
	SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:         Bit Time         0.5 x TCCS       RSKM         Sampling Window       RSKM         0.5 x TCCS       RSKM
S	Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values.         The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.         The new logic state is then maintained as long as the input stays beyond the DC threshold.         This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:         Single-Ended Voltage Referenced I/O Standard
	t <sub>C</sub>	High-speed receiver and transmitter input and output clock period.
	TCCS (channel- to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).
		High-speed I/O block—Duty cycle on the high-speed transmitter output clock.
т	t <sub>DUTY</sub>	<b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and the data sampling window.
		$(TUI = 1/(receiver input clock frequency multiplication factor) = t_C/w)$
	t <sub>FALL</sub>	Signal high-to-low transition time (80-20%)
	t <sub>INCCJ</sub>	Cycle-to-cycle jitter tolerance on the PLL clock input.
	t <sub>outpj_i0</sub>	Period jitter on the general purpose I/O driven by a PLL.
	t <sub>outpj_dc</sub>	Period jitter on the dedicated clock output driven by a PLL.
	t <sub>RISE</sub>	Signal low-to-high transition time (20-80%)
U	—	—

# **Document Revision History**

Table 61 lists the revision history for this chapter.

 Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes
June 2018	3.9	<ul> <li>Added the "Stratix V Device Overshoot Duration" figure.</li> </ul>
April 2017	3.8	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "PS Timing Parameters for Stratix V Devices" table.</li> </ul>
		<ul> <li>Changed the condition for 100-Ω R<sub>D</sub> in the "OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices" table.</li> </ul>
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table</li> </ul>
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>
		<ul> <li>Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency" table.</li> </ul>
June 2016	3.7	<ul> <li>Added the V<sub>ID</sub> minimum specification for LVPECL in the "Differential I/O Standard Specifications for Stratix V Devices" table</li> </ul>
		<ul> <li>Added the I<sub>OUT</sub> specification to the "Absolute Maximum Ratings for Stratix V Devices" table.</li> </ul>
December 2015	3.6	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.
December 2015	3.5	<ul> <li>Changed the transmitter, receiver, and ATX PLL data rate specifications in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>
		<ul> <li>Changed the configuration .rbf sizes in the "Uncompressed .rbf Sizes for Stratix V Devices" table.</li> </ul>
	3.4	• Changed the data rate specification for transceiver speed grade 3 in the following tables:
July 2015		<ul> <li>"Transceiver Specifications for Stratix V GX and GS Devices"</li> </ul>
		<ul> <li>"Stratix V Standard PCS Approximate Maximum Date Rate"</li> </ul>
		<ul> <li>"Stratix V 10G PCS Approximate Maximum Data Rate"</li> </ul>
		<ul> <li>Changed the conditions for reference clock rise and fall time, and added a note to the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>
		<ul> <li>Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>
		<ul> <li>Changed the t<sub>c0</sub> maximum value in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table.</li> </ul>
		<ul> <li>Removed the CDR ppm tolerance specification from the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>

# Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes
November 2014		<ul> <li>Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.</li> </ul>
		<ul> <li>Added the I3YY speed grade to the V<sub>CC</sub> description in Table 6.</li> </ul>
	3.3	<ul> <li>Added the I3YY speed grade to V<sub>CCHIP_L</sub>, V<sub>CCHIP_R</sub>, V<sub>CCHSSI_L</sub>, and V<sub>CCHSSI_R</sub> descriptions in Table 7.</li> </ul>
		■ Added 240-Ω to Table 11.
		Changed CDR PPM tolerance in Table 23.
		<ul> <li>Added additional max data rate for fPLL in Table 23.</li> </ul>
		<ul> <li>Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.</li> </ul>
		<ul> <li>Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.</li> </ul>
		<ul> <li>Changed CDR PPM tolerance in Table 28.</li> </ul>
		<ul> <li>Added additional max data rate for fPLL in Table 28.</li> </ul>
		<ul> <li>Changed the mode descriptions for MLAB and M20K in Table 33.</li> </ul>
		<ul> <li>Changed the Max value of f<sub>HSCLK_OUT</sub> for the C2, C2L, I2, I2L speed grades in Table 36.</li> </ul>
		<ul> <li>Changed the frequency ranges for C1 and C2 in Table 39.</li> </ul>
		<ul> <li>Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.</li> </ul>
		<ul> <li>Added note about nSTATUS to Table 50, Table 51, Table 54.</li> </ul>
		<ul> <li>Changed the available settings in Table 58.</li> </ul>
		<ul> <li>Changed the note in "Periphery Performance".</li> </ul>
		<ul> <li>Updated the "I/O Standard Specifications" section.</li> </ul>
		<ul> <li>Updated the "Raw Binary File Size" section.</li> </ul>
		<ul> <li>Updated the receiver voltage input range in Table 22.</li> </ul>
		<ul> <li>Updated the max frequency for the LVDS clock network in Table 36.</li> </ul>
		■ Updated the DCLK note to Figure 11.
		<ul> <li>Updated Table 23 VO<sub>CM</sub> (DC Coupled) condition.</li> </ul>
		Updated Table 6 and Table 7.
		<ul> <li>Added the DCLK specification to Table 55.</li> </ul>
		Updated the notes for Table 47.
		<ul> <li>Updated the list of parameters for Table 56.</li> </ul>
November 2013	3.2	Updated Table 28
November 2013	3.1	Updated Table 33
November 2013	3.0	Updated Table 23 and Table 28
October 2013	2.9	<ul> <li>Updated the "Transceiver Characterization" section</li> </ul>
October 2013	2.8	<ul> <li>Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59</li> </ul>
		<ul> <li>Added Figure 1 and Figure 3</li> </ul>
		<ul> <li>Added the "Transceiver Characterization" section</li> </ul>
		<ul> <li>Removed all "Preliminary" designations.</li> </ul>