# E·XFL

## Intel - 5SGSMD8N3F45I3LN Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

## Details

Product Status	Obsolete
Number of LABs/CLBs	262400
Number of Logic Elements/Cells	695000
Total RAM Bits	51200000
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgsmd8n3f45i3ln

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

		saring transitions		
Symbol	Description	Condition (V)	Overshoot Duration as % @ T <sub>J</sub> = 100°C	Unit
		3.8	100	%
		3.85	64	%
		3.9	36	%
	AC input voltage	3.95	21	%
Vi (AC)		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Table 5. Maximum Allowed Overshoot During Transitions

#### Figure 1. Stratix V Device Overshoot Duration



Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub> I	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
		Fast POR	200 µs		4 ms	

### Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

#### Notes to Table 6:

(1)  $V_{CCPD}$  must be 2.5 V when  $V_{CCI0}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCI0}$  is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

## Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCA GXBL</sub>	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V <sub>CCR_GXBL</sub>	Receiver analog nower supply (left side)		0.87	0.90	0.93	v
(2) _	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	

				Calibration Accuracy				
Symbol	Description	Conditions	C1	C2,I2	C3,I3, I3YY	C4,14	Unit	
50-Ω R <sub>S</sub>	Internal series termination with calibration (50- $\Omega$ setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%	
34- $\Omega$ and 40- $\Omega$ R <sub>S</sub>	Internal series termination with calibration (34- $\Omega$ and 40- $\Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	±15	%	
48-Ω, 60-Ω, 80-Ω, and 240-Ω R <sub>S</sub>	Internal series termination with calibration (48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , and 240- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	±15	±15	±15	±15	%	
50-Ω R <sub>T</sub>	Internal parallel termination with calibration (50-Ω setting)	V <sub>CCI0</sub> = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%	
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration ( $20 - \Omega$ , $30 - \Omega$ , $40 - \Omega$ , $60 - \Omega$ , and $120 - \Omega$ setting)	V <sub>CCI0</sub> = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%	
60- $Ω$ and 120- $Ω$ R <sub>T</sub>	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V <sub>CCI0</sub> = 1.2	-10 to +40	-10 to +40	-10 to +40	-10 to +40	%	
$25-\Omega \\ R_{S\_left\_shift}$	Internal left shift series termination with calibration ( $25-\Omega$ R <sub>S_left_shift</sub> setting)	V <sub>CCI0</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%	

Table II. OUI Valiblation Accuracy specifications for Stratix V Devices' / (Latt 2 OF	Table 11.	<b>OCT Calibration A</b>	ccuracy Specificati	ons for Stratix V D	Devices <sup>(1)</sup> (	Part 2 of
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## Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance to PVT changes.

Table 12.	OCT Without Calibration	<b>Resistance</b> 1	<b>Tolerance</b>	<b>Specifications</b>	for Stratix	V Devices	(Part 1	of 2)
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			<b>Resistance Tolerance</b>				
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit
25-Ω R, 50-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	$V_{CCIO} = 3.0$ and 2.5 V	±30	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCI0</sub> = 1.8 and 1.5 V	±30	±30	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCI0</sub> = 1.2 V	±35	±35	±50	±50	%

			Re	esistance	Tolerance		
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit
50-Ω R <sub>S</sub>	Internal series termination without calibration (50- $\Omega$ setting)	$V_{CCIO} = 1.8$ and 1.5 V	±30	±30	±40	±40	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	±35	±35	±50	±50	%
100-Ω R <sub>D</sub>	Internal differential termination (100- $\Omega$ setting)	V <sub>CCPD</sub> = 2.5 V	±25	±25	±25	±25	%

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

## Equation 1. OCT Variation Without Recalibration for Stratix V Devices (1), (2), (3), (4), (5), (6)

$$R_{OCT} \,=\, R_{SCAL} \Big( 1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle \Big) \label{eq:ROCT}$$

### Notes to Equation 1:

- (1) The  $R_{OCT}$  value shows the range of OCT resistance with the variation of temperature and  $V_{CCIO}$ .
- (2) R<sub>SCAL</sub> is the OCT resistance value at power-up.
- (3)  $\Delta T$  is the variation of temperature with respect to the temperature at power-up.
- (4)  $\Delta V$  is the variation of voltage with respect to the V<sub>CCIO</sub> at power-up.
- (5) dR/dT is the percentage change of  $R_{\text{SCAL}}$  with temperature.
- (6) dR/dV is the percentage change of  $\mathsf{R}_{\mathsf{SCAL}}$  with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2)
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Symbol	Description	V <sub>CCIO</sub> (V)	Typical	Unit
		3.0	0.0297	
dR/dV	OCT variation with voltage without recalibration	2.5	0.0344	
		1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	

## **Internal Weak Pull-Up Resistor**

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Symbol	Description	V <sub>CCIO</sub> Conditions (V) <sup>(3)</sup>	Value <sup>(4)</sup>	Unit
		3.0 ±5%	25	kΩ
R <sub>PU</sub>		2.5 ±5%	25	kΩ
	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ
	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ
	pull-up resistor option.	1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k $\Omega$ .

- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V<sub>CCIO</sub>.
- (4) These specifications are valid with a  $\pm 10\%$  tolerance to cover changes over PVT.

## I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V<sub>IH</sub> and V<sub>IL</sub>), output voltage (V<sub>OH</sub> and V<sub>OL</sub>), and current drive characteristics (I<sub>OH</sub> and I<sub>OL</sub>) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V<sub>OL</sub> and V<sub>OH</sub> values are valid at the corresponding I<sub>OH</sub> and I<sub>OL</sub>, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012\_486.

I/O		V <sub>ccio</sub> (V)		VII	∟ (V)	VIH	(V)	V <sub>OL</sub> (V)	V <sub>OH</sub> (V)	V <sub>OH</sub> (V)	
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mA)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V <sub>CCIO</sub>	0.65 * V <sub>CCIO</sub>	V <sub>CCI0</sub> + 0.3	0.45	V <sub>CCI0</sub> – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V <sub>CCI0</sub>	0.65 * V <sub>CCI0</sub>	V <sub>CCI0</sub> + 0.3	0.25 * V <sub>CCIO</sub>	0.75 * V <sub>CCIO</sub>	2	-2

Table 17. Single-Ended I/O Standards for Stratix V Devices

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- **\*** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Transceiver Speed Grade 3			Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	DC Gain Setting = 0		0	_	_	0	_	_	0	—	dB
	DC Gain Setting = 1	_	2		_	2	_	_	2	_	dB
Programmable DC gain	DC Gain Setting = 2	_	4	_	_	4	_	_	4	_	dB
	DC Gain Setting = 3	_	6	_	_	6	_	_	6	_	dB
	DC Gain Setting = 4		8			8	—		8	_	dB
Transmitter											
Supported I/O Standards	_				-	1.4-V ar	nd 1.5-V PC	ML			
Data rate (Standard PCS)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS)	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
	85-Ω setting	_	85 ± 20%	_	_	85 ± 20%	_	_	85 ± 20%	—	Ω
Differential on-	100-Ω setting	_	100 ± 20%	_	_	100 ± 20%	_	_	100 ± 20%	_	Ω
chip termination resistors	120-Ω setting		120 ± 20%	_		120 ± 20%	_		120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_		150 ± 20%	_	Ω
V <sub>OCM</sub> (AC coupled)	0.65-V setting	_	650		_	650	_	_	650	—	mV
V <sub>OCM</sub> (DC coupled)	_	_	650	_	_	650		_	650	_	mV
Rise time <sup>(7)</sup>	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time <sup>(7)</sup>	80% to 20%	30		160	30		160	30	—	160	ps
Intra-differential pair skew	Tx V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	_	_	15			15		_	15	ps
Intra-transceiver block transmitter channel-to- channel skew	x6 PMA bonded mode	_	_	120	_	_	120	_		120	ps

## Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 5 of 7)

Table 26 shows the approximate maximum data rate using the 10G PCS.

Mode (2) Transceiver		PMA Width	64	40	40	40	32	32	
mode ""	Speed Grade	PCS Width	64	66/67	50	40	64/66/67	32	
	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6	
		C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5	
	2	C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88	
FIFO or Register		C1, C2, C2L, I2, I2L core speed grade							
		C3, I3, I3L core speed grade	8.5 Gbps						
	5	C4, I4 core speed grade							
		I3YY core speed grade	10.3125 Gbps						

Notes to Table 26:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Symbol/	Conditions	s	Transceive peed Grade	r 2	S	Transceive peed Grade	r 3	Unit		
Description		Min	Тур	Max	Min	Тур	Max			
Reference Clock								1		
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL								
otanuarus	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS								
Input Reference Clock Frequency (CMU PLL) <sup>(6)</sup>	_	40	_	710	40	_	710	MHz		
Input Reference Clock Frequency (ATX PLL) <sup>(6)</sup>	_	100	_	710	100	_	710	MHz		
Rise time	20% to 80%	_		400	_	_	400			
Fall time	80% to 20%			400	—	_	400	ps		
Duty cycle	—	45	_	55	45	_	55	%		
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz		
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%		
On-chip termination resistors <sup>(19)</sup>	_	_	100	_	_	100	_	Ω		
Absolute V <sub>MAX</sub> <sup>(3)</sup>	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V		
	RX reference clock pin	_	_	1.2	_	_	1.2			
Absolute V <sub>MIN</sub>	—	-0.4		—	-0.4	_		V		
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV		
V <sub>ICM</sub> (AC coupled)	Dedicated reference clock pin		1050/1000 <sup>(,</sup>	2)	1	050/1000 (	2)	mV		
	RX reference clock pin	1	.0/0.9/0.85 (	22)	1.	V				
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250		550	mV		

## Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)<sup>(1)</sup>

Symbol/	Conditions	S	Transceive peed Grade	2	S	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Differential on-chip termination resistors <sup>(7)</sup>	GT channels		100	_	_	100	_	Ω
	85- $\Omega$ setting	_	85 ± 30%	_	_	85 ± 30%	_	Ω
Differential on-chip	100-Ω setting	_	100 ± 30%	_	_	100 ± 30%	_	Ω
for GX channels <sup>(19)</sup>	120-Ω setting	_	120 ± 30%	_	—	120 ± 30%	—	Ω
	150-Ω setting		150 ± 30%	_	_	150 ± 30%	_	Ω
V <sub>ICM</sub> (AC coupled)	GT channels	_	650	_	—	650	—	mV
	VCCR_GXB = 0.85 V or 0.9 V	_	600	_	_	600	_	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 1.0 V full bandwidth	_	700		_	700	_	mV
	VCCR_GXB = 1.0 V half bandwidth	_	750	_	_	750	_	mV
t <sub>LTR</sub> <sup>(9)</sup>	—	_	—	10	—	—	10	μs
t <sub>LTD</sub> <sup>(10)</sup>		4			4	_	_	μs
t <sub>LTD_manual</sub> <sup>(11)</sup>		4	_		4	_	_	μs
t <sub>LTR_LTD_manual</sub> <sup>(12)</sup>	—	15	—	_	15	—	—	μs
Run Lenath	GT channels		—	72	—	—	72	CID
	GX channels				(8)			
CDR PPM	GT channels	_	—	1000	—	—	1000	± PPM
	GX channels				(8)			
Programmable	GT channels	_		14		_	14	dB
(AC Gain) <sup>(5)</sup>	GX channels				(8)			
Programmable	GT channels	_		7.5	_		7.5	dB
DC gain <sup>(6)</sup>	GX channels				(8)			
Differential on-chip termination resistors <sup>(7)</sup>	GT channels	_	100	—	_	100	_	Ω
Transmitter								
Supported I/O Standards	_			1.4-V	and 1.5-V P	CML		
Data rate (Standard PCS)	GX channels	600	_	8500	600		8500	Mbps
Data rate (10G PCS)	GX channels	600		12,500	600		12,500	Mbps

## Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5)<sup>(1)</sup>

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

## **Transceiver Characterization**

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

	Oanditiana		C1		C2,	C2L, I	2, I2L	C3, I3, I3L, I3YY		C4,14				
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t <sub>duty</sub>	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
	True Differential I/O Standards	_	_	160	_	_	160	_	_	200	_	_	200	ps
t <sub>rise</sub> & t <sub>fall</sub>	Emulated Differential I/O Standards with three external output resistor networks			250			250			250			300	ps
TCCS	True Differential I/O Standards	_	_	150	_	_	150	_	_	150	_	_	150	ps
	Emulated Differential I/O Standards			300			300	_		300			300	ps
Receiver														
	SERDES factor J = 3 to 10 (11), (12), (13), (14), (15), (16)	150		1434	150	_	1434	150	_	1250	150	_	1050	Mbps
True Differential 1/0 Standards	SERDES factor J ≥ 4 LVDS RX with DPA (12), (14), (15), (16)	150	_	1600	150	_	1600	150	_	1600	150	_	1250	Mbps
i/O Standards - f <sub>HSDRDPA</sub> (data rate)	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps

## Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 3 of 4)

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			<u> </u>
			-

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum	
SPI-4	00000000001111111111	2	128	640 data transitions	
Parallel Rapid I/O	00001111	2	128	640 data transitions	
	10010000	4	64	640 data transitions	
Miscellaneous	10101010	8	32	640 data transitions	
Wiscenareous	01010101	8	32	640 data transitions	

#### Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps.





Symbol	Description	Min	Max	Unit
t <sub>JPH</sub>	JTAG port hold time	5	—	ns
t <sub>JPCO</sub>	JTAG port clock to output	—	11 <sup>(1)</sup>	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output	—	14 <sup>(1)</sup>	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance	—	<b>14</b> <sup>(1)</sup>	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Notes to Table 46:

(1) A 1 ns adder is required for each V<sub>CCI0</sub> voltage step down from 3.0 V. For example,  $t_{JPC0} = 12$  ns if V<sub>CCI0</sub> of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## **Raw Binary File Size**

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) <sup>(4), (5)</sup>	
	500742	H35, F40, F35 <sup>(2)</sup>	213,798,880	562,392	
	JOUNAS	H29, F35 <sup>(3)</sup>	137,598,880	564,504	
	5SGXA4	—	213,798,880	563,672	
	5SGXA5	—	269,979,008	562,392	
	5SGXA7	—	269,979,008	562,392	
Stratix V GX	5SGXA9	—	342,742,976	700,888	
	5SGXAB	—	342,742,976	700,888	
	5SGXB5	—	270,528,640	584,344	
	5SGXB6	—	270,528,640	584,344	
	5SGXB9	—	342,742,976	700,888	
	5SGXBB	—	342,742,976	700,888	
Stratix V CT	5SGTC5	—	269,979,008	562,392	
	5SGTC7	—	269,979,008	562,392	
	5SGSD3	—	137,598,880	564,504	
	590904	F1517	213,798,880	563,672	
Strativ V CS	J303D4	_	137,598,880	564,504	
	5SGSD5		213,798,880	563,672	
	5SGSD6		293,441,888	565,528	
	5SGSD8	—	293,441,888	565,528	

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
	Disabled	Enabled	4
IFF XJZ	Enabled	Disabled	8
	Enabled	Enabled	8

Table 49.	DCLK-to-DATA[]	Ratio <sup>(1)</sup>	(Part 2 of 2)
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Note to Table 49:

(1) Depending on the DCLK-to-DATA [] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA [] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

## Figure 11. Single Device FPP Configuration Using an External Host



#### Notes to Figure 11:

- (1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device.  $V_{CCPGM}$  must be high enough to meet the  $V_{IH}$  specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with  $V_{CCPGM}$ .
- (2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.
- (3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (4) If you use FPP ×8, use DATA [7..0]. If you use FPP ×16, use DATA [15..0].

IF the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51.	<b>FPP</b> Timing	<b>Parameters</b> fo	r Stratix V	<b>Devices</b> When	the DCLK-	to-DATA[] Rati	o is >1 (	(1)
							• • • •	

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2		μS
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	μS
t <sub>CF2CK</sub> (5)	nCONFIG high to first rising edge on DCLK	1,506		μS
t <sub>ST2CK</sub> (5)	nSTATUS high to first rising edge of DCLK	2		μS
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5		ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	N-1/f <sub>DCLK</sub> (5)		S
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$		S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$		S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>		S
f	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t <sub>R</sub>	Input rise time	—	40	ns
t <sub>F</sub>	Input fall time	—	40	ns
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>CD2CU</sub> + (8576 × CLKUSR period) <sup>(4)</sup>	_	_

#### Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (5) N is the DCLK-to-DATA ratio and  $f_{\text{DCLK}}$  is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	—	μS
t <sub>status</sub>	nSTATUS low pulse width	268	1,506 <sup>(1)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	μS
t <sub>CF2CK</sub> (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t <sub>ST2CK</sub> (5)	nSTATUS high to first rising edge of DCLK	2	—	μS
t <sub>DSU</sub>	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	—	ns
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>	—	S
f <sub>MAX</sub>	DCLK frequency	—	125	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t <sub>cd2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU}$ + (8576 × CLKUSR period) <sup>(4)</sup>	_	_

## Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

## Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	<b>Clock Source</b>	Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles <sup>(1)</sup>
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP <sup>(2)</sup>	125 MHz	8576
DCLK	PS, FPP	125 MHz	

## Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

## **Remote System Upgrades**

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio
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Parameter	Minimum	Maximum	Unit
t <sub>RU_nCONFIG</sub> <sup>(1)</sup>	250	—	ns
t <sub>RU_nRSTIMER</sub> <sup>(2)</sup>	250	_	ns

#### Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## **User Watchdog Internal Circuitry Timing Specification**

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

### Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical Maximum		Units	
5.3	7.9	12.5	MHz	

## I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

## **Programmable IOE Delay**

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Deremeter	Min		Fast	Model				Slow N	lodel			
(1)	Settings	<b>Offset</b> (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

 Table 61. Document Revision History (Part 3 of 3)

Date	Version	Changes
		■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60
May 2013	2.7	Added Table 24, Table 48
		<ul> <li>Updated Figure 9, Figure 10, Figure 11, Figure 12</li> </ul>
February 2013	2.6	<ul> <li>Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46</li> </ul>
		Updated "Maximum Allowed Overshoot and Undershoot Voltage"
		<ul> <li>Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35</li> </ul>
		Added Table 33
		<ul> <li>Added "Fast Passive Parallel Configuration Timing"</li> </ul>
		<ul> <li>Added "Active Serial Configuration Timing"</li> </ul>
December 2012	2.5	<ul> <li>Added "Passive Serial Configuration Timing"</li> </ul>
		<ul> <li>Added "Remote System Upgrades"</li> </ul>
		<ul> <li>Added "User Watchdog Internal Circuitry Timing Specification"</li> </ul>
		Added "Initialization"
		Added "Raw Binary File Size"
	2.4	<ul> <li>Added Figure 1, Figure 2, and Figure 3.</li> </ul>
lune 2012		<ul> <li>Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.</li> </ul>
		<ul> <li>Various edits throughout to fix bugs.</li> </ul>
		Changed title of document to <i>Stratix V Device Datasheet</i> .
		<ul> <li>Removed document from the Stratix V handbook and made it a separate document.</li> </ul>
February 2012	2.3	■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.
December 2011	22	■ Added Table 2–31.
December 2011	2.2	■ Updated Table 2–28 and Table 2–34.
	0.1	<ul> <li>Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.</li> </ul>
November 2011	2.1	<ul> <li>Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.</li> </ul>
		<ul> <li>Various edits throughout to fix SPRs.</li> </ul>
		■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.
May 2011	2.0	<ul> <li>Updated the "DQ Logic Block and Memory Output Clock Jitter Specifications" title.</li> </ul>
		Chapter moved to Volume 1.
		<ul> <li>Minor text edits.</li> </ul>
		■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.
December 2010	1.1	<ul> <li>Converted chapter to the new template.</li> </ul>
		<ul> <li>Minor text edits.</li> </ul>
July 2010	1.0	Initial release.