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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	128300
Number of Logic Elements/Cells	340000
Total RAM Bits	19456000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5sgxea3h2f35i2ln">https://www.e-xfl.com/product-detail/intel/5sgxea3h2f35i2ln</a>

### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

**Table 9. I/O Pin Leakage Current for Stratix V Devices <sup>(1)</sup>**

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_I$	Input pin	$V_I = 0 \text{ V to } V_{CCIO\text{MAX}}$	-30	—	30	$\mu\text{A}$
$I_{OZ}$	Tri-stated I/O pin	$V_O = 0 \text{ V to } V_{CCIO\text{MAX}}$	-30	—	30	$\mu\text{A}$

**Note to Table 9:**

(1) If  $V_O = V_{CCIO}$  to  $V_{CCIO\text{MAX}}$ , 100  $\mu\text{A}$  of leakage current per I/O is expected.

### Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

**Table 10. Bus Hold Parameters for Stratix V Devices**

Parameter	Symbol	Conditions	V <sub>CCIO</sub>										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	μA
High sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	−22.5	—	−25.0	—	−30.0	—	−50.0	—	−70.0	—	μA
Low overdrive current	I <sub>ODL</sub>	0V < V <sub>IN</sub> < V <sub>CCIO</sub>	—	120	—	160	—	200	—	300	—	500	μA
High overdrive current	I <sub>ODH</sub>	0V < V <sub>IN</sub> < V <sub>CCIO</sub>	—	−120	—	−160	—	−200	—	−300	—	−500	μA
Bus-hold trip point	V <sub>TRIP</sub>	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 1 of 2)**

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3, I3YY	C4,I4	
25- $\Omega$ $R_S$	Internal series termination with calibration (25- $\Omega$ setting)	$V_{\text{CCIO}} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$	$\pm 15$	$\pm 15$	$\pm 15$	$\pm 15$	%

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) <sup>(1)</sup>**

Symbol	Description	V <sub>CCIO</sub> (V)	Typical	Unit
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/ <sup>o</sup> C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

**Note to Table 13:**

(1) Valid for a V<sub>CCIO</sub> range of  $\pm 5\%$  and a temperature range of 0° to 85°C.

**Pin Capacitance**

Table 14 lists the Stratix V device family pin capacitance.

**Table 14. Pin Capacitance for Stratix V Devices**

Symbol	Description	Value	Unit
C <sub>IOTB</sub>	Input capacitance on the top and bottom I/O pins	6	pF
C <sub>IOLR</sub>	Input capacitance on the left and right I/O pins	6	pF
C <sub>OUTFB</sub>	Input capacitance on dual-purpose clock output and feedback pins	6	pF

**Hot Socketing**

Table 15 lists the hot socketing specifications for Stratix V devices.

**Table 15. Hot Socketing Specifications for Stratix V Devices**

Symbol	Description	Maximum
I <sub>IOPIN</sub> (DC)	DC current per I/O pin	300 $\mu$ A
I <sub>IOPIN</sub> (AC)	AC current per I/O pin	8 mA <sup>(1)</sup>
I <sub>XCVR-TX</sub> (DC)	DC current per transceiver transmitter pin	100 mA
I <sub>XCVR-RX</sub> (DC)	DC current per transceiver receiver pin	50 mA

**Note to Table 15:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns,  $|I_{IOPIN}| = C \, dv/dt$ , in which C is the I/O pin capacitance and dv/dt is the slew rate.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 7 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{pll\_lock}^{(16)}$	—	—	—	10	—	—	10	—	—	10	μs

**Notes to Table 23:**

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the  $V_{CCR\_GXB}$  power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows  $V_{CCR\_GXB}$ .
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11)  $t_{LTR}$  is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12)  $t_{LTD}$  is time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high.
- (13)  $t_{LTD\_manual}$  is the time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14)  $t_{LTR\_LTD\_manual}$  is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx\_is\_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15)  $t_{pll\_powerdown}$  is the PLL powerdown minimum pulse width.
- (16)  $t_{pll\_lock}$  is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz  $\times$  100/f.
- (18) The maximum peak to peak differential input voltage  $V_{ID}$  after device configuration is equal to  $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$ .
- (19) For ES devices,  $R_{REF}$  is  $2000 \Omega \pm 1\%$ .
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz +  $20 \times \log(f/622)$ .
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with  $100 \Omega$ . The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 24 shows the maximum transmitter data rate for the clock network.

**Table 24. Clock Network Maximum Data Rate Transmitter Specifications <sup>(1)</sup>**

Clock Network	ATX PLL			CMU PLL <sup>(2)</sup>			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 <sup>(3)</sup>	14.1	—	6	12.5	—	6	3.125	—	3
x6 <sup>(3)</sup>	—	14.1	6	—	12.5	6	—	3.125	6
x6 PLL Feedback <sup>(4)</sup>	—	14.1	Side-wide	—	12.5	Side-wide	—	—	—
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

**Notes to Table 24:**

- (1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.
- (2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
- (3) Channel span is within a transceiver bank.
- (4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 25 shows the approximate maximum data rate using the standard PCS.

**Table 25. Stratix V Standard PCS Approximate Maximum Date Rate <sup>(1)</sup>, <sup>(3)</sup>**

Mode <sup>(2)</sup>	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
		C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
	3	C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
		I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
		C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
Register	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
		C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
	3	C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
		I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
		C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

**Notes to Table 25:**

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 27 shows the  $V_{OD}$  settings for the GX channel.

**Table 27. Typical  $V_{OD}$  Setting for GX Channel, TX Termination = 100  $\Omega$  <sup>(2)</sup>**

Symbol	$V_{OD}$ Setting	$V_{OD}$ Value (mV)	$V_{OD}$ Setting	$V_{OD}$ Value (mV)
<b><math>V_{OD}</math> differential peak to peak typical <sup>(3)</sup></b>	0 <sup>(1)</sup>	0	32	640
	1 <sup>(1)</sup>	20	33	660
	2 <sup>(1)</sup>	40	34	680
	3 <sup>(1)</sup>	60	35	700
	4 <sup>(1)</sup>	80	36	720
	5 <sup>(1)</sup>	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

**Note to Table 27:**

- (1) If TX termination resistance = 100 $\Omega$ , this VOD setting is illegal.
- (2) The tolerance is +/-20% for all VOD settings except for settings 2 and below.
- (3) Refer to Figure 2.

Figure 2 shows the differential transmitter output waveform.

**Figure 2. Differential Transmitter Output Waveform**

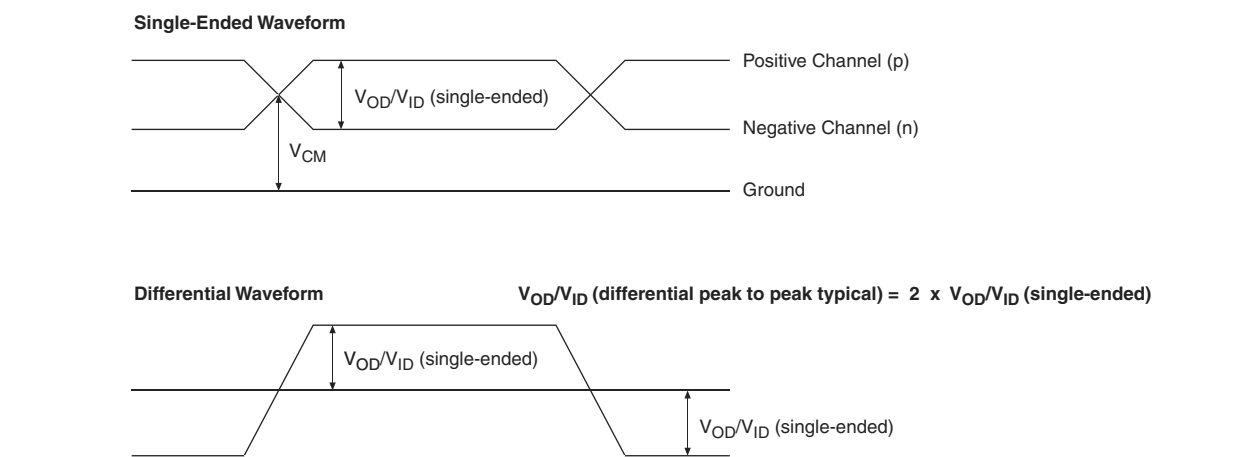


Figure 3 shows the Stratix V AC gain curves for GX channels.

**Figure 3. AC Gain Curves for GX Channels (full bandwidth)**



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.



## PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

**Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}$	Input clock frequency (C1, C2, C2L, I2, and I2L speed grades)	5	—	800 <sup>(1)</sup>	MHz
	Input clock frequency (C3, I3, I3L, and I3YY speed grades)	5	—	800 <sup>(1)</sup>	MHz
	Input clock frequency (C4, I4 speed grades)	5	—	650 <sup>(1)</sup>	MHz
$f_{INPFD}$	Input frequency to the PFD	5	—	325	MHz
$f_{FINPFD}$	Fractional Input clock frequency to the PFD	50	—	160	MHz
$f_{VCO}$ <sup>(9)</sup>	PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades)	600	—	1600	MHz
	PLL VCO operating range (C3, I3, I3L, I3YY speed grades)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grades)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
$f_{OUT}$	Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades)	—	—	717 <sup>(2)</sup>	MHz
	Output frequency for an internal global or regional clock (C3, I3, I3L speed grades)	—	—	650 <sup>(2)</sup>	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grades)	—	—	580 <sup>(2)</sup>	MHz
$f_{OUT\_EXT}$	Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades)	—	—	800 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C3, I3, I3L speed grades)	—	—	667 <sup>(2)</sup>	MHz
	Output frequency for an external clock output (C4, I4 speed grades)	—	—	553 <sup>(2)</sup>	MHz
$t_{OUTDUTY}$	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
$t_{FCOMP}$	External feedback clock compensation time	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic Configuration Clock used for <code>mgmt_clk</code> and <code>scanclk</code>	—	—	100	MHz
$t_{LOCK}$	Time required to lock from the end-of-device configuration or deassertion of <code>areset</code>	—	—	1	ms
$t_{DLOCK}$	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$f_{CLBW}$	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth <sup>(7)</sup>	—	4	—	MHz
$t_{PLL\_PSERR}$	Accuracy of PLL phase shift	—	—	±50	ps
$t_{ARESET}$	Minimum pulse width on the <code>areset</code> signal	10	—	—	ns

**Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{RES}$	Resolution of VCO frequency ( $f_{INPFD} = 100$ MHz)	390625	5.96	0.023	Hz

**Notes to Table 31:**

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is  $f_{IN}/N$  when  $N = 1$ .
- (5) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
  - a. Upstream PLL:  $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$  MHz
  - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 - 0.95 must be  $\geq 1000$  MHz, while  $f_{VCO}$  for fractional value range 0.20 - 0.80 must be  $\geq 1200$  MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05-0.95 must be  $\geq 1000$  MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.20-0.80 must be  $\geq 1200$  MHz.

## DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)**

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using one DSP								
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
Modes using two DSPs								
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)**

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using Three DSPs								
One complex 18 x 25	425	425	415	340	340	275	265	MHz
Modes using Four DSPs								
One complex 27 x 27	465	465	465	380	380	300	290	MHz

### Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

**Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 1 of 2)**

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
MLAB	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x16 depth <sup>(3)</sup>	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

**Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled**

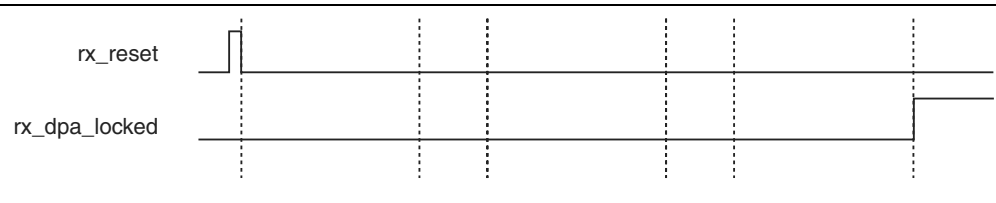


Table 37 lists the DPA lock time specifications for Stratix V devices.

**Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only <sup>(1), (2), (3)</sup>**

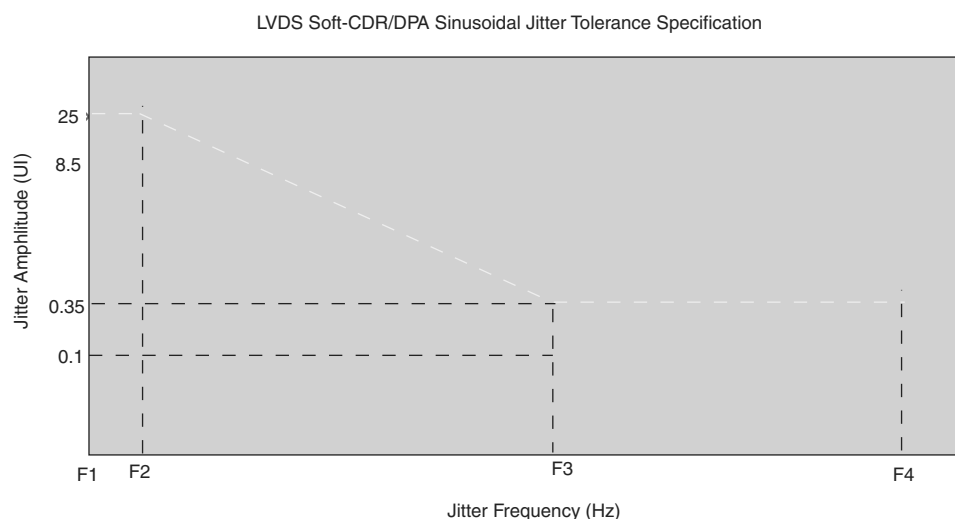
Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

**Notes to Table 37:**

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq 1.25$  Gbps. Table 38 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq 1.25$  Gbps.

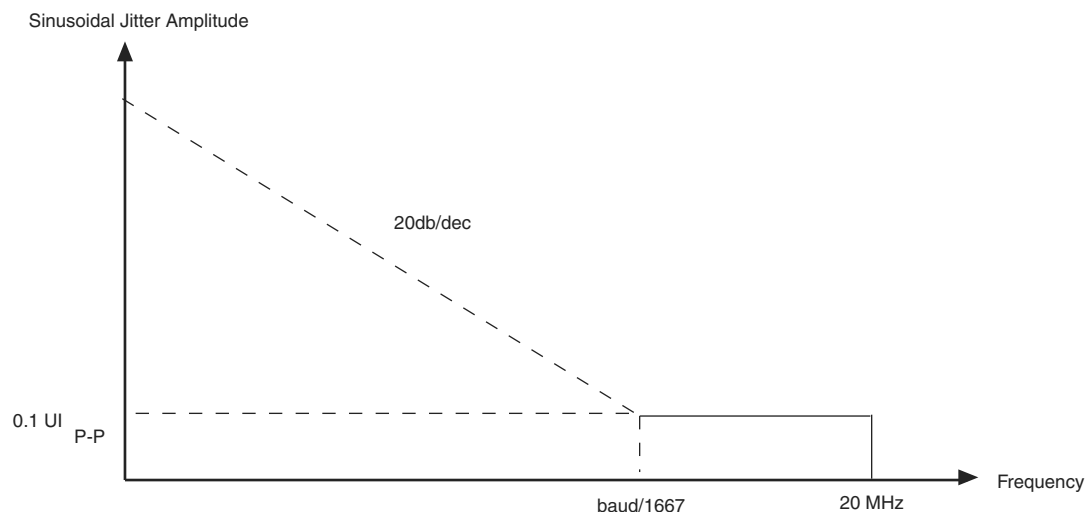
**Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $\geq 1.25$  Gbps**



**Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate  $\geq 1.25$  Gbps**

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $< 1.25$  Gbps.

**Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $< 1.25$  Gbps**

### DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 39. DLL Range Specifications for Stratix V Devices <sup>(1)</sup>**

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

**Note to Table 39:**

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

Symbol	Description	Min	Max	Unit
$t_{JPH}$	JTAG port hold time	5	—	ns
$t_{JPCO}$	JTAG port clock to output	—	11 <sup>(1)</sup>	ns
$t_{JPZX}$	JTAG port high impedance to valid output	—	14 <sup>(1)</sup>	ns
$t_{JPXZ}$	JTAG port valid output to high impedance	—	14 <sup>(1)</sup>	ns

**Notes to Table 46:**

- (1) A 1 ns adder is required for each  $V_{CCIO}$  voltage step down from 3.0 V. For example,  $t_{JPCO}$  = 12 ns if  $V_{CCIO}$  of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.
- (2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## Raw Binary File Size

For the POR delay specification, refer to the “POR Delay Specification” section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices”.

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

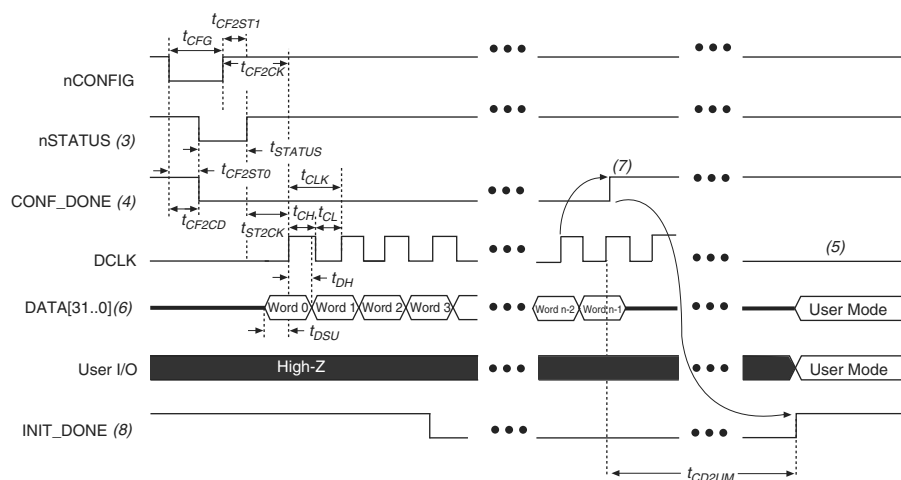
**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) <sup>(4), (5)</sup>
Stratix V GX	5SGXA3	H35, F40, F35 <sup>(2)</sup>	213,798,880	562,392
		H29, F35 <sup>(3)</sup>	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V GT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
Stratix V GS	5SGSD3	—	137,598,880	564,504
	5SGSD4	F1517	213,798,880	563,672
		—	137,598,880	564,504
	5SGSD5	—	213,798,880	563,672
	5SGSD6	—	293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

## FPP Configuration Timing when DCLK-to-DATA [] = 1

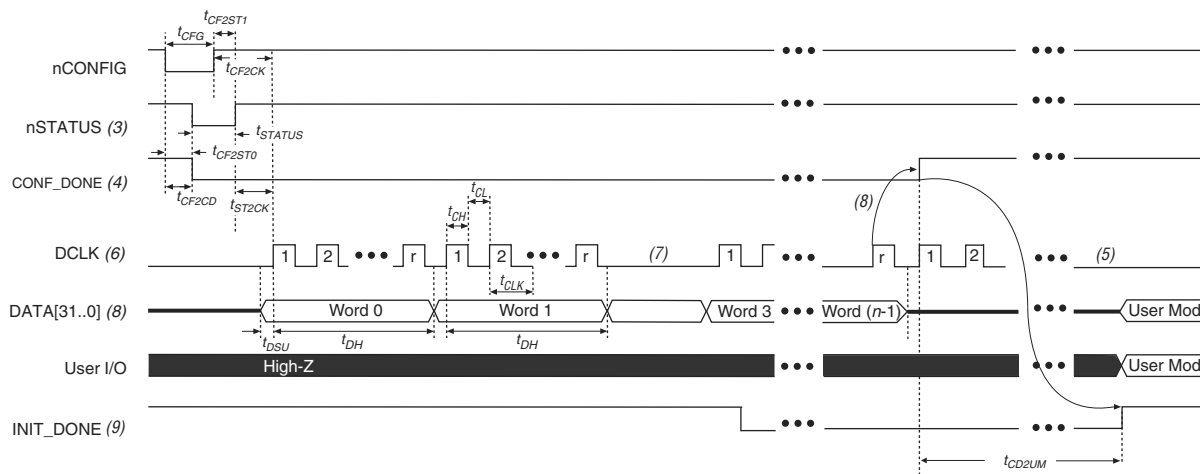
Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is 1.

**Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 <sup>(1), (2)</sup>**



### Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP x16, use DATA [15..0]. For FPP x8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

**Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)****Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.



**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)**

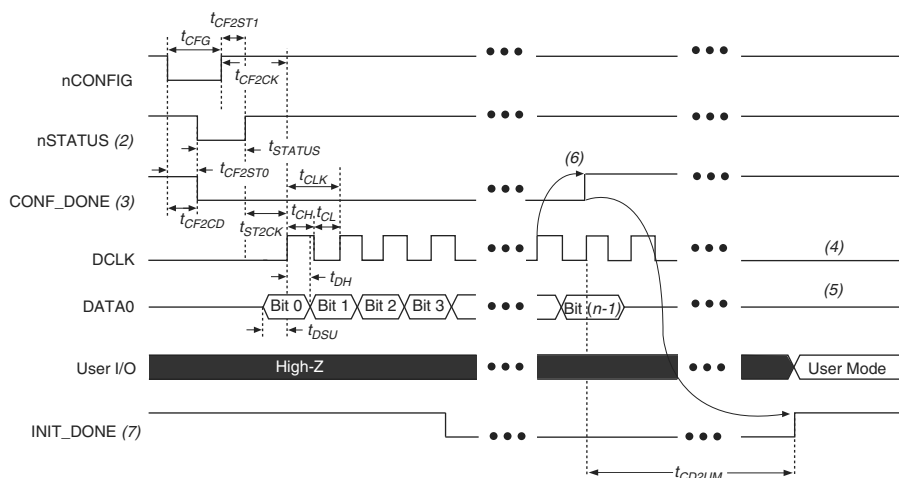
Symbol	Parameter	Minimum	Maximum	Units
$t_{CD2UM}$	CONF_DONE high to user mode <sup>(3)</sup>	175	437	μs
$t_{CD2CU}$	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
$t_{CD2UMC}$	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$	—	—

**Notes to Table 53:**

- (1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (2)  $t_{CF2CD}$ ,  $t_{CF2ST0}$ ,  $t_{CFG}$ ,  $t_{STATUS}$ , and  $t_{CF2ST1}$  timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.
- (3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

## Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

**Figure 15. PS Configuration Timing Waveform <sup>(1)</sup>****Notes to Figure 15:**

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF\_DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

**Table 54. PS Timing Parameters for Stratix V Devices**

Symbol	Parameter	Minimum	Maximum	Units
$t_{CF2CD}$	nCONFIG low to CONF_DONE low	—	600	ns
$t_{CF2ST0}$	nCONFIG low to nSTATUS low	—	600	ns
$t_{CFG}$	nCONFIG low pulse width	2	—	$\mu$ s
$t_{STATUS}$	nSTATUS low pulse width	268	1,506 <sup>(1)</sup>	$\mu$ s
$t_{CF2ST1}$	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	$\mu$ s
$t_{CF2CK}$ <sup>(5)</sup>	nCONFIG high to first rising edge on DCLK	1,506	—	$\mu$ s
$t_{ST2CK}$ <sup>(5)</sup>	nSTATUS high to first rising edge of DCLK	2	—	$\mu$ s
$t_{DSU}$	DATA [] setup time before rising edge on DCLK	5.5	—	ns
$t_{DH}$	DATA [] hold time after rising edge on DCLK	0	—	ns
$t_{CH}$	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CL}$	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CLK}$	DCLK period	$1/f_{MAX}$	—	s
$f_{MAX}$	DCLK frequency	—	125	MHz
$t_{CD2UM}$	CONF_DONE high to user mode <sup>(3)</sup>	175	437	$\mu$ s
$t_{CD2CU}$	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
$t_{CD2UMC}$	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$ <sup>(4)</sup>	—	—

**Notes to Table 54:**

- (1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section.
- (5) If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

## Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

**Table 55. Initialization Clock Source Option and the Maximum Frequency**

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles <sup>(1)</sup>
Internal Oscillator	AS, PS, FPP	12.5 MHz	8576
CLKUSR	AS, PS, FPP <sup>(2)</sup>	125 MHz	
DCLK	PS, FPP	125 MHz	

**Notes to Table 55:**

- (1) The minimum number of clock cycles required for device initialization.
- (2) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

## Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

Date	Version	Changes
June 2018	3.9	<ul style="list-style-type: none"> <li>■ Added the “Stratix V Device Overshoot Duration” figure.</li> </ul>
April 2017	3.8	<ul style="list-style-type: none"> <li>■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “PS Timing Parameters for Stratix V Devices” table.</li> <li>■ Changed the condition for <math>100\text{-}\Omega</math> <math>R_D</math> in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table.</li> </ul>
June 2016	3.7	<ul style="list-style-type: none"> <li>■ Added the <math>V_{ID}</math> minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table</li> <li>■ Added the <math>I_{OUT}</math> specification to the “Absolute Maximum Ratings for Stratix V Devices” table.</li> </ul>
December 2015	3.6	<ul style="list-style-type: none"> <li>■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> </ul>
December 2015	3.5	<ul style="list-style-type: none"> <li>■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table.</li> </ul>
July 2015	3.4	<ul style="list-style-type: none"> <li>■ Changed the data rate specification for transceiver speed grade 3 in the following tables: <ul style="list-style-type: none"> <li>■ “Transceiver Specifications for Stratix V GX and GS Devices”</li> <li>■ “Stratix V Standard PCS Approximate Maximum Date Rate”</li> <li>■ “Stratix V 10G PCS Approximate Maximum Data Rate”</li> </ul> </li> <li>■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Changed the <math>t_{CO}</math> maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table.</li> <li>■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> </ul>

**Table 61. Document Revision History (Part 2 of 3)**

Date	Version	Changes
November 2014	3.3	<ul style="list-style-type: none"> <li>■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.</li> <li>■ Added the I3YY speed grade to the <math>V_{CC}</math> description in Table 6.</li> <li>■ Added the I3YY speed grade to <math>V_{CCHIP\_L}</math>, <math>V_{CCHIP\_R}</math>, <math>V_{CCHSSI\_L}</math>, and <math>V_{CCHSSI\_R}</math> descriptions in Table 7.</li> <li>■ Added 240-<math>\Omega</math> to Table 11.</li> <li>■ Changed CDR PPM tolerance in Table 23.</li> <li>■ Added additional max data rate for fPLL in Table 23.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.</li> <li>■ Changed CDR PPM tolerance in Table 28.</li> <li>■ Added additional max data rate for fPLL in Table 28.</li> <li>■ Changed the mode descriptions for MLAB and M20K in Table 33.</li> <li>■ Changed the Max value of <math>f_{HCLK\_OUT}</math> for the C2, C2L, I2, I2L speed grades in Table 36.</li> <li>■ Changed the frequency ranges for C1 and C2 in Table 39.</li> <li>■ Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.</li> <li>■ Added note about nSTATUS to Table 50, Table 51, Table 54.</li> <li>■ Changed the available settings in Table 58.</li> <li>■ Changed the note in “Periphery Performance”.</li> <li>■ Updated the “I/O Standard Specifications” section.</li> <li>■ Updated the “Raw Binary File Size” section.</li> <li>■ Updated the receiver voltage input range in Table 22.</li> <li>■ Updated the max frequency for the LVDS clock network in Table 36.</li> <li>■ Updated the DCLK note to Figure 11.</li> <li>■ Updated Table 23 <math>VO_{CM}</math> (DC Coupled) condition.</li> <li>■ Updated Table 6 and Table 7.</li> <li>■ Added the DCLK specification to Table 55.</li> <li>■ Updated the notes for Table 47.</li> <li>■ Updated the list of parameters for Table 56.</li> </ul>
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the “Transceiver Characterization” section
October 2013	2.8	<ul style="list-style-type: none"> <li>■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59</li> <li>■ Added Figure 1 and Figure 3</li> <li>■ Added the “Transceiver Characterization” section</li> <li>■ Removed all “Preliminary” designations.</li> </ul>

**Table 61. Document Revision History (Part 3 of 3)**

Date	Version	Changes
May 2013	2.7	<ul style="list-style-type: none"> <li>■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60</li> <li>■ Added Table 24, Table 48</li> <li>■ Updated Figure 9, Figure 10, Figure 11, Figure 12</li> </ul>
February 2013	2.6	<ul style="list-style-type: none"> <li>■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46</li> <li>■ Updated “Maximum Allowed Overshoot and Undershoot Voltage”</li> </ul>
December 2012	2.5	<ul style="list-style-type: none"> <li>■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35</li> <li>■ Added Table 33</li> <li>■ Added “Fast Passive Parallel Configuration Timing”</li> <li>■ Added “Active Serial Configuration Timing”</li> <li>■ Added “Passive Serial Configuration Timing”</li> <li>■ Added “Remote System Upgrades”</li> <li>■ Added “User Watchdog Internal Circuitry Timing Specification”</li> <li>■ Added “Initialization”</li> <li>■ Added “Raw Binary File Size”</li> </ul>
June 2012	2.4	<ul style="list-style-type: none"> <li>■ Added Figure 1, Figure 2, and Figure 3.</li> <li>■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.</li> <li>■ Various edits throughout to fix bugs.</li> <li>■ Changed title of document to <i>Stratix V Device Datasheet</i>.</li> <li>■ Removed document from the Stratix V handbook and made it a separate document.</li> </ul>
February 2012	2.3	<ul style="list-style-type: none"> <li>■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.</li> </ul>
December 2011	2.2	<ul style="list-style-type: none"> <li>■ Added Table 2–31.</li> <li>■ Updated Table 2–28 and Table 2–34.</li> </ul>
November 2011	2.1	<ul style="list-style-type: none"> <li>■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.</li> <li>■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.</li> <li>■ Various edits throughout to fix SPRs.</li> </ul>
May 2011	2.0	<ul style="list-style-type: none"> <li>■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.</li> <li>■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title.</li> <li>■ Chapter moved to Volume 1.</li> <li>■ Minor text edits.</li> </ul>
December 2010	1.1	<ul style="list-style-type: none"> <li>■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.</li> <li>■ Converted chapter to the new template.</li> <li>■ Minor text edits.</li> </ul>
July 2010	1.0	Initial release.