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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	128300
Number of Logic Elements/Cells	340000
Total RAM Bits	19456000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxea3k1f35c2ln

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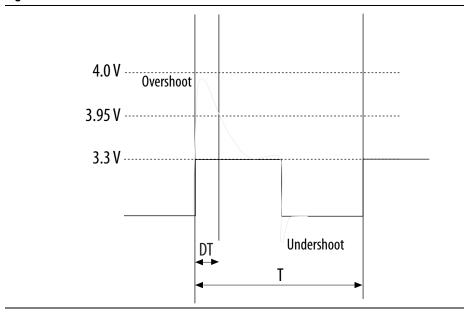
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Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 5. Maximum Allowed Overshoot During Transitions

Symbol	Description	Condition (V)	Overshoot Duration as % @ T _J = 100°C	Unit
		3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
Vi (AC)	AC input voltage	4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Figure 1. Stratix V Device Overshoot Duration



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Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

Symbol	Description	Condition	Min ⁽⁴⁾	Тур	Max ⁽⁴⁾	Unit
t	Power supply ramp time	Standard POR	200 μs	_	100 ms	_
LRAMP	Fower supply rainp line	Fast POR	200 μs	_	4 ms	_

Notes to Table 6:

- (1) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.
- (2) If you do not use the design security feature in Stratix V devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V_{CCBAT}. Stratix V devices will not exit POR if V_{CCBAT} stays at logic low.
- (3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.
- (4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
V _{CCA_GXBL}	Transceiver channel PLL power supply (left	GX, GS, GT	2.85	3.0	3.15	V
(1), (3)	side)	७४, ७७, ७१	2.375	2.5	2.625	V
V _{CCA_GXBR}	Transceiver channel PLL power supply (right	GX, GS	2.85	3.0	3.15	V
$(1), (\overline{3})$	side)	রম, রহ	2.375	2.5	2.625	V
V _{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V_{CCHIP_R}	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V _{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	0.87	0.90	0.93	V
(2)	Treceiver arialog power supply (left side)	un, us, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	

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Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Symbol	Description	V _{CC10} Conditions (V) ⁽³⁾	Value ⁽⁴⁾	Unit
		3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
	Value of the I/O pin pull-up resistor before	1.8 ±5%	25	kΩ
R _{PU}	and during configuration, as well as user mode if you enable the programmable	1.5 ±5%	25	kΩ
	pull-up resistor option.	1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

1/0		V _{CCIO} (V)		VII	_(V)	V _{IH}	(V)	V _{OL} (V)	V _{OH} (V)	I _{OL}	I _{OH}
Standard	Min	Тур	Max	Min	Max	Min	Max	Max	Min	(mĀ)	(mA)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} - 0.2	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.45	V _{CCIO} – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	-2

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 2 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	nsceive Grade	r Speed 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	_	0 to -0.5	_	%
On-chip termination resistors (21)	_	_	100	_	_	100	_	_	100	_	Ω
Absolute V _{MAX} ⁽⁵⁾	Dedicated reference clock pin	_	_	1.6	_	_	1.6	_	_	1.6	V
	RX reference clock pin	_	_	1.2	_	_	1.2	_	_	1.2	
Absolute V _{MIN}	_	-0.4		_	-0.4	_		-0.4	_	1	V
Peak-to-peak differential input voltage	_	200	_	1600	200		1600	200	_	1600	mV
V _{ICM} (AC coupled) (3)	Dedicated reference clock pin	1050/	1000/90	00/850 ⁽²⁾	1050/1000/900/850 ⁽²⁾ 1050/1000/900/850 ⁽²⁾		1050/1000/900/850 (2)		mV		
coupled) (9	RX reference clock pin	1.	.0/0.9/0	.85 ⁽⁴⁾	1.	0/0.9/0	.85 ⁽⁴⁾	1.	0/0.9/0	.85 ⁽⁴⁾	V
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	250	_	550	mV
	100 Hz	_	_	-70	_	_	-70	_	_	-70	dBc/Hz
Transmitter	1 kHz	_	_	-90	_	_	-90	_	_	-90	dBc/Hz
REFCLK Phase Noise	10 kHz		_	-100	_	_	-100	_	_	-100	dBc/Hz
(622 MHz) ⁽²⁰⁾	100 kHz	_	_	-110	_	_	-110	_	_	-110	dBc/Hz
	≥1 MHz	_	_	-120	_	_	-120	_	_	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) (17)	10 kHz to 1.5 MHz (PCle)	_	_	3	_	_	3	_	_	3	ps (rms)
R _{REF} (19)	_	_	1800 ±1%	_	_	1800 ±1%	_	_	180 0 ±1%	_	Ω
Transceiver Clock	<u> </u>			_			_			_	
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	_	100 or 125	_	MHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 4 of 7)

Symbol/	Conditions	Tra	nsceive Grade	r Speed 1	Trai	nsceive Grade	r Speed 2	Trai	nsceive Grade	r Speed 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	85– Ω setting	_	85 ± 30%	_	_	85 ± 30%	_	_	85 ± 30%	_	Ω
Differential on-	100–Ω setting	_	100 ± 30%		_	100 ± 30%	_	_	100 ± 30%	_	Ω
chip termination resistors ⁽²¹⁾	$120-\Omega$ setting $150-\Omega$ setting	_	120 ± 30%	_	_	120 ± 30%	_	_	120 ± 30%	_	Ω
		_	150 ± 30%	_	_	150 ± 30%	_	_	150 ± 30%	_	Ω
	V _{CCR_GXB} = 0.85 V or 0.9 V full bandwidth	_	600	_	_	600	_	_	600	_	mV
V _{ICM} (AC and DC coupled)	V _{CCR_GXB} = 0.85 V or 0.9 V half bandwidth	_	600	_	_	600	_	_	600	_	mV
coupleu)	$V_{CCR_GXB} = \\ 1.0 \text{ V/1.05 V} \\ \text{full} \\ \text{bandwidth}$	_	700	_	_	700	_	_	700	_	mV
	V _{CCR_GXB} = 1.0 V half bandwidth	_	750	_	_	750	_	_	750	_	mV
t _{LTR} (11)	_	_	_	10	_	_	10	_	_	10	μs
t _{LTD} (12)	_	4	_		4			4			μs
t _{LTD_manual} (13)	_	4	_		4			4			μs
t _{LTR_LTD_manual} (14)		15			15		_	15	_		μs
Run Length		_	_	200	_		200	_	-	200	UI
Programmable equalization (AC Gain) (10)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	_	_	16	_	_	16	_	_	16	dB

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Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 7 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1		Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit	
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
t _{pll_lock} (16)	_		_	10	_	_	10	_	_	10	μs

Notes to Table 23:

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows VCCR_GXB.
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t_{I TD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.
- (13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14) t_{LTR_LTD_manual} is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15) $t_{pll\ powerdown}$ is the PLL powerdown minimum pulse width.
- (16) t_{nll lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCle at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin V_{ICM}).
- (19) For ES devices, R_{REF} is 2000 Ω ±1%.
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

		ATX PLL			CMU PLL (2))		fPLL	
Clock Network	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non- bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 ⁽³⁾	14.1	_	6	12.5	_	6	3.125	_	3
x6 ⁽³⁾	_	14.1	6	_	12.5	6	_	3.125	6
x6 PLL Feedback ⁽⁴⁾	_	14.1	Side- wide	_	12.5	Side- wide	_	_	_
xN (PCIe)	_	8.0	8	_	5.0	8	_	_	_
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above	3.125	3.125	Up to 13 channels above
AN (NAUVE FITTIF)	П	8.01 to 9.8304	Up to 7 channels above and below PLL	· 7.55	7.88	and below PLL	3.123	3.123	and below PLL

Notes to Table 24:

⁽¹⁾ Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

⁽²⁾ ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

⁽³⁾ Channel span is within a transceiver bank.

⁽⁴⁾ Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Figure 2 shows the differential transmitter output waveform.

Figure 2. Differential Transmitter Output Waveform

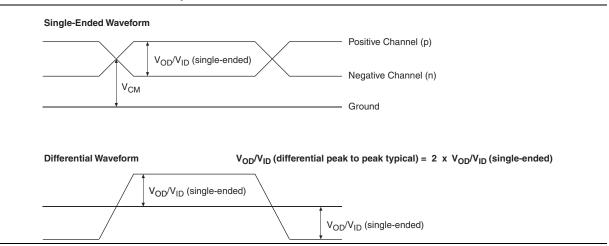


Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

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Figure 4 shows the differential transmitter output waveform.

Figure 4. Differential Transmitter/Receiver Output/Input Waveform

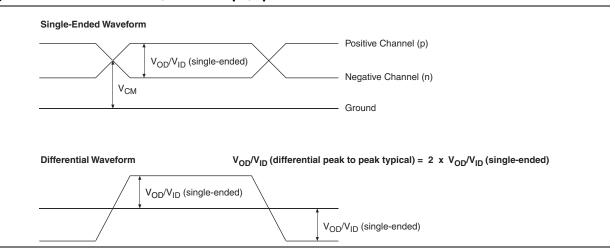


Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

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Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
→ (3) (4)	Input clock cycle-to-cycle jitter (f _{REF} ≥ 100 MHz)	_	_	0.15	UI (p-p)
t _{INCCJ} (3), (4)	Input clock cycle-to-cycle jitter (f _{REF} < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175 ⁽¹⁾	ps (p-p)
t _{OUTPJ_DC} (5)	Period Jitter for dedicated clock output (f _{OUT} < 100 MHz)	_	_	17.5 ⁽¹⁾	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
t _{FOUTPJ_DC} (5)	Period Jitter for dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)	_	_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} \ge 100 \text{ MHz})$	_	_	175	ps (p-p)
t _{outccj_dc} (5)	Cycle-to-Cycle Jitter for a dedicated clock output (f _{OUT} < 100 MHz)	_	_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	250 ⁽¹¹⁾ , 175 ⁽¹²⁾	ps (p-p)
t _{FOUTCCJ_DC} ⁽⁵⁾	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)+	_	_	25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾	mUI (p-p)
t _{OUTPJ_IO} (5),	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O (f _{OUT} < 100 MHz)	_	_	60	mUI (p-p)
t _{FOUTPJ 10} (5),	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	600 (10)	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f_{OUT} < 100 MHz)	_	_	60 (10)	mUI (p-p)
t _{outccj_10} (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \ge 100$ MHz)	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f_{OUT} < 100 MHz)	_	_	60 (10)	mUI (p-p)
t _{ғоитссу_10}	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100$ MHz)	_	_	600 (10)	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f_{OUT} < 100 MHz)	_	_	60	mUI (p-p)
t _{CASC_OUTPJ_DC}	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs (f _{OUT} < 100 MHz)	_	_	17.5	mUI (p-p)
f _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	_	_	±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k _{VALUE}	Numerator of Fraction	128	8388608	2147483648	_

Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

	Symbol	Parameter	Min	Тур	Max	Unit
f	RES	Resolution of VCO frequency (f _{INPFD} = 100 MHz)	390625	5.96	0.023	Hz

Notes to Table 31:

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4) f_{REF} is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz
 - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (10) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05 0.95 must be \geq 1000 MHz, while f_{VCO} for fractional value range 0.20 0.80 must be \geq 1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05-0.95 must be ≥ 1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20-0.80 must be ≥ 1200 MHz.

DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

			F	Peformano	e			
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes ı	ısing one	DSP				
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
		Modes u	sing two I)SPs				•
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

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Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

Mode		Peformance								
	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit		
		Modes us	ing Three	DSPs	•					
One complex 18 x 25	425	425	415	340	340	275	265	MHz		
Modes using Four DSPs										
One complex 27 x 27	465	465	465	380	380	300	290	MHz		

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 1 of 2)

Memory		Resources Used		Performance							
	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, I2L	13, 13L, 13YY	14	Unit
MLAB -	Single port, all supported widths	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	450	450	400	315	450	400	315	MHz
	Simple dual-port, x16 depth (3)	0	1	675	675	533	400	675	533	400	MHz
	ROM, all supported widths	0	1	600	600	500	450	600	500	450	MHz

Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 2 of 2)

		Resour	ces Used			Pe	erforman	ce			
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	525	525	455	400	525	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Notes to Table 33:

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Tei	mperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°	°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

Description	Min	Тур	Max	Unit
I _{bias} , diode source current	8	_	200	μΑ
V _{bias,} voltage across diode	0.3	_	0.9	V
Series resistance	_	_	<1	Ω
Diode ideality factor	1.006	1.008	1.010	_

⁽¹⁾ To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

⁽²⁾ When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

⁽³⁾ The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

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Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.



The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

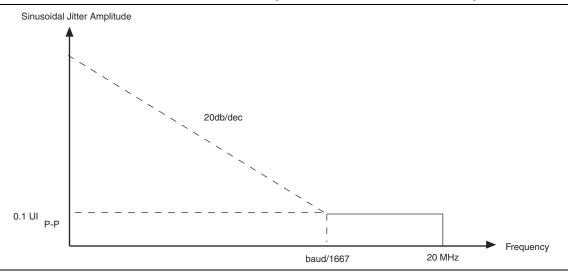
_														
Cumbal	Conditions		C1		C2,	C2L, I	2, I2L	C3,	13, I3L	., I3YY	C4,I4			Unit
Symbol	Conuntions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Ullit
f _{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (4)	5		800	5	_	800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards ⁽³⁾	Clock boost factor W = 1 to 40 (4)	5		800	5	_	800	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 (4)	5		520	5	_	520	5		420	5		420	MHz
f _{HSCLK_OUT} (output clock frequency)	_	5		800	5	_	800	5		625 (5)	5		525 (5)	MHz

Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate \geq 1.25 Gbps

Jitter F	requency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps



DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices (1)

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices (1), (2) (Part 1 of 2)

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

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Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices (1)

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	_	600	ns
t _{CF2ST0}	nconfig low to nstatus low	_	600	ns
t _{CFG}	nCONFIG low pulse width	2	_	μS
t _{STATUS}	nstatus low pulse width	268	1,506 ⁽²⁾	μ\$
t _{CF2ST1}	nCONFIG high to nSTATUS high	_	1,506 ⁽³⁾	μ\$
t _{CF2CK} (6)	nCONFIG high to first rising edge on DCLK	1,506	_	μ\$
t _{ST2CK} (6)	nSTATUS high to first rising edge of DCLK	2	_	μ\$
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	_	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	_	S
t _{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	_	S
t _{CLK}	DCLK period	1/f _{MAX}	_	S
f	DCLK frequency (FPP ×8/×16)	_	125	MHz
f _{MAX}	DCLK frequency (FPP ×32)	_	100	MHz
t _{CD2UM}	CONF_DONE high to user mode (4)	175	437	μS
+	GOVER DOVER high to GUVERN anabled	4 × maximum		
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	DCLK period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽⁵⁾	_	_

Notes to Table 50:

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nstatus low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

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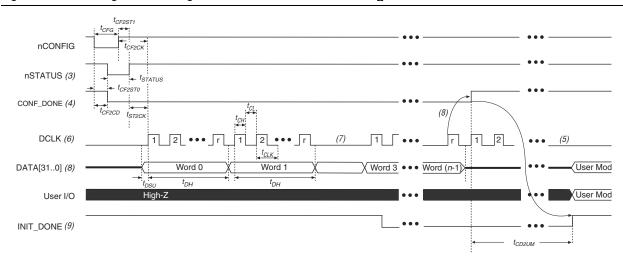


Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)

Notes to Figure 13:

- (1) Use this timing waveform and parameters when the DCLK-to-DATA [] ratio is >1. To find out the DCLK-to-DATA [] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nconfig, nstatus, and conf_done are at logic high levels. When nconfig is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA [31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT DONE pin is configured into the device, the INIT DONE goes low.

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Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51. FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is >1 $^{(1)}$

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nconfig low to conf_done low	_	600	ns
t _{CF2ST0}	nconfig low to nstatus low	_	600	ns
t _{CFG}	nCONFIG low pulse width	2	_	μS
t _{STATUS}	nstatus low pulse width	268	1,506 ⁽²⁾	μS
t _{CF2ST1}	nconfig high to nstatus high	_	1,506 ⁽²⁾	μS
t _{CF2CK} (5)	nconfig high to first rising edge on DCLK	1,506	_	μS
t _{ST2CK} (5)	nstatus high to first rising edge of DCLK	2	_	μS
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	N-1/f _{DCLK} ⁽⁵⁾	_	S
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	_	S
t _{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	_	S
t _{CLK}	DCLK period	1/f _{MAX}	_	S
f	DCLK frequency (FPP ×8/×16)	_	125	MHz
f _{MAX}	DCLK frequency (FPP ×32)	_	100	MHz
t _R	Input rise time	_	40	ns
t _F	Input fall time	_	40	ns
t _{CD2UM}	CONF_DONE high to user mode (3)	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽⁴⁾	_	_

Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nconfig or nstatus low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (5) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Page 68 Glossary

Table 60. Glossary (Part 4 of 4)

Letter	Subject	Definitions
	V _{CM(DC)}	DC common mode input voltage.
	V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
	V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	V _{IH(AC)}	High-level AC input voltage
	V _{IH(DC)}	High-level DC input voltage
V	V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	V _{IL(AC)}	Low-level AC input voltage
	V _{IL(DC)}	Low-level DC input voltage
	V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V _{SWING}	Differential input voltage
	V _X	Input differential cross point voltage
	V _{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
Χ		
Υ	_	_
Z		

Page 70 Document Revision History

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes
		■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.
		■ Added the I3YY speed grade to the V _{CC} description in Table 6.
	3.3	■ Added the I3YY speed grade to V _{CCHIP_L} , V _{CCHIP_R} , V _{CCHSSI_L} , and V _{CCHSSI_R} descriptions in Table 7.
		■ Added 240-Ω to Table 11.
		■ Changed CDR PPM tolerance in Table 23.
		■ Added additional max data rate for fPLL in Table 23.
		■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.
		■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.
		■ Changed CDR PPM tolerance in Table 28.
		■ Added additional max data rate for fPLL in Table 28.
		■ Changed the mode descriptions for MLAB and M20K in Table 33.
		■ Changed the Max value of f _{HSCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36.
November 2014		■ Changed the frequency ranges for C1 and C2 in Table 39.
		■ Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.
		■ Added note about nstatus to Table 50, Table 51, Table 54.
		■ Changed the available settings in Table 58.
		■ Changed the note in "Periphery Performance".
		■ Updated the "I/O Standard Specifications" section.
		■ Updated the "Raw Binary File Size" section.
		■ Updated the receiver voltage input range in Table 22.
		■ Updated the max frequency for the LVDS clock network in Table 36.
		■ Updated the DCLK note to Figure 11.
		■ Updated Table 23 VO _{CM} (DC Coupled) condition.
		■ Updated Table 6 and Table 7.
		■ Added the DCLK specification to Table 55.
		■ Updated the notes for Table 47.
		■ Updated the list of parameters for Table 56.
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the "Transceiver Characterization" section
	2.8	■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59
October 2013		■ Added Figure 1 and Figure 3
		■ Added the "Transceiver Characterization" section
		■ Removed all "Preliminary" designations.